FLASH MODULE

AVAILABLE AS MILITARY SPECIFICATIONS

•SMD 5962-97531
•MIL-STD-883

FEATURES

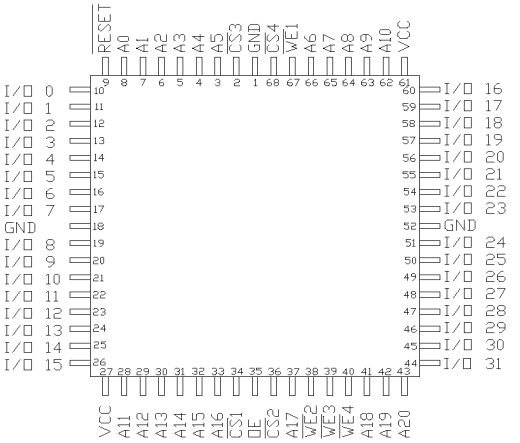
- SMD 5962-97531 Pending
- Fast Access Times: 90, 120 and 150ns
- Operation with single 5 volt supply
- Thirty-Two Equal Sectors of 64K Bytes for each 2Mx8
- Compatible with JEDEC EEPROM command set
- Any Combination of Sectors can be Erased
- Group Sector Protection
- Support Full Chip Erase
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built in decoupling caps for low noise operation
- Suspend Erase/Resume Function
- Individual Byte Read/ Write Control
- 10,000 Program/Erase Cycles

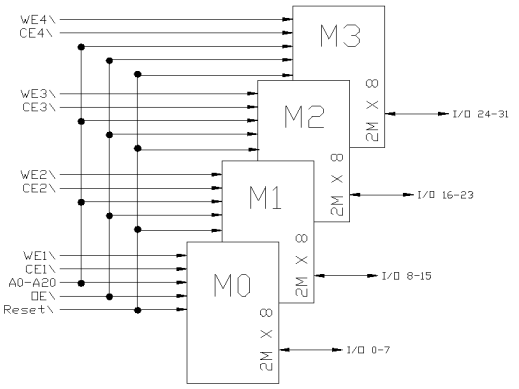
OPTION MARKING

- Timing
  - 90ns -9
  - 120ns -12
  - 150ns -15
- Packages
  - Ceramic Quad Flat Pack Q No.701

PIN ASSIGNMENT (Top View)

68 Lead CQFP





GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8F2M32 is a 32 Megabit CMOS FLASH Module organized as 2Meg x 32 bits. The AS8F2M32 achieves high speed access (90 to 150 ns), low power consumption and high reliability by employing advanced CMOS memory technology.

An on-chip state machine controls the program and erase functions. The embedded byte-program and sector/chip erase functions are fully automatic. Data-protection of any sector combination is accomplished using a hardware sector-protection feature.

The *Erase/Resume function* allows the sector erase operation to read data from, or program to a non-erasing sector, then resume the erase operation.

Device operations are selected by using standard commands into the command register using standard microprocessor write timings. The command register acts as an input to an internal state machine that interprets the commands, controls the erase and programming operations, outputs the status of the device, and outputs data stored in the device. On initial power-up operation, the device defaults to the read mode.

PIN DESCRIPTION	
I/O 0-31	Data Inputs/Output
A0 -A20	Address Input
WE\ 1-4	Write Enable
CE\ 1-4	Chip Enable
OE\	Output Enable
V_{CC}	Power
GND	Ground
RESET	Reset

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss

Vcc (Note 1) .....-0.5V to +6.0V
All Other Pins (Note 1).....-0.5V to +6.0V
V_{PP} Voltage Relative to V_{SS} (Note 2)..... -0.5V to +12.6V
RP# Voltage Relative to V_{SS} .....-0.5V to +12.6V
Operating Temperature, T_A (Ambient).....55°C to +125°C
Storage Temperature .....-65°C to +150°C
Power Dissipation.....1.5W
Short Circuit Output Current (Note 3).....200mA
Lead Temperature (soldering 10 seconds).....+300°C
Junction Temperature.....+165°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied, Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During Voltage transitions, inputs may overshoot Vss to -2.0V for periods of up to 20 ns. See Figure 2. Maximum DC voltage on input or I/O pins is Vcc +0.5V. During Voltage transitions, inputs may overshoot Vcc to +2.0V for periods of up to 20 ns. See Figure 3.

2. Minium DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 pins may overshoot Vss to -2.0V for periods of up to 20 ns. See Figure 2. Maximum DC input voltage on A9 is +12.5V inputs which may overshoot to +14V for periods of up to 20 ns. See Figure 3.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

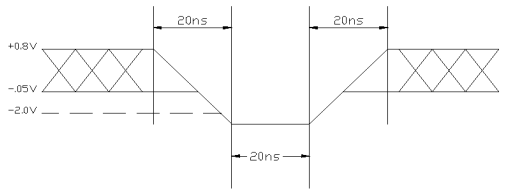

FIGURE 2.
Maximum Negative Overshoot Waveform

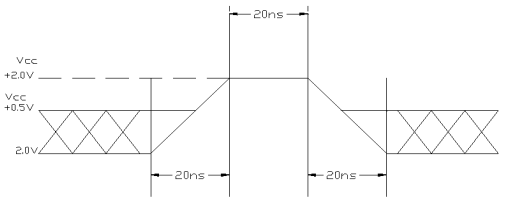

FIGURE 3.
Maximum Positive Overshoot Waveform

CAPACITANCE TABLE
V_{IN} = 0V, f = 1MHz, TA =25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS
C_{ADD}	A0-A20 Capactiance	50	pF
C_{OE}	OE\ Capactiance	50	pF
C_{WE}, C_{CE}	WE\ and CE\ Capactiance	20	pF
C_{IO}	I/O 0 - I/O 31 Capactiance	20	pF

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DC CHARACTERISTICS

CMOS Compatible

Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{CC}	Supply Voltage		4.5	5.5	V
V_{SS}	Ground		0	0	V
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}		±10.0	µA
I_{ID}	A9 Input Load Current (Note 3)	A9 = 12.5 V		200	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC}=V_{CC}$ Max		±10.0	µA
I_{CC1}	V_{cc} Active Current	CE\ = V_{IL}, OE\= V_{IH}, $V_{CC} = V_{CC}$ Max, f = 5MHz		160	mA
I_{CC2}	V_{cc} Active Current (Note 1,2)	CE\= VIL, OE\= VIH, $V_{CC} = V_{CC}$ Max, f = 5MHz		240	mA
I_{CC3}	V_{cc} Standby Current	$V_{CC} = V_{CC}$ Max, CE\ =V_{IH}, f = 5MHz, RESET\ = VCC+ 0.5V		8	mA
V_{IL}	Input Low Voltage		-.05	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC}+0.5	V
V_{ID}	Voltage for Sector Protected	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	A9 Output Low Voltage	I_{OL} = 12mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA, $V_{CC} = V_{CC}$ Min	0.85 x V_{CC}		V
V_{LKO}	Low V_{cc} Lock-out Voltage		3.2	4.2	V

Notes:

1. I_{CC} active while Embedded Program or Embedded Erase Algorithm is in progress.
2. Guaranteed but not tested.
3. Applies to 32 bit operations.

AC Read Characteristics

Parameter Symbol		Parameter Description		Speed Options			Units
JEDEC	Std.			-90	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 3)	Min	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	Max	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	Max	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Delay	Max	35	50	55	ns
t_{EHQZ}	t_{HZ}	Chip Enable High to Output High Z (Note 2, 3)	Max	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 2, 3)	Max	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE\ or OE\, Whichever Occurs First	Min	0	0	0	ns
	t_{Ready}	RST\ Low to Read Mode	Max	20	20	20	µs

Notes:

1. See Figure 9 and AC test conditionsTable for test conditions.
2. Output driver disable time.
3. Guaranteed but not tested.

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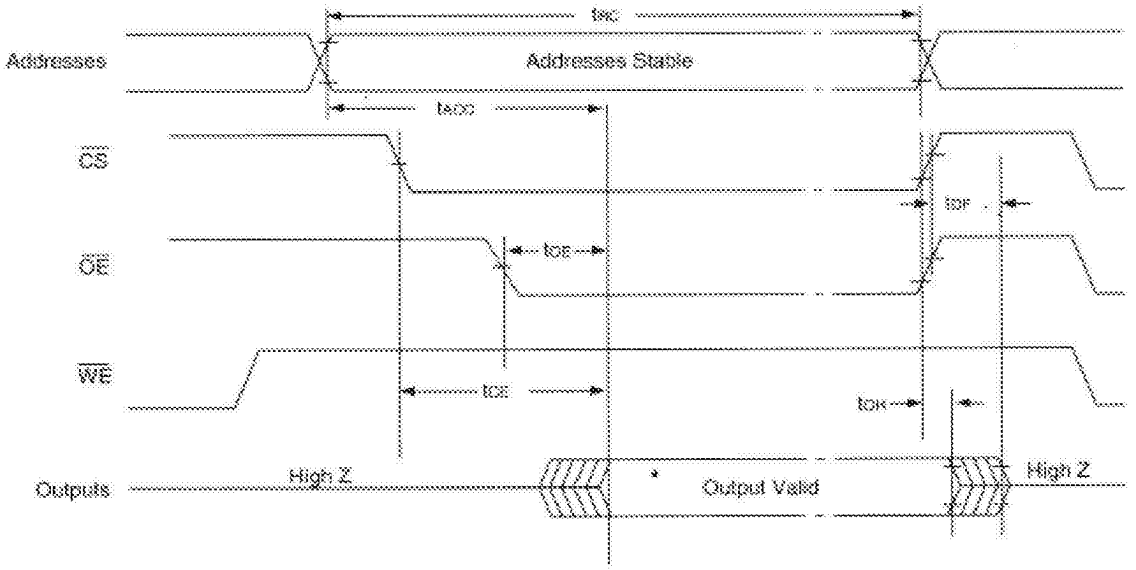
FIGURE 4. Read Operation Timings



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AC Characteristics

Erase and Program WE\ Controlled

Parameter Symbol		Parameter Description		Speed Options			Units
JEDEC	Std.			-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	45	50	50	ns
t_{ELWL}	t_{CE}	Chip Enable Setup Time			0		
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min		0		ns
t_{GHWL}	t_{GHWL}	Read Recover time Before Write (OE\ high to WE\ low)	Min		0		µs
	t_{OEH}	Output Enable Hold Time Note 1	Max		10		ns
t_{WLWH}	t_{WP}	Write Enable Pulse Width	Min	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min		20		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Max		1		ms
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Max		15		sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation	Max		480		sec
t_{VCHEL}		V_{CC} Setup Time	Min		50		µs
		Chip Program Time	Max		100		sec
	t_{RP}	Reset\ Pulse Width Note 2	Min		500		ns

Notes:
1. For Toggle and Data Polling
2. RESET internally tied to VCC for the default pin configuration in the CQFP Package.

FIGURE 5.
Reset Timing Diagram

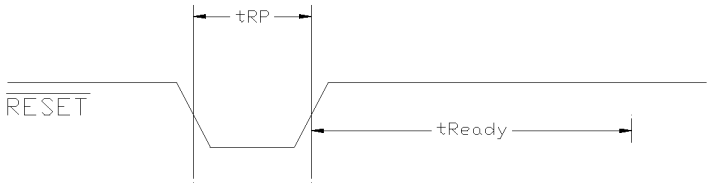

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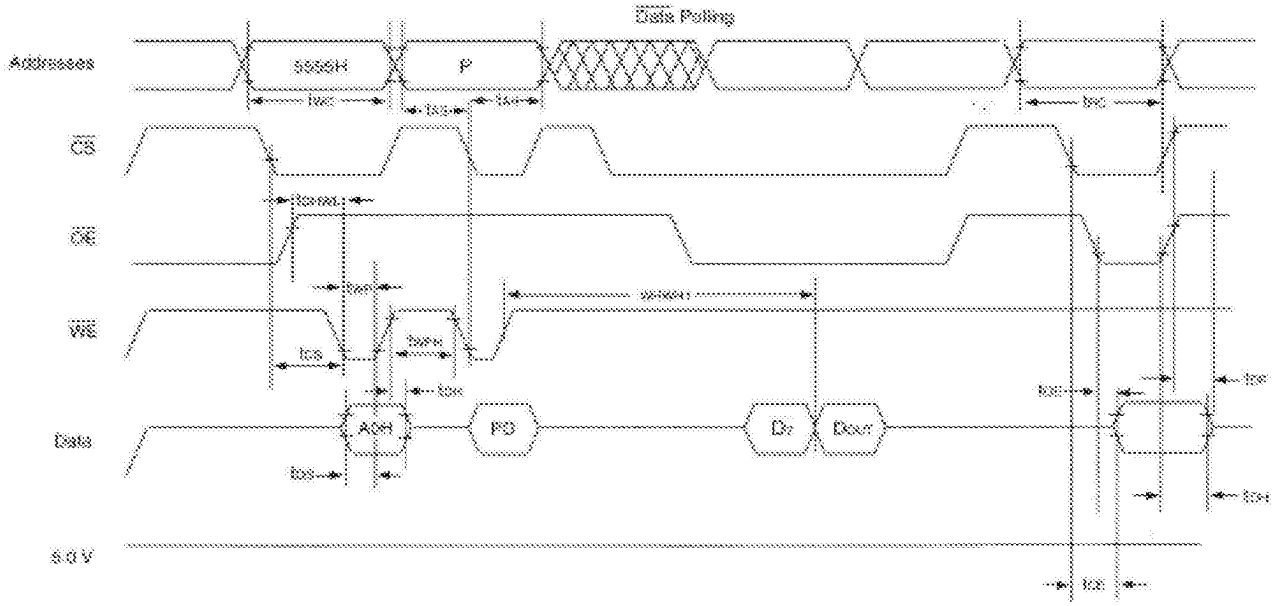
FIGURE 6. Program Operation Timings



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at the byte address.
3. D7 is the output of the complement of data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycle of four bus cycle sequence.

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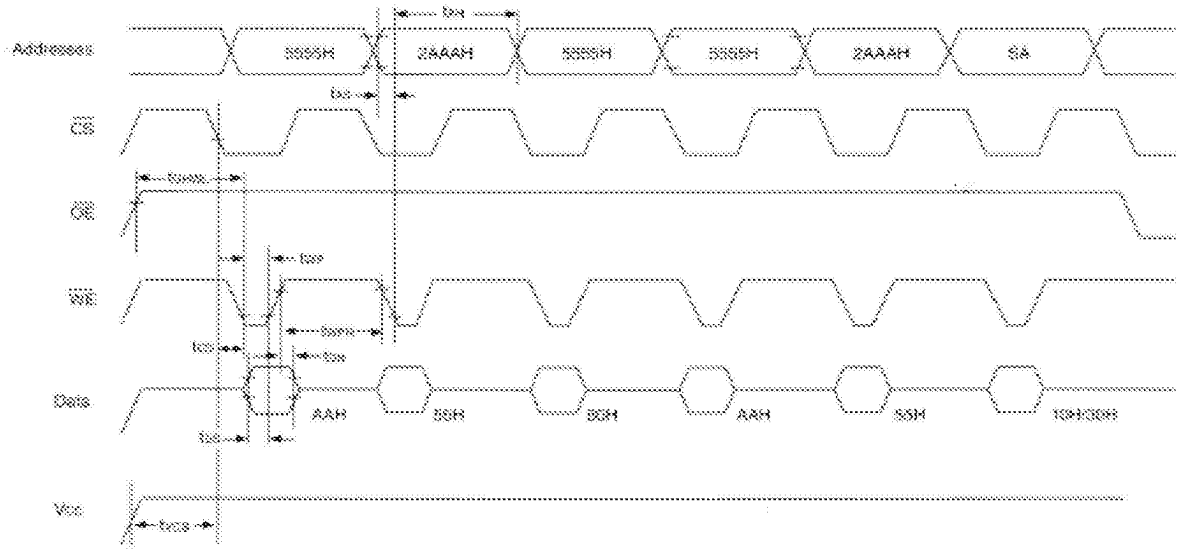
FIGURE 7. Chip/Sector Erase Operation Timings



NOTES:
1. SA is the sector address for Sector Erase.

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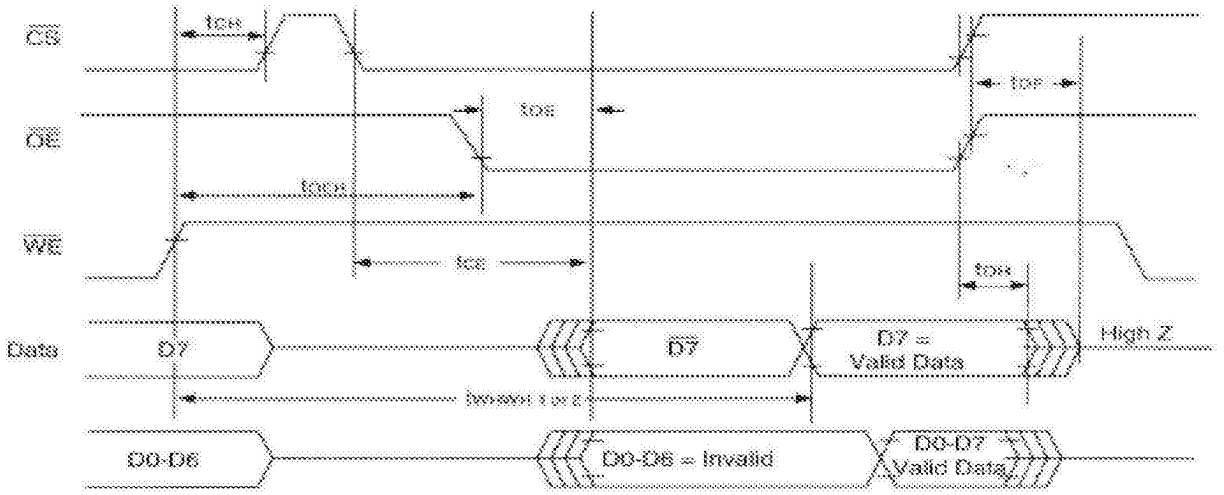
FIGURE 8. Data Polling Timings (During Emmbedded Algorithms)



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AC Characteristics

Erase and Program CE\ Controlled

Parameter Symbol		Parameter Description		Speed Options			Units
JEDEC	Std.			-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold time	Min		0		ns
t_{GHEL}	t_{GHEL}	Read Recover time Before Write	Min		0		µs
t_{WLEL}	t_{WS}	Setup time, Write Enable	Min		0		ns
	t_{OEH}	Output Enable Hold Time Note 1	Max		10		ns
t_{ELEH}	t_{CP}	Pulse Duration Chip Enable Low	Min	45	50	50	ns
t_{EHEL}	t_{CPH}	Pulse Duration Chip Enable High	Min		20		ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Max		1		ms
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Max		15		sec
		Chip Erase	Max		480		sec
		Chip Programming	Max		100		sec

Note:
1. For Toggle and Data Polling.

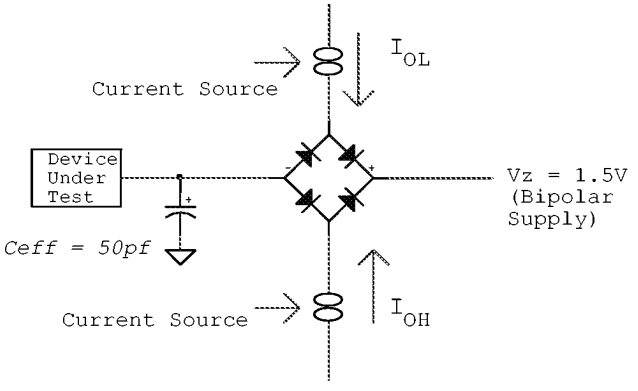

FIGURE 9.

AC TEST CONDITIONS

Notes:
Vz is programable from -2V to + 7V.
I_{OL} and I_{OH} programmable from 0 to 16 mA.
Vz is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.

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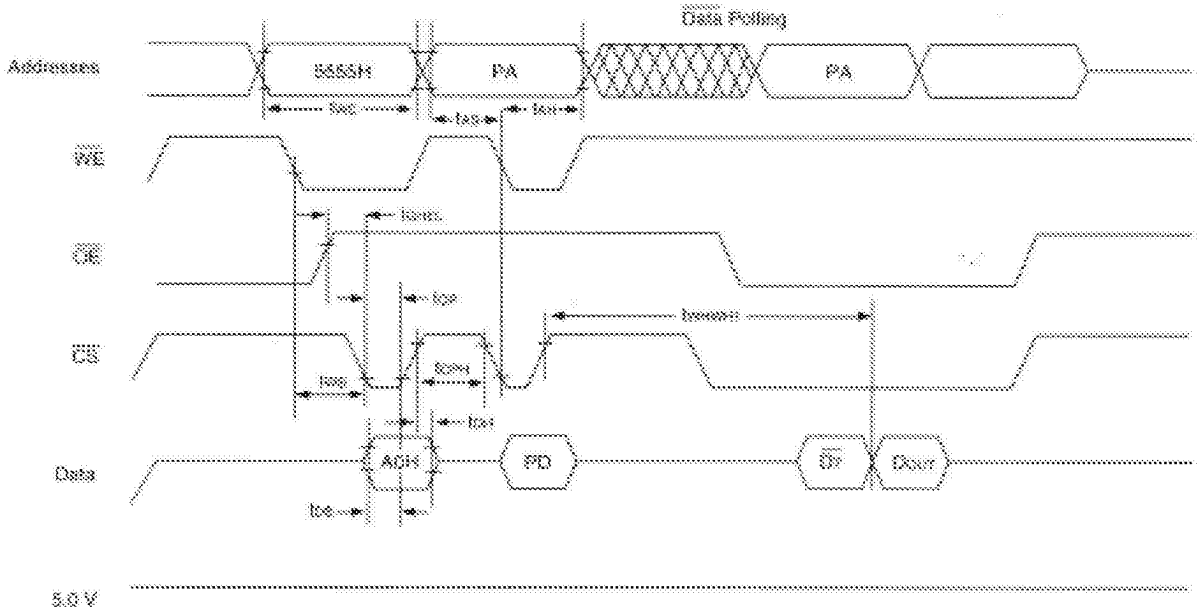
FIGURE 10. Alternate $\overline{CE}$ Controlled Write Operation Timings



NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at the byte address.
3. D7 is the output of the complement of data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycle of four bus cycle sequence.

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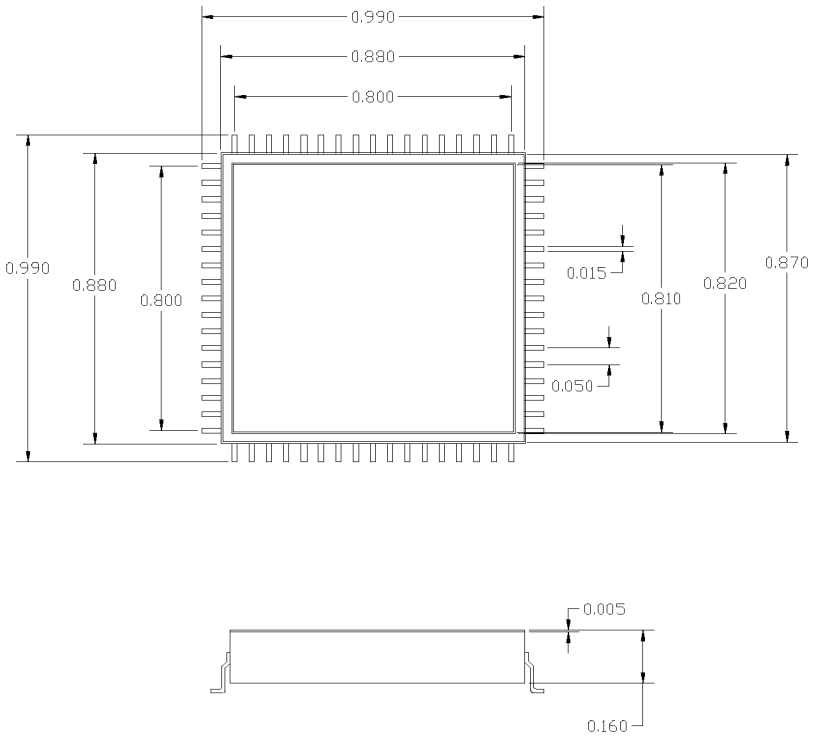
MECHANICAL DEFINITION

for the AS8F2MX32Q Ceramic Quad Flat Pack



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