V360EPC Rev. A0

LOCAL BUS TO PCI BRIDGE FOR DE-MULTIPLEXED A/D PROCESSORS

- Glueless interface to i960Cx/Hx and AMD29030/40 processors
- Configurable for primary master, bus master or target operation.
- Type 0 and type 1 configuration cycles.
- Up to 1Kbyte burst access on PCI or local.
- Large, 640-byte FIFOs using V3's unique *DYNAMIC BANDWIDTH ALLOCATION™* architecture
- 64-byte read FIFO per aperture.
- Enhanced support for 8/16-bit local bus devices with programmable region sizes.
- 3.3 volt support
- Dual bi-directional address space remapping
- Fully compliant with PCI 2.1 specification
- On-the-fly byte order (endian) conversion
- I_2O ATU and messaging unit including hardware controlled circular queues
- 2 channel DMA controller plus multiprocessor DMA chaining and demand mode DMA
- Hot swapping capability
- 16 8-bit bi-directional mailbox registers with doorbell interrupts
- Flexible PCI and local interrupt management
- Optional power-on serial EEPROM initialization
- 33MHz and 50MHz local bus versions
- Industrials Temperature Grade -40 to +85'C
- Low cost 160-pin EIAJ PQFP package

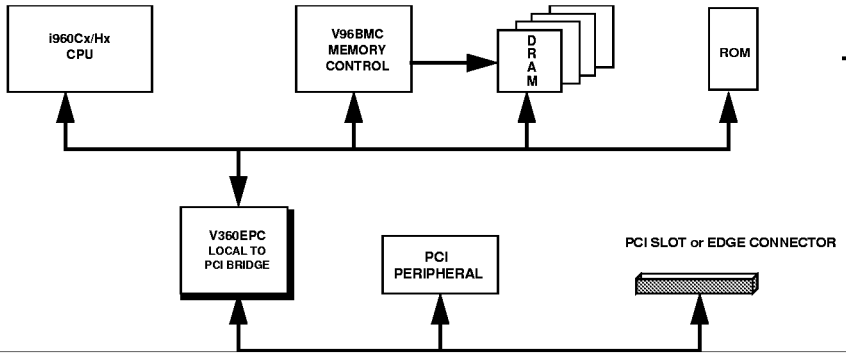
V360EPC provides the highest performance, most flexible, and most economical method to directly connect i960Cx/Hx or AMD2930/40 processors to the PCI bus. As a generic solution for 32-bit de-multiplexed local bus applications, V360EPC is also a suitable candidate for a variety of high-performance applications based on Motorola, IBM, DEC and Hitachi embedded processors - where a minimal amount of glue logic is needed.

V360EPC is the second generation of V3's I_2O ready PCI bridges - fully backward compatible with V962PBC and V292PBC Rev B2 devices - and is supporting powerful features like Hot Swap and DMA chaining. The PCI bus can be run at full 33MHz, independent of local bus clock rate. The overall throughput of the system is dramatically improved by increasing the FIFO depths and utilizing the unique *DYNAMIC BANDWIDTH ALLOCATION™* architecture.

Access to the PCI bus can be performed through two programmable address apertures. Two more apertures are provided for PCI-to-local bus accesses. There are 64-bytes of read FIFOs in each direction, 32-bytes dedicated for each aperture.

Two high-performance DMA channels with chaining and demand mode capabilities provide a powerful data transfer engine for bulk data transfers. Mailbox registers and flexible PCI interrupt controllers are also included to provide a simple mechanism to emulate PCI device control ports. The part is available in 160-pin low cost PQFP packages.

TYPICAL APPLICATION



This document contains the product codes, pinouts, package mechanical information, DC characteristics, and AC characteristics for the V360EPC. Detailed functional information is contained in the User's Manual.

V3 Semiconductor retains the rights to change documentation, specifications, or device functionality at any time without notice. Please verify that you have the latest copy of all documents before finalizing a design.

1.0 Product Codes

Table 1: Product Codes

Product Code	Processors	Bus Type	Package	Frequency
V360EPC-33 REV A0	i960Cx/Hx, AMD29030/40	32-bit de-multiplexed	160-pin EIAJ PQFP	33MHz
V360EPC-50 REV A0	i960Cx/Hx, AMD29030/40	32-bit de-multiplexed	160-pin EIAJ PQFP	50MHz

2.0 Pin Description and Pinout

Table 2 below lists the pin types found on the V360EPC. Table 3 describes the function of each pin on the V360EPC. Table 5 lists the pins by pin number. Figure 1 shows the pinout for the 160-pin EIAJ PQFP package and Figure 2 shows the mechanical dimensions of the package.

Table 2: Pin Types

Pin Type	Description
PCI I	PCI input only pin.
PCI O	PCI output only pin.
PCI I/O	PCI tri-state I/O pin.
PCI I/OD	PCI input with open drain output.
I/O_4	TTL I/O pin with 4mA output drive.
I	TTL input only pin.
O_4	TTL output pin with 4mA output drive.

Table 3: Signal Descriptions

PCI Bus Interface			
Signal	Type	R[a]	Description
AD[31:0]	PCI I/O	Z	Address and data, multiplexed on the same pins.
C/$\overline{\text{BE}}$[3:0]	PCI I/O	Z	Bus Command and Byte Enables, multiplexed on the same pins.
PAR	PCI I/O	Z	Parity represents even parity across AD[31:0] and C/$\overline{\text{BE}}$[3:0].
$\overline{\text{FRAME}}$	PCI I/O	Z	Cycle Frame indicates the beginning and burst length of an access.
$\overline{\text{IRDY}}$	PCI I/O	Z	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
$\overline{\text{TRDY}}$	PCI I/O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
$\overline{\text{STOP}}$	PCI I/O	Z	Stop indicates the current target is requesting the master to stop the current transaction (retry or disconnect).
$\overline{\text{DEVSEL}}$	PCI I/O	Z	Device Select, when actively driven by a target, indicates the driving device has decoded its address as the target of the current access. As an input to the initiator, DEVSEL indicates whether any device on the bus has been selected.
IDSEL	PCI I		Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
$\overline{\text{REQ}}$	PCI O	Z	Request indicates to the arbiter that this agent requests use of the bus.
$\overline{\text{GNT}}$	PCI I		Grant indicates to the agent that access to the bus has been granted.
PCLK	PCI I		PCLK provides timing for all transactions on the PCI bus.
$\overline{\text{PRST}}$	PCI I/O	Z/L	Acts as an input when RDIR is high, an output when RDIR is low. As an input it is asserted low to bring all internal PBC operation to a reset state.
$\overline{\text{PERR}}$	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{\text{SERR}}$	PCI I/OD	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
$\overline{\text{INT[A:D]}}$	PCI I/OD	Z	Level-sensitive interrupt requests may be received or generated.

Table 3: Signal Descriptions (cont'd)

Local Bus Interface			
Signal	Type	R	Description
LD[31:0] ID[31:0][b]	I/O4	Z	Local multiplexed address and data bus.
LA[31:2]	I/O4	Z	Local address bus.
$\overline{\text{BE[3:0]}}$ $\overline{\text{BWE[3:0]}}$[b]	I/O4	Z	Local bus byte enables.
W/$\overline{\text{R}}$ R/$\overline{\text{W}}$[b]	I/O4	Z	Read-Write strobe.
$\overline{\text{ADS}}$ $\overline{\text{LREQ}}$[b]	I/O4	Z	Asserted low to indicate the beginning of a bus cycle.
$\overline{\text{READY}}$ $\overline{\text{RDY}}$[c]	I/O4	Z	Local Bus data ready
$\overline{\text{HOLD}}$ $\overline{\text{LBREQ}}$[b]	O4	L	Local bus hold request: asserted by the chip to initiate a local bus master cycle.
$\overline{\text{HOLDA}}$ $\overline{\text{LBGRT}}$[b]	I		Local bus hold acknowledge.
LPAR[3:0]	I/O4	Z	Local bus parity.
$\overline{\text{BLAST}}$ $\overline{\text{BURST}}$[b]	I/O4	Z	Burst last[c]. Burst request[b].
$\overline{\text{BTERM}}$ $\overline{\text{ERR}}$[b]	I/O4	Z	Bus Time-out. Burst terminate[c].
$\overline{\text{LINT}}$	O4	H	Local interrupt request.
$\overline{\text{LRST}}$	I/O4	L/Z	Local bus RESET signal.
LCLK MEMCLK[b]	I		Local bus clock.

Serial EEPROM Interface			
Signal	Type	R	Description
SCL/$\overline{\text{LPERR}}$	O4	X	EEPROM clock. Local parity error.
SDA	I/O4	X	EEPROM data.

Table 3: Signal Descriptions (cont'd)

Configuration			
Signal	Type	R	Description
RDIR	I		Reset direction. Tie low to drive $\overline{\text{PRST}}$ out and $\overline{\text{LRST}}$ in, high to drive $\overline{\text{LRST}}$ out and $\overline{\text{PRST}}$ in.
$\overline{\text{EN5V}}$	I		Selects 5V ($\overline{\text{EN5V}}$ driven low) or 3.3V ($\overline{\text{EN5V}}$ driven high) device operation modes.
Power and Ground Signals			
Signal	Type	R	Description
V_{CC}	-		POWER leads intended for external connection to a V_{CC} board plane.
GND	-		GROUND leads intended for external connection to a GND board plane.

a. **R** indicates state during reset.
b. Applies to AMD29030/40 mode.
c. Applies to i960Cx/Hx mode.

2.1 Test Mode Pins

Several device pins are used during manufacturing test to put the V360EPC device into various test modes. ***These pins must be maintained at proper levels during reset to insure proper operation.*** This is typically handled through pull-up or pull-down resistors (typically 1K to 10K) on the signal pins if they are not guaranteed to be at the proper level during reset. Table 4 below shows the reset states for test mode pins:

Table 4: RESET State for Test Mode Pins

Mode	Pin 134	Pin 135	Pin 153
i960Cx/Hx	Pull-Up	Pull-Up	Pull-Up
AMD2930/40	Pull-Down	Pull-Up	Pull-Up

Table 5: Pin Assignments

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	V_{CC}	41	V_{CC}	81	V_{CC}	121	V_{CC}
2	$\overline{\text{INTD}}$	42	AD14	82	LA23	122	LA6
3	$\overline{\text{PRST}}$	43	AD13	83	LD8/ID8	123	LD25/ID25
4	PCLK	44	AD12	84	LA22	124	LA5
5	$\overline{\text{GNT}}$	45	AD11	85	LD9/ID9	125	LD26/ID26
6	$\overline{\text{REQ}}$	46	AD10	86	LA21	126	LA4
7	AD31	47	AD9	87	LD10/ID10	127	LD27/ID27
8	AD30	48	AD8	88	LA20	128	LA3
9	AD29	49	C/$\overline{\text{BE0}}$	89	LD11/ID11	129	LD28/ID28
10	AD28	50	V_{CC}	90	LA19	130	LA2
11	GND	51	GND	91	LD12/ID12	131	LD29/ID29
12	AD27	52	AD7	92	LA18	132	LD30/ID30
13	AD26	53	AD6	93	LD13/ID13	133	LD31/ID31
14	AD25	54	AD5	94	LA17	134	'1' '0'[a]
15	AD24	55	AD4	95	LD14/ID14	135	$\overline{\text{BTERM}}$ $\overline{\text{ERR}}$[a]
16	C/$\overline{\text{BE3}}$	56	AD3	96	LA16	136	$\overline{\text{READY}}$ $\overline{\text{RDY}}$[a]
17	IDSEL	57	AD2	97	LD15/ID15	137	$\overline{\text{HOLD}}$ LBREQ[a]
18	AD23	58	AD1	98	LA15	138	$\overline{\text{HOLDA}}$ $\overline{\text{LBGNT}}$[a]
19	AD22	59	AD0	99	LD16/ID16	139	$\overline{\text{ADS}}$ LREQ[a]
20	V_{CC}	60	V_{CC}	100	V_{CC}	140	V_{CC}
21	GND	61	GND	101	GND	141	GND
22	AD21	62	LD0/ID0	102	LA14	142	LCLK MEMCLK[a]

Table 5: Pin Assignments (cont'd)

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
23	AD20	63	LA31	103	LD17/ID17	143	$\overline{EN5V}$
24	AD19	64	LD1/ID1	104	LA13	144	V_{CC}
25	AD18	65	LA30	105	LD18/ID18	145	$\overline{BE3}$ / $\overline{BWE3}$[a]
26	AD17	66	LD2/ID2	106	LA12	146	$\overline{BE2}$ / $\overline{BWE2}$[a]
27	AD16	67	LA29	107	LD19/ID19	147	$\overline{BE1}$ / $\overline{BWE1}$[a]
28	C/$\overline{BE2}$	68	LD3/ID3	108	LA11	148	$\overline{BE0}$ / $\overline{BWE0}$[a]
29	$\overline{FRAME}$	69	LA28	109	LD20/ID20	149	$\overline{BLAST}$ / $\overline{BURST}$[a]
30	GND	70	LD4/ID4	110	LA10	150	W/$\overline{R}$ R/$\overline{W}$[a]
31	$\overline{IRDY}$	71	LA27	111	LD21/ID21	151	RDIR
32	$\overline{TRDY}$	72	LD5/ID5	112	LA9	152	$\overline{LRST}$
33	$\overline{DEVSEL}$	73	LA26	113	LD22/ID22	153	'1'
34	$\overline{STOP}$	74	LD6/ID6	114	LA8	154	$\overline{LINT}$
35	$\overline{PERR}$	75	LA25	115	LD23/ID23	155	SDA
36	$\overline{SERR}$	76	LD7/ID7	116	LA7	156	SCL/ LPERR
37	PAR	77	LA24	117	LPAR2	157	$\overline{INTA}$
38	C/$\overline{BE1}$	78	LPAR0	118	LPAR3	158	$\overline{INTB}$
39	AD15	79	LPAR1	119	LD24/ID24	159	$\overline{INTC}$
40	GND	80	GND	120	GND	160	GND

a. Applies to AMD29030/40 mode.

Figure 1: Pinout for 160-pin EIAJ PQFP (top view)

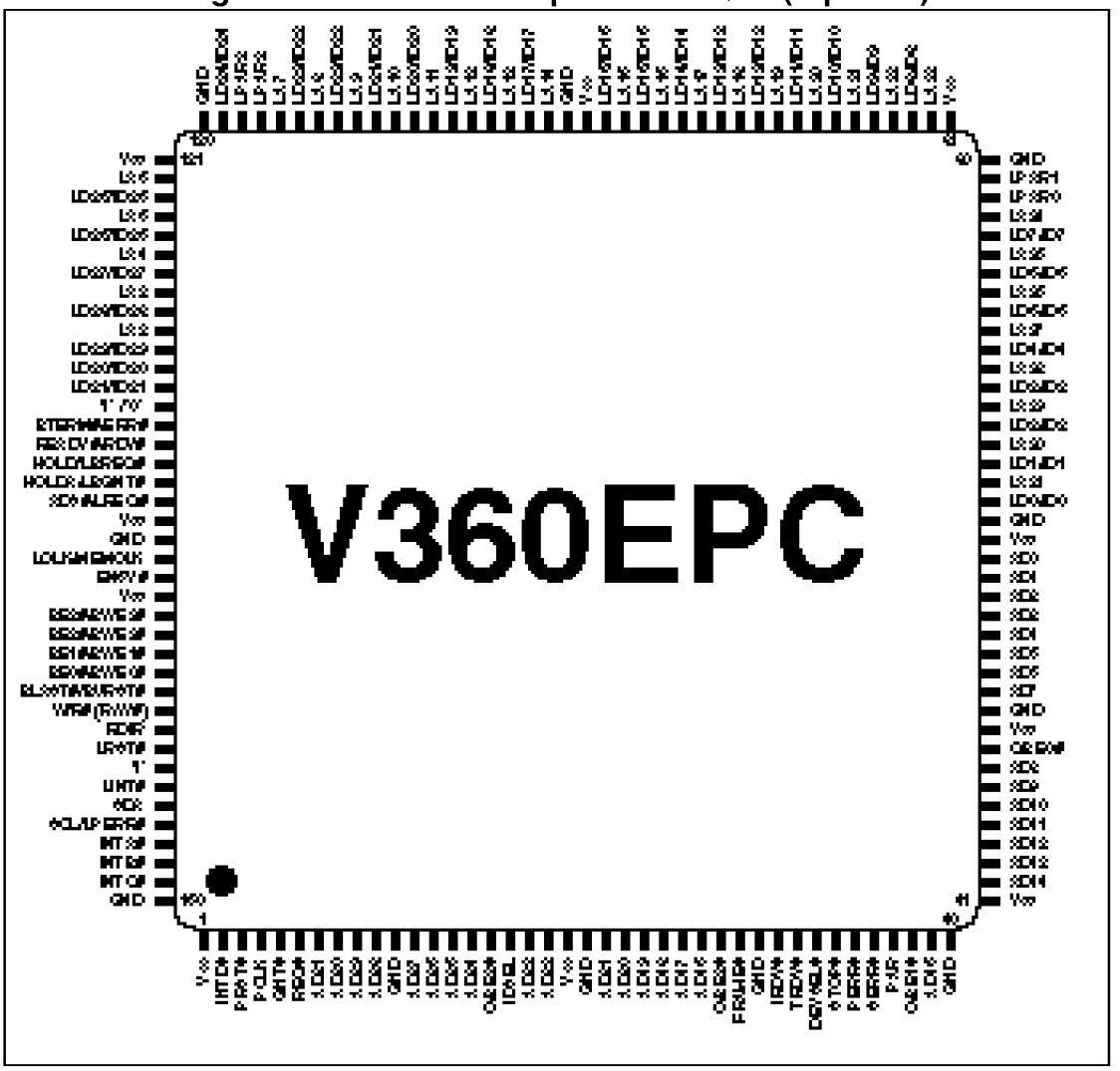
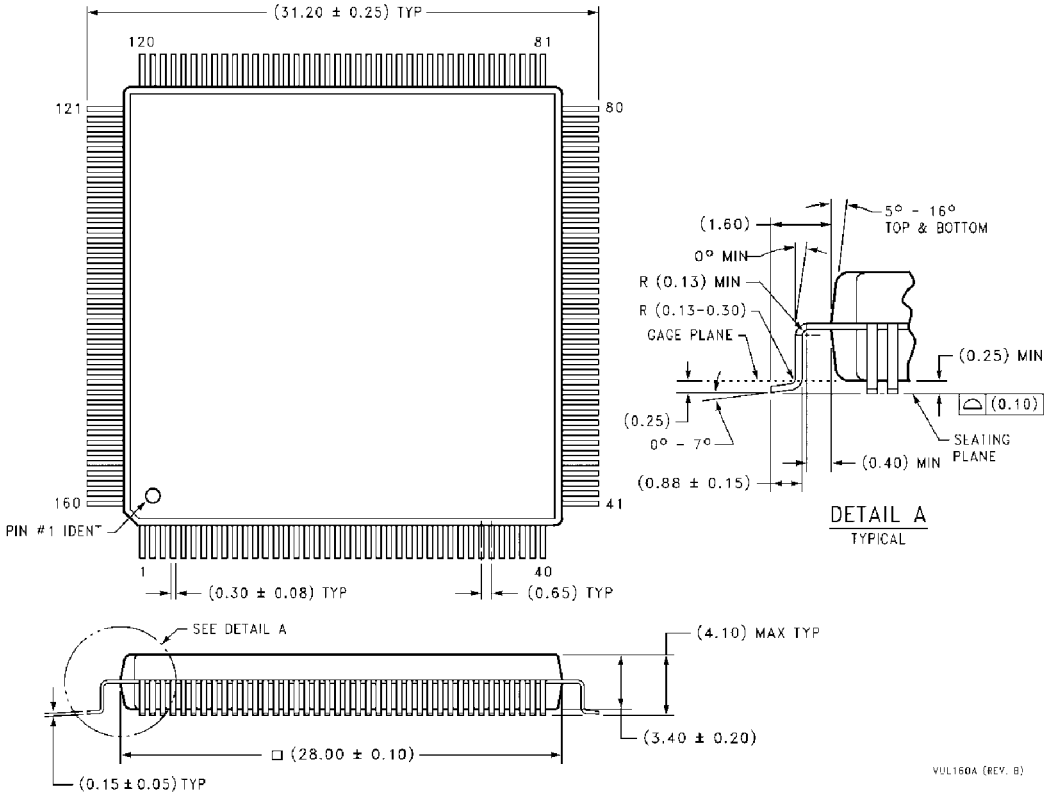


Figure 2: 160-pin EIAJ PQFP mechanical details



Unit of Measurement = millimeters

3.0 DC Specifications

The DC specifications for the PCI bus signals match exactly those given in the PCI Specification, Rev. 2.1, Section 4.2.1.1. For more information on the PCI DC specifications, see the PCI Specification.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	-0.3 to +7	V
V_{IN}	DC input voltage	-0.3 to V_{CC}+0.3	V
I_{IN}	DC input current	± 10	mA
Tj	Junction temperature	125	°C
T_{STG}	Storage temperature range	-40 to +125	°C

Table 7: Guaranteed Operating Conditions

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage 5 volt	4.50 to 5.50	V
V_{CC}	Supply voltage 3.3 volt	3.0 to 3.6	V
Theta Ja	Thermal resistance	50	°C/w
T_A	Ambient temperature range	-40 to 85	°C

3.1 PCI Bus DC Specifications

Table 8: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{IH}	Input high voltage		2.0	V_{CC}+0.5	V	
V_{IL}	Input low voltage		-0.5	0.8	V	
I_{IH}	Input high leakage current	V_{IN} = 2.7V		70	µA	1
I_{IL}	Input low leakage current	V_{IN} = 0.5V		-70	µA	1
V_{OH}	Output high voltage	I_{OUT} = -2mA	2.4		V	
V_{OL}	Output low voltage	I_{OUT} = 3mA, 6mA		0.55	V	2
C_{IN}	Input pin capacitance			10	pF	3

Table 8: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
C_{CLK}	PCLK pin capacitance		5	12	pF	
C_{IDSEL}	IDSEL pin capacitance			8	pF	4
L_{PIN}	Pin inductance			20	nH	

Notes:
1. Input leakage currents include high impedance output leakage for all bi-directional buffers with tri-state outputs.
2. Signals without pull-up resistors have greater than 3mA low output current. Signals requiring pull resistors have greater than 6mA output current. The latter include FRAME, TRDY, IRDY, STOP, SERR, PERR.
3. Absolute maximum pin capacitance for a PCI unit is 10pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

3.2 Local Bus DC Specifications

Table 9: Local Bus Signals DC Operating Specifications for Vcc = 5 volt

Symbol	Description	Conditions	Min	Max	Units
V_{IL}	Low level input voltage	V_{CC} = 4.75V		0.8	V
V_{IH}	High level input voltage	V_{CC} = 5.25V	2.0		V
I_{IL}	Low level input current	V_{IN}=GND, V_{CC}=5.25V	-10		µA
I_{IH}	High level input current	V_{IN} = V_{CC} = 5.25V		10	µA
V_{OL4}	Low level output voltage for 4 mA outputs and I/O pins	I_{OL} = -4 mA		0.4	V
V_{OH4}	High level output voltage for 4 mA outputs and I/O pins	I_{OH} = 4 mA	2.4		V
I_{OZL}	Low level float input leakage	V_{IN} = GND	-10		µA
I_{OZH}	High level float input leakage	V_{IN} = V_{CC}		10	µA
I_{CC} (max)	Maximum supply current	V_{CC} = 5.25V PCLK = LCLK = 33MHz		150	mA
I_{CC} (typ)	Typical supply current	V_{CC} = 5.0V PCLK = LCLK = 33MHz		120	mA
C_{IO}	Input and output capacitance			10	pF

Table 10: Local Bus Signals DC Operating Specifications for Vcc = 3.3 Volt

Symbol	Description	Conditions	Min	Max	Units
V_{IL}	Low level input voltage	V_{CC} = 3.0V		0.8	V
V_{IH}	High level input voltage	V_{CC} = 3.6V	2.1		V
I_{IL}	Low level input current	V_{IN}=GND, V_{CC}=3.6V	-10		µA
I_{IH}	High level input current	V_{IN} = V_{CC} = 3.6V		10	µA
V_{OL4}	Low level output voltage for 4 mA outputs and I/O pins	I_{OL} = -4 mA		0.4	V
V_{OH4}	High level output voltage for 4 mA outputs and I/O pins	I_{OH} = 4 mA	2.4		V
I_{OZL}	Low level float input leakage	V_{IN} = GND	-10		µA
I_{OZH}	High level float input leakage	V_{IN} = V_{CC}		10	µA
I_{CC} (max)	Maximum supply current	V_{CC} = 3.6V PCLK = LCLK = 33MHz		95	mA
I_{CC} (typ)	Typical supply current	V_{CC} = 3.3V PCLK = LCLK = 33MHz		80	mA
C_{IO}	Input and output capacitance			10	pF

4.0 AC Specifications

The AC specifications for the PCI bus signals match exactly those given in the PCI Specification, Rev. 2.1, Section 4.2.1.2. For more information on the PCI AC specifications, including the V/I curves for 5V signalling, see section 4.2.1.2 of Rev 2.1 PCI Specification.

4.1 PCI Bus Timings

Table 11: PCI Bus Signals AC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
$I_{OH(AC)}$	Switching current high	$0V<V_{OUT}\leq1.4V$	-44		mA	1
		$1.4V<V_{OUT}<2.4V$	$-44+(V_{OUT}-1.4)/0.024$	Equation A	mA	1, 2, 3
	(Test point)	$V_{OUT}=3.1V$		-142	mA	3
$I_{OL(AC)}$	Switching current low	$V_{OUT}\geq2.2V$	95		mA	1
		$2.2V>V_{OUT}>0.55$	$V_{OUT}/0.023$	Equation B	mA	1, 3
	(Test point)	$V_{OUT}=0.71$		206	mA	3
I_{CL}	Low clamp current	$-5<V_{IN}\leq-1$	$-25+(V_{IN}+1)/0.015$		mA	
t_R	Unloaded output rise time	0.4V to 2.4V	1	5	V/ns	4
t_F	Unloaded output fall time	2.4V to 0.4V	1	5	V/ns	4

Notes:
1. Refer to the V/I curves in Section 4.2.1 of the PCI Specification. This specification does not apply to CLK and RST which are system outputs. "Switching Current High" specifications are not relevant to open drain outputs such as SERR and INTA-INTD.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as it does in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements are met as drivers pull beyond the first step voltage (AC drive point). Equations defining these maximums (A and B) are provided with the respective V/I curves given in the PCI Spec. The equation defined maxima is met by design.
4. The minimum slew rate (slowest signal edge) is met by the PCI drivers. The maximum slew rate (fastest signal edge) is a guideline. Motherboard designers must bear in mind that rise and fall times faster than this maximum guideline could occur, and should ensure that signal integrity modeling accounts for this.

Equation A: $I_{OH} = 11.9\cdot(V_{OUT} - 5.25V)\cdot(V_{OUT} + 2.45V)$ for $V_{CC} > V_{OUT} > 3.1V$

Equation B: $I_{OL} = 78.5\cdot V_{OUT}(4.4V - V_{OUT})$ for $0V < V_{OUT} < 0.71V$

4.2 Local Bus Timings

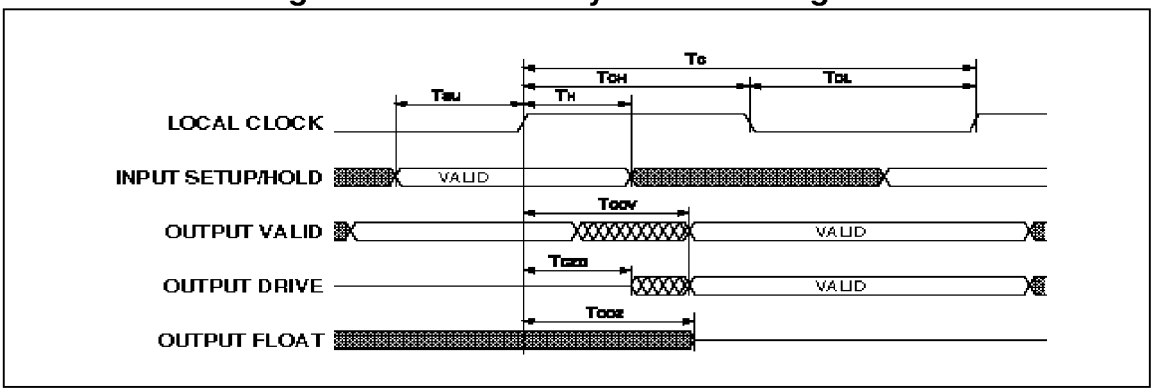
Table 12: Local Bus AC Test Conditions

Symbol	Parameter	Limits	Units
V_{CC}	Supply voltage 5 volt operation	4.50 to 5.50	V
V_{CC}	Supply voltage 3.3 volt operation	3.0 to 3.60	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 13: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Supply voltage	Derating
4mA	5 volt	0.058 ns/pF for loads > 50pF
4mA	3.3 volt	0.099 ns/pF for loads > 50pF

Figure 3: Clock and Synchronous Signals



Notes:

Table 14: Local Bus Timing Parameters for Vcc = 5 Volts +/- 5%

				33MHz		50MHz		
#	Symbol	Description	Notes	Min	Max	Min	Max	Units
1	T_C	LCLK/MEMCLK period		30		20		ns
2	T_{CH}	LCLK/MEMCLK high time	1	12		9		ns
3	T_{CL}	LCLK/MEMCLK low time	1	12		9		ns
4	T_{SU}	Synchronous input setup	2	7		6		ns
4a	T_{SU}	Synchronous input setup (BLAST,BTERM)/(BURST, ERR)		8		7		ns
4b	T_{SU}	Synchronous input setup (ADS/LREQ)		6		5		ns
4c	T_{SU}	Synchronous input setup (address, data, byte enables)		8		6		ns
4d	T_{SU}	Synchronous input setup for read data when in local bus master mode		5		5		ns
4e	T_{SU}	Synchronous input setup for (READY, W/R, HOLDA)/(RDY, R/W, LBGRT)		5		4		
5	T_H	Synchronous input hold			2		2	ns
6	T_{COV}	LCLK/MEMCLK to output valid delay	3	3	14	3	10	ns
6a	T_{COV}	LCLK/MEMCLK to output valid delay (address, data, byte enable, parity)		3	15	3	12	ns
7	T_{CZO}	LCLK to output driving delay		3	15	3	12	ns
8	T_{COZ}	LCLK/MEMCLK to high impedance delay	4	3	15	3	12	ns
9	T_{RST}	Reset period when LRST used as input		$16 \cdot T_C$		$16 \cdot T_C$		ns

1. Measured at 1.5V.
2. All local bus signals except those in 4a, 4b, 4c, 4d and 4e.
3. All local bus signals except those in 6a.
4. READY, BLAST, ADS are driven to high impedance at the falling edge of LCLK.

Table 15: Local Bus Timing Parameters for Vcc = 3.3 Volts +/- 5%

				33MHz		
#	Symbol	Description	Notes	Min	Max	Units
1	T_C	LCLK/MEMCLK period		30		ns
2	T_{CH}	LCLK/MEMCLK high time	1	12		ns
3	T_{CL}	LCLK/MEMCLK low time	1	12		ns
4	T_{SU}	Synchronous input setup	2	8		ns
4a	T_{SU}	Synchronous input setup ($\overline{BLAST}$,$\overline{BTERM}$)/($\overline{BURST}$, $\overline{ERR}$)		9		ns
4b	T_{SU}	Synchronous input setup ($\overline{ADS}$/$\overline{LREQ}$)		7		ns
4c	T_{SU}	Synchronous input setup (address, data, byte enables)		8		ns
4d	T_{SU}	Synchronous input setup for read data when in local bus master mode		7		ns
4e	T_{SU}	Synchronous input setup for ($\overline{READY}$, W/$\overline{R}$, HOLDA)/($\overline{RDY}$, R/$\overline{W}$, $\overline{LBGRT}$)		5		
5	T_H	Synchronous input hold			3	ns
6	T_{COV}	LCLK/MEMCLK to output valid delay	3	4	14	ns
6a	T_{COV}	LCLK/MEMCLK to output valid delay (address, data, byte enable, parity)		4	16	ns
7	T_{CZO}	LCLK to output driving delay		4	16	ns
8	T_{COZ}	LCLK/MEMCLK to high impedance delay	4	4	16	ns
9	T_{RST}	Reset period when LRST used as input		$16 \cdot T_C$		ns

Table 16: PCI Bus Timing Parameters for Vcc = 5 or 3.3 Volts +/- 10%

#	Symbol	Description	Notes	Min	Max	Units
1	T_C	PCLK period		30		ns
2	T_{SU}	Synchronous input setup to PCLK	1	7		ns
2a	T_{SU}	Synchronous input setup to PCLK ($\overline{GNT}$)		10		ns
3	T_H	Synchronous input hold from PCLK		0		ns
4	T_{COV}	PCLK to output valid delay	2	3	11	ns

Table 16: PCI Bus Timing Parameters for Vcc = 5 or 3.3 Volts +/- 10%

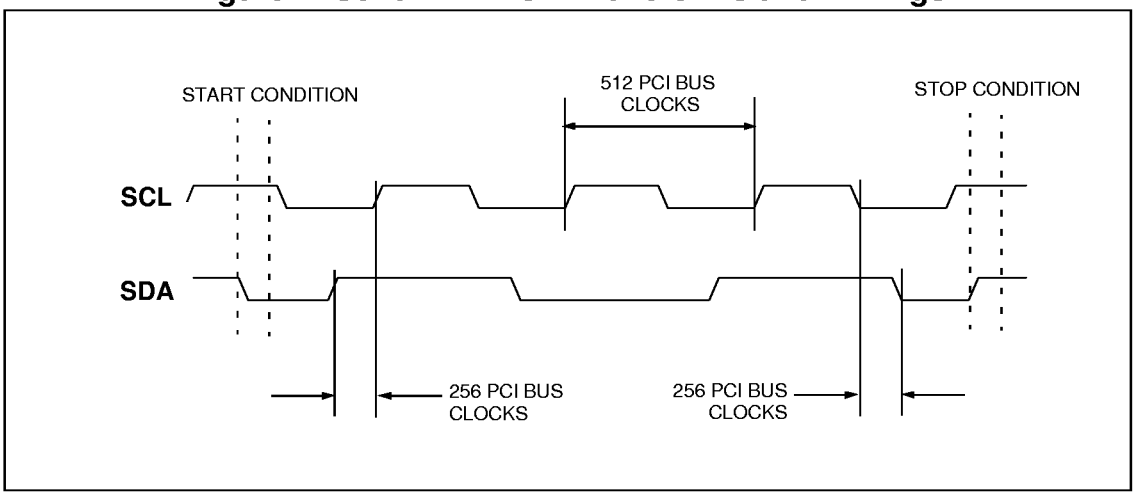
4a	T_{COV}	PCLK to output valid delay ($\overline{REQ}$)		4	12	ns
5	T_{CZO}	PCLK to output driving delay		4	11	ns
6	T_{COZ}	PCLK to high impedance delay		5	18	ns
7	T_{RST}	Reset period when PRST used as input		$16 \cdot T_C$		

Notes:
1. All PCI bus signals except those in 2a.
2. All PCI bus signals except those in 4a.

4.3 Serial EEPROM Port TImings

The clock for the serial EEPROM interface is derived by dividing the PCI bus clock. The waveforms generated are shown in Figure 4.

Figure 4: Serial EEPROM Waveforms and Timings



5.0 Revision History

Table 17: Revision History

Revision Number	Date	Comments and Changes
1.1	5/98	Addition of 3.3 volt information.
1.0	8/97	First pre-silicon revision of preliminary data sheet.

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