VTC Inc.
Value the Customer™

VM214

4-CHANNEL, THIN-FILM HEAD READ/WRITE PREAMPLIFIER

July, 1992

FEATURES

- For Use with Non Center-Tapped Thin-Film Heads
- Supports Four Read / Write Heads Per Circuit
- Complete Fault Detect Capability
- On-Chip Current Source, Externally Adjusted
- TTL-Compatible Control Signals
- Very Low Input Noise
- High Gain

DESCRIPTION

The VM214 is an integrated read/write preamplifier designed for use with non center-tapped thin-film heads. Each circuit controls four heads and has three modes of operation: read, write, and idle. The circuit functions as a low-noise differential amplifier in the read mode and as a differential current switch in the write mode. Write current is supplied by an internal current source. The magnitude of the write-current to the heads is determined by an external resistor. The VM214 operates on +5V and -5V and is available in 24-lead flatpack and SOIC packages.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{CC} 6V
- V_{EE} ..... -6V

Input Voltages:
- Head Select (HS1, HS2) ..... to V_{CC} + 0.3V
- Chip Select (CS) ..... -0.4V to V_{CC} + 0.3V
- Read/Write Select (R/W) ..... -0.4V to V_{CC} + 0.3V
- Write Data (WD) ..... $-V_{EE}$ to 0.3V
- Read Inputs, Read Mode (+HDN) ..... -0.6V to 0.4V

Output Levels:
- Read Data (+RD) ..... V_{CC} - 2.5V to V_{CC} + 0.3V
- Write OK (WOK) ..... -0.4V to V_{CC} + 0.3V and 20mA
- Write Select Verifty (WSV) ... -0.4V to V_{CC} + 0.3V and 20mA
- Current Monitor (IMF) ..... 0.4V to V_{CC} + 0.3V
- Current Reference (R_{EXT}) ..... $-V_{EE}$ to V_{CC} + 0.3V and 8mA
- Head Outputs, Write Mode (±HDN) ..... IW max. = 150mA

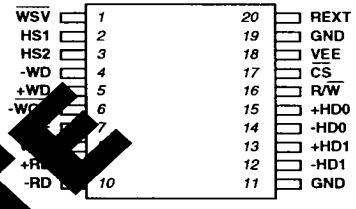
Storage Temperature Range ..... -65° to 150°C
Lead Temperature (Soldering 60 Sec.) ..... 300°C
Operating Temperature ..... 70°C
Junction Temperature ..... 150°C
Thermal Characteristics Θ_{JA}:
- 20-lead SOIC ..... 80°C/W
- 24-lead SOIC ..... 80°C/W
- 24-lead Flatpack ..... 110°C/W

RECOMMENDED OPERATING CONDITIONS

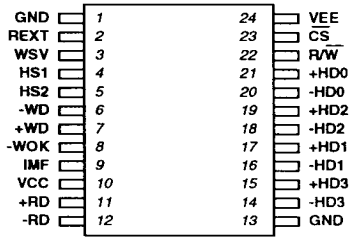
DC Power Supply Voltage:
- V_{CC} ..... 5V ± 5%

Negative Supply Voltage (V_{EE}) ..... -5V ± 5%
Head Load (L_H) ..... 150 - 600µH
Junction Temperature ..... 25° to +125°C

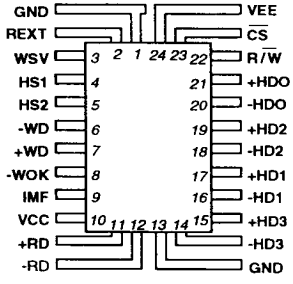
CONNECTION DIAGRAM



2-Channel
20-lead SOIC
VM2142POP

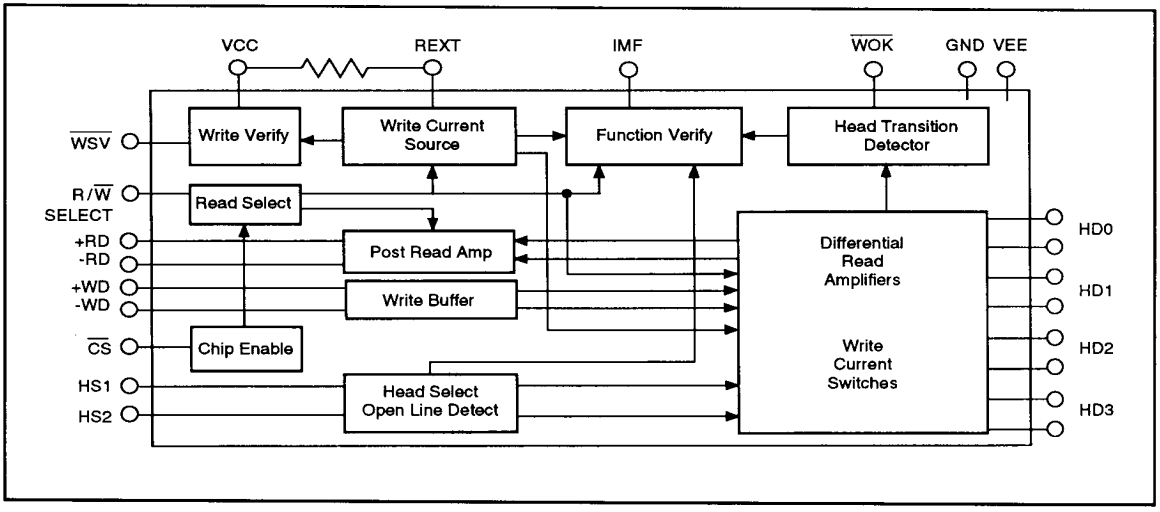


4-Channel
24-lead SOIC
VM2144POP



4-Channel
24-lead Flatpack
VM214FP

BLOCK DIAGRAM



CIRCUIT OPERATION

The VM214 has four channels of read amplifiers and write drivers plus an internal write current source. The write current magnitude is determined by an external resistor (R_{EXT}) connected between pins R_{EXT} and V_{CC}. The VM214 has the following TTL-compatible control lines:

1. The chip select ($\overline{CS}$) input selects the active or the idle mode. The idle mode allows circuits to be multiplexed.
2. If the chip is active (enabled), the read/write select (R/W) input is used to select the read or write modes.
3. The head select inputs (HS1, HS2) select one of the four channels for a read or write operation.

The write data (±WD) input voltage range includes the ECL levels. The read (±RD) outputs are open collector, requiring external 100Ω (R_L) load resistors connected to V_{CC}.

Write Mode

In the write mode, the VM214 functions as a differential current switch channeling the write current to the selected head determined by HS1 and HS2. The write data inputs (±WD) determine the polarity of the head current. The write current is supplied by an internal current source and the magnitude is determined by the value of an external resistor connected between V_{CC} and the R_{EXT} pin.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier. Pins HS1 and HS2 determine which differential input channel is selected and applied to the amplifier. The amplifier output is read differentially at the read data (±RD) pins.

Fault Detection

The chip contains fault detection circuits. A high level at an enabled chip's write OK ($\overline{WOK}$) output is caused by the following write fault conditions:

1. Chip not enabled
2. Open head
3. Non-switching write data (±WD)
4. No write current (can be in read mode)
5. Open head select inputs (HS1, HS2)
6. Head shorted to ground
7. Write frequency is outside of limits
8. Chip in read mode

When a chip is enabled the IMF current monitor provides a 3mA output. This feature allows single or multichip enabled conditions to be detected.

An open collector output, write select verify ($\overline{WSV}$), goes low when the chip has write current present.

PIN DESCRIPTIONS

Read Data Outputs

Read data outputs (±RD) consist of a pair of differential lines used to pass the amplified read signal (30 to 100mVp-p signals-typical) to the disk drive electronics. External 100Ω load resistors tied to V_{CC} are required.

Write Data Inputs

Write data inputs (±WD) consist of a pair of differential lines used to write high frequency data patterns onto the disk via the selected R/W head and chip. Input data levels can either be driven directly from ECL level drivers with proper termination resistances or from open collector current drivers terminated into 100Ω resistors to ground.

Chip Select Input ($\overline{CS}$)

Chip select input (CS) is a TTL-compatible input line used to enable or disable the VM214. The chip enable input requires an open collector TTL-compatible drive source. A logic low enables the chip, while a logic high or open cable disables the chip by putting it into an idle state.

Read/Write Select Input (R/$\overline{W}$)

The read/write select input (R/W) is a TTL-compatible input line used to select either the read or write mode of operation when the chip has been enabled ($\overline{CS}$ = 0V). A logic high state or open cable selects the read mode of operation while low state selects the write mode of operation.

Write Select Verify Output (WSV)

The write select verify (WSV) output is an open-collector, TTL-compatible output that is used to verify that write current is present. The output is terminated into a user-determined resistor to +5V. A logic low state indicates that write current is present.

Current Monitor Output (IMF)

The current monitor (IMF) output is an open-collector current output that is used to indicate the chip is in the active or enabled mode. Output is terminated into a user-determined resistance to +5V.

Nominal "safe" current is 3mA for one chip enabled. If the IMF current falls below 2mA, a "no function" error is detected in the drive electronics indicating the chip selected has not been enabled or the chip is defective. If more than 4mA is detected a "multi-function" error is generated in the disk drive electronics. This indicates that more than one chip has been activated, the chip selected is defective or the IMF line is shorted to ground or negative voltage.

Write OK Output ($\overline{WOK}$)

The write OK (WOK) output is an open-collector, TTL-Compatible output that is used to indicate an open head, no write data, no write-current or open head select (HS1, HS2) condition exists. The WOK output is terminated into a user-determined resistor to +5V. A logic low indicates a "safe" condition while a logic high indicates a "fault" condition.

Head Select Inputs (HS1, HS2)

The head select inputs (HS1,HS2) are bussed TTL-Compatible logic control signals used to select one of four R/W channels on a selected chip (0.8V). An open HS1 or HS2 input will give a fault indication to the disk drive electronics via write OK (WOK).

Table 1: Head Select

HS2	*HS1*	*HEAD*
L	L	0
L	H	1
H	L	2
H	H	3

Table 2: Mode Select

$\overline{CS}$	*R/$\overline{W}$*	*MODE*
L	L	Write
L	H	Read
H	L	Idle
H	H	Idle

Table 3: External Resistor vs. Write Current

External resistor vs. DC write current I_W into the selected head terminal X or Y with V_{CT} shorted only to the respective X or Y terminal.

1% External Resistor R_{WC} (Ω)	Write Current I_W (mA)
6.9	10
4.0	20
2.7	30
2.0	40
1.6	50

DC CHARACTERISTICS Unless otherwise specified, V_{CC} = 5 ± 0.01V, V_{EE} = -5V ±0.01V, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Positive Supply Current I_W = 40mA	I_{CC}	Read			56	mA
		Write			50	mA
		Idle			12	mA
Negative Supply Current I_W = 40mA	I_{EE}	Read			-85	mA
		Write			-165	mA
		Idle			-15	mA
Power Dissipation I_W = 40mA	P_D	Read			670	mW
		Write			1.05	W
		Idle			140	mW
Digital TTL Inputs (CS, R/W, HS1, HS2)	V_H	High Voltage	2	3.5	4	V
	V_L	Low Voltage		0.2	0.8	V
Digital ECL Inputs (±WD)	V_H	High Voltage			-0.6	V
	V_L	Low Voltage			-1.5	V
Chip Select Current	I_{CSH}	High; V_{CSH} = 4V			-0.3	mA
	I_{CSL}	Low; V_{CSL} = 0.4V			-1.4	mA
R/W Select Current	I_{RSH}	High; $V_{R/\overline{WH}}$ = 4V (RM)			-15	µA
	I_{RSL}	Low; $V_{R/\overline{WL}}$ = 0.4V (WM)			-200	µA
Head Select Current (HS1, HS2)	I_{HSH}	High; V_{HSH} = 4V			250	µA
	I_{HSL}	Low; V_{HSL} = 0.4V			250	µA

FAULT DETECTION CHARACTERISTICS Unless otherwise specified, V_{CC} = 5 ± 0.01V, V_{EE} = -5V ±0.01V, T_A = 25°C.

PARAMETER		*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Select Verify Voltage	High (Unsafe)	V_{WSVH}	I_W = 80mAp-p, $\overline{CS}$ = V_{CSL}, R/W = $V_{R/\overline{WL}}$, R_L = 750Ω min.	4.9			V
	Low (Safe)	V_{WSVL}				400	mV
Write OK Voltage	High (Unsafe)	V_{WOKH}	$\overline{CS}$ = V_{CSL}, R/$\overline{W}$ = $V_{R/\overline{WL}}$, min. R_L = 750Ω min.	4.9			V
	Low (Safe)	V_{WOKL}				400	mV
IMF Current Chip Enable (ON)		I_{IMF}	$\overline{CS}$ = V_{CSL}, read or write mode, R_L = 1KΩ to 5V	-2.2		3.7	mA
IMF Voltage Chip Disable (OFF)		V_{IMF}	$\overline{CS}$ = V_{CSL}, R_L = 1KΩ to 5V	4.9			V
Write Select Verfiy Delay Time							
Read to Write Mode (ON)		t_{WSON}	$\overline{CS}$ = V_{CSL}			600	ns
Write to Read Mode (OFF)		t_{WSOFF}					

READ CHARACTERISTICS Unless otherwise specified, V_{CC} = 5 ± 0.01V, V_{EE} = -5V ±0.01V, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	R_L = 100Ω each side to V_{CC}, f = 1MHz, Input V_{IN} = 1mVrms	100		150	V/V
Bandwidth	BW	R_L = 100Ω each side. Zs = 2.4Ω, V_{IN} = 1mVrms, $f_{MIDBAND}$ = 300KHz				MHz
-3 dB			35		100	
-1 dB			15			
Input Noise Voltage	e_{in}	V_{IN} = 0V, PWR BW = 17MHz, R_L = 100Ω each side.			1.1	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 0V, f = 5MHz			65	pF
Differential Input Resistance	R_{IN}	V_{IN} = 0V	1330		2470	Ω
Voltage Gain Linearity	A_{VL}	AC input voltage where the gain is 90% of the gain with 0.2mVrms Input, f = 1MHz, R_L = 100Ω each side to V_{CC}.			± 2	mV
Common Mode Rejection Ratio	CMRR	CMPR = 20 · log (A_V/ [V_O /V_{CM}])				dB
1MHz ≤ f ≤ 10MHz		V_{CM} = 100mVp-p	50			
f = 20MHz		Input Referred	46			
Power Supply Rejection Ratio	PSRR	V_{IN} = V_{EE} + 100mVp-p OR V_{CC} + 100mVp-p PSRR = 20 · log (A_V/ [V_{OUT}/V_{IN}])				dB
f = 1MHz			65			
f = 20MHz			40			
Channel Separation (Read Crosstalk)	CS	Selected Head V_{IN} = 0V Unselected Heads V_{IN} = 20mVp-p				dB
1MHz ≤ f ≤ 10MHz			46			
f = 20MHz			40			
Output Offset Voltage	V_{OS}	R_L = 100Ω each side to V_{CC}	-360		360	mV
Common Mode Output Voltage	V_{OCM}	R_L = 100Ω each side to V_{CC}	V_{CC} – 0.9		V_{CC} – 0.3	V
Output Leakage Current (Idle Mode)	I_{OL}				10	µA

WRITE CHARACTERISTICS Unless otherwise specified, I_W = 40mA, L_H = 2.5µH, R_D = 750Ω, f_{DATA} = 5MHz, C_L (RDX, RDY) ≤ 20pF, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W		10		50	mA
Current Tolerance	I_{WT}	Current set to nominal value by external 1% resistor (R_{EXT}), R_H = 20Ω ± 1%	-8		8	%
Head Differential Load Resistance	R_{DL}		1330		2470	Ω
Head Differential Load Capacitance	C_{DL}				10	pF
Head Current Rise Time	t_r	I_W = 40mA, L_H = 150nH, R_H = 20Ω, Measure t_r 10% to 90% of transition, Measure t_f 90% to 10% of transition			16	ns
Head Current Fall Time	t_f					
Current Gain	A_I			20		mA/mA
Head Current Switching Delay	t_{HC}	I_W = 40mA, L_H = 150nH, R_H = 20Ω, Measured from 50% of write data to 50% transition of write current (I_W)			18	ns
Head Current Switching Delay Difference		f = 3MHz (Write Data)			1	ns
Write Crosstalk (Unselected Head Current	W_{XT}	I_W = 40mA, L_H = 150nH, R_H = 20Ω maximum. Measured unselected channels while driving selected channels			2	mA peak
Head Current Switching Time-Symmetry	t_{SYM}	V_{WDD} = 200mV, I_W = 40mA L_H = 150nH, R_H = 20Ω max. ±WD transition = 2ns ±WD symmetry = 0.2ns			1.5	ns
Differential Data Voltage	V_{WDD}		200			mV
Write Data Input Voltage Range	V_{WD}		-2.5		0.1	V
Data Input Current (per side)	I_{WD}	$\overline{CS}$ = V_L = 0V			150	µA
Write Current Overshoot B/A	I_{WOS}	I_W = 40mA, L_H = 150nH, R_H = 20Ω			20	%

SWITCHING CHARACTERISTICS Unless otherwise specified, I_W = 40mA, L_H = 2.5µH, R_D = 750Ω, f_{DATA} = 5MHz, C_L (RDX, RDY) ≤ 20pF, T_A = 25°C.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Chip Select Delay		Measure delay to 90% of 5MHz. Read Output or Write Current				
Idle to Write	t_{IW}				1	µs
Idle to Read	t_{IR}				600	ns
Chip Select Delay		Measure delay to 10% of 5MHz. Read Output or Write Current				
Read to Idle	t_{RI}				600	ns
Write to Idle	t_{WI}				600	ns
Chip Select to ($\overline{WOK}$) Delay		Write Mode $V_{R/\overline{WH}}$ = 4V				
Chip Enabled (ON)	t_{IWI}				1.5	µs
Chip Disabled (OFF)	t_{WII}				600	ns
Chip Select to ($\overline{WOK}$) Delay						
Chip Enabled (ON)	t_2				1	µs
Chip Disabled (OFF)	t_1				2	µs
Chip Select to Write Select Verify						
Chip Enabled (ON)	W_{SVL}				600	ns
Chip Disabled (OFF)	W_{SVH}				600	ns
R/W Select to Write Current Delay						
Write Select	t_{RWW}	Measure delay to 90% of write Current. (CS = VL)			1	µs
Read Select	t_{WRW}	Measure delay to 10% of write Current. (CS = VL)			600	ns
R/W Select to Read Output Delay						
Read Select	t_{WRR}	Measure delay to 90% of 5MHz Read Output. Waveform offset shift may be positive or negative depending on Write Data Input conditions and should not be considered when taking measurement. CS = VL			600	ns
Write Select	t_{RWR}	Measure to 10% of 5MHz Read Output. CS = VL			1.5	µs
Head Select Switching Delay	t_{HS}	Measure 50% of HS to 90% Read Output or Write Current. CS = VL			1	µs
IMF Switching Time		Delay from 50% of Chip Select voltage (CS) to 50% (ON) or 50% (OFF) of final IMF voltage respectively.				
Chip Enabled (ON)	t_{IMF1}				600	ns
Chip Disabled (OFF)	t_{IMF2}				600	ns
Write OK Delay						
Unsafe to Safe Delay after Write Data (WD) Begins	t_{UN1}	f_{DATA} = 5MHz (Write Data)			600	ns
Safe to Unsafe Delay	t_{UN2}	Head opens or non-switching write data (WD) or no write current	0.6		3.6	µs
Head Select Input Opened (Safe to Unsafe Delay)	t_{UN3}				600	ns
Unsafe to Safe Read to Write	t_{UN4}	f_{DATA} = 5MHz (Write Data)			3	µs
Safe to Unsafe Write to Read	t_{UN5}	f_{DATA} = 5MHz (Write Data)			600	ns