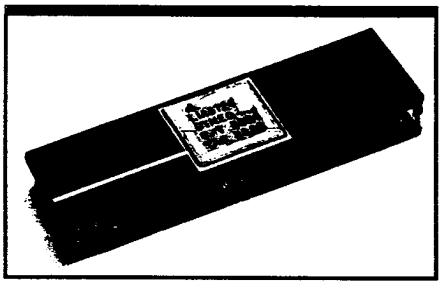
DYMEC

MODEL:

5024

24-Bit Programmable Counter/Timer



Description

To implement a counter/timer function, two functional blocks are required — a counter, which counts the pulses from an incoming frequency or event source, and a timer, which controls the *time base*, or interval of time over which the counting takes place. The **5024** contains both a 24-bit counter that can accept an input pulse train (frequency) of up to 50MHz, and a timer that can be programmed to vary the length of the time base. The time base can range from hundreds of nanoseconds to tens of seconds, with specific time values depending upon the frequency of a *timing reference*. The timing reference for the counter/timer may be either a timing signal from the system itself, or a dedicated crystal used with the crystal oscillator circuitry built-in to the **5024**.

The first major problem solved by the **5024** is that of high frequency operation. The **5024** is designed to operate to rated performance with input frequencies up to 50MHz on either the frequency and/or the timing reference inputs. This means that systems currently using a counter/timer function can dramatically improve their counter resolution, *without* having to pay a penalty in board real estate or parts count, which would be the case if the designer had to resort to a discrete

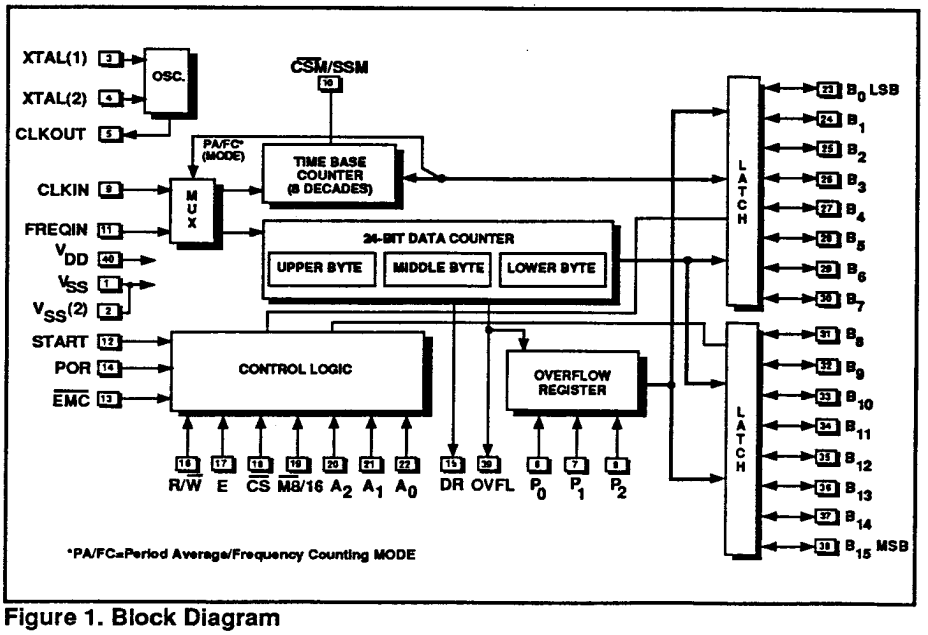


Figure 1. Block Diagram

FEATURES

- ❒ **24-Bit Resolution**
- ❒ **Microprocessor-compatible**
- ❒ **No Missing Counts Between Counting Intervals**
- ❒ **1Hz to 50MHz Input Frequency**
- ❒ **Up to 50MHz Time Base(Clock) Input**
- ❒ **Programmable Time Base**
- ❒ **8- or 16-bit Data Bus**
- ❒ **Dual Measurement Techniques**
  Frequency counting or period averaging
- ❒ **Dual Operating Modes**
  Continuous or Single Counting
- ❒ **Overflow and Data Ready Flags**
- ❒ **Power-On-Reset**

APPLICATIONS

- ❒ **Wide Dynamic Range A/D Converters**
  Analytical Instrumentation
  Seismic Data Acquisition
  Biomedical Data Acquisition
- ❒ **Frequency Meters**
- ❒ **Period Averaging Counters**
- ❒ **General Purpose Counter/Timer**

Description (Continued)

design to get the higher operating frequency.

The second major problem the **5024** solves is the problem of missing counts during the interval when the output data from one counting interval is being transferred to the output registers, and the next counting interval is started. Most counter/timer ICs will miss counts on their inputs while this latching operation is happening. This can be a significant problem to overcome if the counter/timer is used with a voltage-to-frequency converter as part of an A/D conversion subsystem. Those missed pulses represent important data in these systems. The **5024** has unique architecture that captures any incoming pulses during the transfer, and is guaranteed by design not to miss a single pulse during this interval, even at 50MHz! This is achieved *without* external synchronizing or other circuitry.

The third major problem addressed by the **5024**, again in systems using V/F converters with the counter/timer as an A/D function, is resolution for both low and high level signals. Frequency counting techniques allow for high resolution data for input voltages above, say, one-tenth of full scale, because the V/F is outputting a large number of pulses during a fixed "conversion time" or counting interval. As input voltages fall from there to very low levels, resolution decreases, because the V/F is outputting fewer and fewer pulses to count over the same interval. Yet quite often, data at these low signal levels is critical, and having the same resolution at the low end, as is available at the high end of the input range, is also critical. In these instances, period averaging techniques are used. Period averaging provides high resolution for small signal inputs because a high frequency clock is counted over an interval of time (a user-defined number of V/F output periods) that is controlled, ultimately by the low level signal to be converted. Because the output data, which is proportional to the low level input signal, is the result of counting a very high frequency, it contains a large number of bits, which means it there-

Specifications

All Specifications Guaranteed at 25°C Unless Otherwise Noted

Absolute Maximum Ratings

DC Supply Voltage V_{DD} - V_{SS}	+5V, ±5%
Operating Temperature	0°C to +70°C
Storage Temperature	-25°C to +100°C

D.C. Electrical Operating Characteristics: T_A = 0°C to +70°C; V_{DD} = +5V (±5%); V_{SS} = 0V unless otherwise noted

Symbol	Parameter/Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High Level Logic Input	3.15		V_{DD}	V
V_{IL}	Low Level Logic Input	V_{SS}		+0.8	V
V_{OH}	High Level Logic Outputs	3.9		V_{DD}	V
V_{OL}	Low Level Logic Outputs	0		+0.4	V
P_O	Power Dissipation @ +5.25V, and 50MHz clock frequency			700	mW

AC Electrical Characteristics V_{DD} = 5V±5%, all temperature ranges

R/$\overline{W}$	Read cycle time	50			ns
	Write cycle time	50			ns
A_0, A_1, A_2	Byte select set up time	10			ns
E	Enable set up time	10			ns
	Enable hold time	10			ns
$\overline{CS}$	Chip select set up time	10			ns
	Chip select hold time	10			ns
D_7-D_0	Program Code set up time	10			ns
	Program Code hold time	10			ns
FREQIN	Frequency Input			50	MHz
CLKIN	Clock Input		10	50	MHz

Description (Continued)

fore provides high resolution data. The 5024 allows switching between these operating modes "*on-the-fly*" by changing only one control line.

The **5024** also has operating modes that allow it to count either for a single counting interval and stop, or, can repeatedly count the incoming pulses for the programmed interval, latch the resultant data, and start counting for another interval. In either case, a *data ready* signal is generated by the **5024** at the end of each counting interval. The operation of the **5024** is controlled in a synchronous manner, where counting starts at a given point in time relative to the command to start, and is completely repeatable.

The **5024** is designed to make interfacing with a microprocessor as simple as possible. Counter data from the **5024** is accessed by the microprocessor and can be placed on its data bus in either 8-bit bytes or 16-bit words. Programming of the time base counting interval is accomplished by writing a single 8-bit byte into the **5024** in the same manner as a memory location would be addressed.

The **5024** is packaged as a standard 40-pin DIL IC. Plastic packaged units are standard, but ceramic packaging is available as an option.

Pin Description

Please refer to *Figure 2* for the location of each pin.

Pin 1/2 V_{ss} (Ground) — Provides ground for the **5024**. Must be grounded for **5024** to function.

Pins 3/4 XTAL(1)/XTAL(2) — Completes the internal oscillator circuitry. Two capacitors and a resistor are required with the crystal to determine the operating frequency. (See *Figure 3.*)

Pin 5 CLKOUT — This is the output of the crystal oscillator circuit. It is normally connected to the **CLKIN** pin 9.

Pin 6,7 & 8 P_0, P_1 & P_2 — These three inputs are user defined. Whatever data is connected to these three inputs appears on the data bus when reading the overflow byte.

Pin 9 CLKIN — This is a TTL/CMOS compatible frequency input. In a frequency counting mode, this input provides the clock to the time base counter. In a period averaging mode, this input provides the clock to the data counter section of the counter/timer. For the most accurate time base, tie the **CLKOUT** (pin 5) to the **CLKIN** (pin 9).

Pin 10 $\overline{\text{CSM}}$/SSM — This pin controls the mode of operation of the counter/timer; it selects between the continuous counting (logical 0) and synchronous start (logical 1) modes.

Pin 11 FREQIN — This is a TTL/CMOS compatible frequency input. In the frequency counting mode, this input provides the clock to the data accumulators. In a period averaging mode, this input provides the clock to the period counter.

Pin 12 START — This pin provides the control of the initial start of any counting/timing interval. **START** is positive edge-triggered.

Pin 13 $\overline{\text{EMC}}$ — External Master Clear provides a master reset function. When applied, i.e. a logical "0" on the pin, all operations are stopped and all counters and latches are reset to zero. A minimum pulse width of 100ns at logical "0" is required.

Pin 14 POR — This is the **Power-On-Reset** function pin. It provides a full reset upon power-up. If POR is not used, it should be tied low.

Pin 15 DR — Data Ready provides a logical "1" that indicates that data has been latched and is ready to be read. On **Power-On Reset** (pin 14) or **External Master Clear** (pin 13), **Data Ready** becomes active high, and remains high until either, (1) a READ operation is performed, or (2) the time base interval is completed.

Pin 16 R/$\overline{\text{W}}$ — This pin selects the read or write modes of the programming/data latches. It is used in conjunction with the **E (Enable** - pin 17) and $\overline{\text{CS}}$ (**Chip Select** - pin 18) lines. A logical "1" selects the read mode; a logical "0" selects the write mode.

Pin 17 E— Enable initiates the instructions represented by the various mode and programming signal inputs. It is a positive pulse with a minimum width of 50ns.

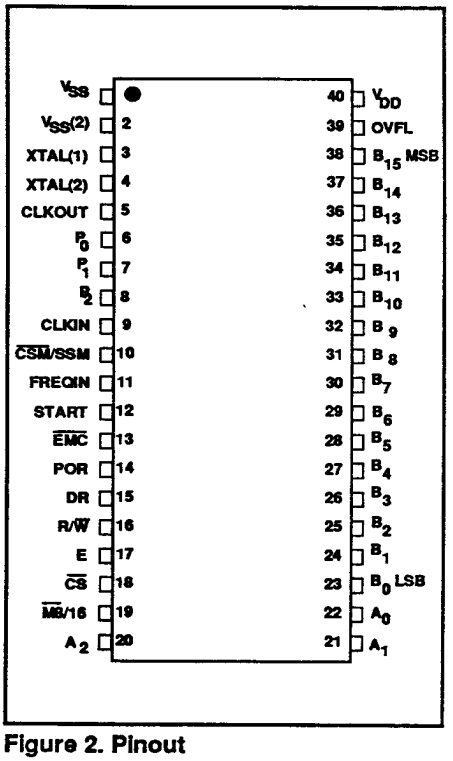


Figure 2. Pinout

Pin 18 $\overline{\text{CS}}$ — Chip Select signals the counter/timer to set up for an interface with a peripheral device. It is active low.

Pin 19 $\overline{\text{M8}}$/16 — This pin configures the output data in either an 8-bit or 16-bit wide path. A logical "0" selects an 8-bit path; logical "1" selects a 16-bit path. It is usually hard-wired for any given system in which the **5024** is used.

Pin 20,21 & 22 A_2, A_1A_0 Byte/Word Select lines — These pins are the select lines that determine which byte of output data is being read.

Pin Description (continued)

Pin 23 - 38 B_0 (LSB) - B_{15} (MSB) —Data Output Pins: These pins provide the output data from the output latches in the format selected by the $\overline{M8}$/16 control (pin 19). Output data is presented as follows in the read mode:

D_0 through D_7 (8-bit)
or
D_0 through D_{15} (16-bit)

In the write (programming) mode, programming data must appear on D_0 through D_7, regardless of output data mode.

Pin 39 OVFL — Overflow; this pin provides the overflow indicator function. When overflow of the data counter occurs, the pin will go high (logical "1") and remain high for one period of the signal on the FREQIN pin (pin 11).

Pin 40 V_{DD} — +5V power input to the 5024.

Using the 5024

General Information

The **5024** is a CMOS device. Please use suitable handling procedures and precautions. As with other high speed digital ICs, the **5024** should be decoupled. Two decoupling capacitors are recommended, one, a 1µF tantalum unit, and the other, a 0.1µF ceramic capacitor.

A **Power-On-Reset (POR)** function is included on pin 14. A minimum pulse width of 250ns is required, as is a V_{DD} =+5V. (Refer to *Figure 8.*) An increase in R will create a longer reset pulse.

A_0	A_1	A_2	COMMAND	BYTE
0	0	0	READ	LOWER
1	0	0	READ	MIDDLE
0	1	0	READ	UPPER
1	1	0	READ	OVER FLOW
1	0	1	READ	PROG. BYTE
X	X	X	WRITE	PROG. BYTE

8-BIT INTERFACE ($\overline{M8}$/16=0)

A_0	A_1	A_2	COMMAND	BYTE
0	0	0	READ	LOWER
0	1	0	READ	UPPER OVRFLO
1	0	1	READ	PROG. BYTE
X	X	X	WRITE	PROG. BYTE

16-BIT INTERFACE ($\overline{M8}$/16=1)

0=logic low; 1= logic high; X=don't care
CAUTION: Combinations of A_0, A_1, and A_2 other than those shown are invalid and will produce erroneous operation.

Table 1. Control Lines

Recommended values are 100pF for C and 3.61kΩ for R. Resistor values greater than 15kΩ are not recommended.

The **5024** is designed to be treated as a microprocessor peripheral. System software can access the various **5024** functions as an array of I/O ports, with address decoding used to supply the required control signals. These signals are defined in the section entitled **PIN DESCRIPTION**. Please refer to this section for more information.

Counter output data is 24-bits wide. It can be read as three 8-bit bytes, plus an 8-bit overflow (status) register, or, as two 16-bit words. This is controlled by the **$\overline{M8}$/16** control pin, which is usually hard-wired in any given system. Time base programming inputs are applied (written) as an 8-bit byte on the lower eight (bidirectional) data bus lines.

Reading Counter Data

Figure 4 shows the timing relationships for each of the control signals used to execute a READ operation. *Table 1* shows the relationships among the various control lines and data bytes to be read.

To read data from the **5024**, the **R/$\overline{W}$** line is in the logical "1" (high) state, and the A_2, A_1, and A_0 control lines are brought to the appropriate states for the data byte to be read, and finally the chip select line ($\overline{CS}$) is brought to a logical "0" (low). The order in which these signals are applied isn't important, as long as they are present and static for at least 10ns before the **enable** (E) line is activated, and for a minimum of 10ns after it is removed. The enable line performs the actual read operation. It is a positive pulse, at least 50ns wide. Valid data is present on the output bus 30ns maximum after the leading edge of **enable**; the data bus returns to a high impedance state 25ns maximum after the trailing edge of the enable pulse.

Programming The Time Base And Operating Mode (WRITING)

Figure 6 shows the timing relationships among the control lines during a WRITE operation. To write the programming data into the **5024**, the **R/$\overline{W}$** line is in the logical "0" (low) state. The A_2, A_1 and A_0 control lines are DON'T CARE terms during write, and are ignored. Finally the chip select line ($\overline{CS}$) is brought to a logical "0" (low); as in the read operation, $\overline{CS}$ must be pre-sent and static for at least 10ns before the **enable** (E) line is activated.

CRYSTAL FREQUENCY	C_1	R_1	C_2
2MHz	0-50pF	500	220pF
5MHz	0-50pF	180	200pF
10MHz	0-50pF	150	100pF
20MHz	0-50pF	100	80pF

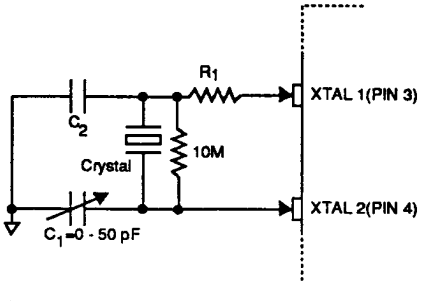


Figure 3. Crystal Inputs

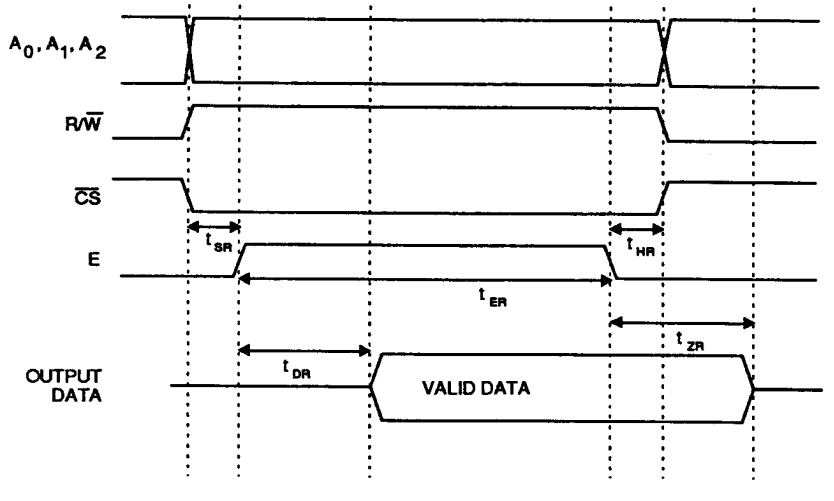
Using the 5024 (continued)

The enable line performs the actual write operation. Again, it is a positive pulse, at least 50ns wide. $\overline{CS}$ must remain static for at least 10ns after the trailing edge of the enable pulse.

The time base, or counting interval, as well as the operating mode (frequency counting or period averaging) are determined during the WRITE cycle. *Figure 7* shows the programming byte consists of 8 bits applied to the low order data lines (B_7-B_0); one bit (the MSB of the programming byte) determines whether the **5024** operates in the frequency counting mode (logical "0") or period averaging mode (logical "1"). The remaining seven bits determine the time base or counting interval. Specific values for the time base assume the use of a time-reference signal, either as a crystal at pins 3 and 4, or a system clock signal applied to pin 9. Any time-reference frequency up to 50MHz may be used, with corresponding changes in the range of actual counting intervals available. With a timing reference of 10MHz, time bases can be programmed from 100ns to 16 seconds. *Figure 7* shows the formula for determining the time base, and two examples.

System Test

This procedure provides a very fast method of testing the functionality of the **5024** installed in a microprocessor system. The test involves taking two measurements, one using the frequency counting technique, and the second using the period averaging technique, and comparing the results. A known frequency is applied to the FREQIN and CLKIN inputs of the **5024**. These can be at the same or different frequencies. The time base is programmed for a convenient interval. A measurement is taken in the frequency counting mode, and a second is made in the period averaging mode, with the same time base interval. If the counter/timer is functioning properly, the result of the frequency counting measurement should be equal to the inverse of the result of the period averaging measurement, ±1 count.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SR}	READ Set-up Time	10		ns
t_{HR}	READ Hold Time	10		ns
t_{ER}	ENABLE Pulse Width	50		ns
t_{DR}	Valid DATA Delay		30	ns
t_{ZR}	Valid DATA Hold Time		25	ns

Figure 4. READ Timing

Typical Application IBM PC/XT/AT Family Interface

The **5024** Counter/Timer design allows for straight-forward interfacing to virtually any microprocessor bus structure. The **5024** is configured to be used in a bus-command oriented interfacing scheme, rather than an interrupt-driven scheme. Figure 8 is an example of how the **5024** can be interfaced to the IBM® PC/XT/AT family of personal computers. In this example, the counter/timer is interfaced in specific I/O-mapped address spaces. Other valid I/O-mapped addresses may be substituted depending upon overall system requirements. The address spaces implemented in this example are:

ADDRESS (HEX)	FUNCTION
300	WRITE Program Byte
308	READ Lower Data Byte
309	READ Middle Data Byte
30A	READ Upper Data Byte
30B	READ Overflow/Status Byte
30D	READ Program Byte
318	READ DATA READYRegister
319	RESET EMC
31F	START

Refer to *Figure 8*. Address decoding is accomplished by placing the available address bits from the PC's I/O channel (AEN, SA_9, ... SA_4) onto the inputs of the magnitude comparator (U_2 — 74HCT688). When equality is detected, the comparator's output enables the data bus transceiver (U_1 — 74HCT245), and activates the chip select $\overline{CS}$ of the **5024**. The data buffer (U_3 — 74HCT244) provides buffering for the $\overline{IORD}$, $\overline{IOWR}$, and lower four (4) address bits. Address bit SA_3 establishes whether a READ or WRITE operation is to be performed.

Address bits SA_0, SA_1, and SA_2 determine the state of the **5024**'s A_2, A_1, and A_0 control lines. $\overline{IORD}$, $\overline{IOWR}$ determine the direction of the transceiver as well as providing the enable, E, pulse necessary for the **5024**. Using a similar scheme, the reset ($\overline{EMC}$) and the start of counting (**START**) signals can be generated and controlled by the interface bus. The **DATA READY** signal from the **5024** can be monitored either by the inter-

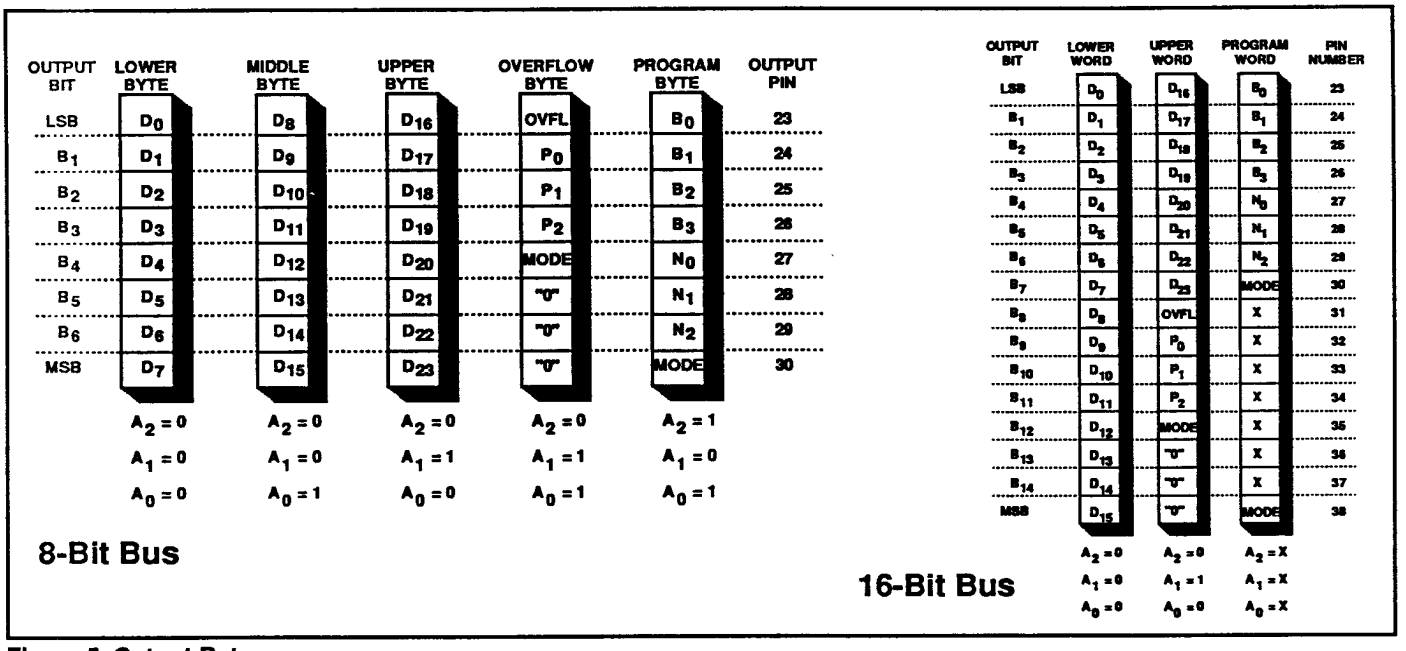
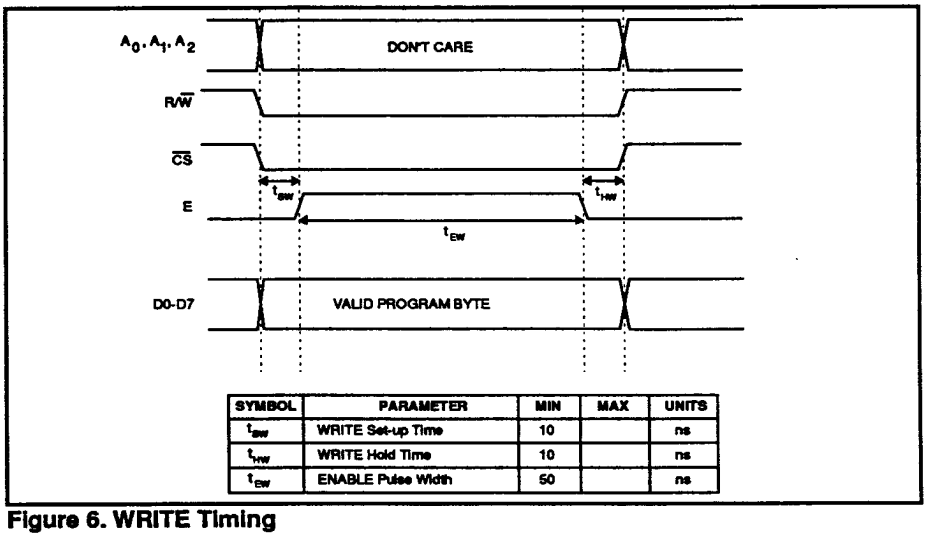


Figure 5. Output Data

face bus as shown in *Figure 8*, or by tying it to an appropriate interrupt request line.

A sample program in BASIC that would access the interface described above is listed here. This would be adapted for the particular version of BASIC used on the PC. All numbers are in HEXADECIMAL. The 74HCT688 (U_2) is set to decode address HEX 300. The second 74HCT688 (U_5) is set to decode address HEX 310. "PB" is the time base program byte.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{sw}	WRITE Set-up Time	10		ns
t_{hw}	WRITE Hold Time	10		ns
t_{EW}	ENABLE Pulse Width	50		ns

Figure 6. WRITE Timing

```
 50 INPUT PB: REM "PB" DENOTES USER-DEFINED 5024 TIME BASE PROGRAM BYTE
100 OUT 319,0:REM RESETS C/T 5024
200 OUT 300,PB:REM WRITES PROGRAM BYTE TO 5024
300 LET X=IN 30D: REM READ PROGRAM BYTE FROM 5024
400 IF X≠PB THEN PRINT "ERROR IN PROGRAM BYTE TO 5024 C/T":GOTO 100
450 OUT 31F,0: REM START COUNTING
500 LET DR=IN 318: REM MONITOR DATA READY FROM 5024 C/T
600 IF DR≠1 THEN GOTO 500: REM IS DATA READY?
700 LET LSB=IN308: REM READ LOWER DATA BYTE
800 LET MDB=(IN 309*256):REM READ MIDDLE DATA BYTE
900 LET MSB=(IN 30A*65536): REM READ UPPER OR MOST SIGNIFICANT BYTE
1000 LET OVFL=IN 30B:REM LINES 1000 TO 1300 TEST FOR ODD OR EVEN NUMBER
1100 LET TEMP=OVFL/2
1200 IF TEMP>1 THEN LET TEMP=TEMP/2: GOTO 1200
1300 IF TEMP=1 THEN LET OVFL:0:GOTO 1500
1400 LET OVFL= 16,777,216:REM WHICH EQUALS 2 TO THE 24TH, OR THE 25TH BIT
1500 LET TOTAL=LSB+MDB+MSB+OVFL
1600 END
```

TypicalApplication 24-Bit A/D Converter Subsystem

The **5024** is ideally suited to provide all of the digital circuitry required in an A/D Converter subsystem using voltage-to-frequency converters. *Figure 9* depicts a very wide dynamic range, precision A/D converter subsystem using the **5024** in conjuction with the **DYMEC Model 2824 24-bit A/D Converter Analog Front-end.** This A/D features 20-bit dynamic range, 24-bit resolution with conversion times of 100ms. The **Model 2824 Front-end** features an instrumentation amplifier with driven guard, internal multiplexer for selecting the input signal, internal reference and ground allowing for self-calibration of the front-end, isolated multiplexer control inputs, precision 10MHz V/F converter, and an isolated frequency output to drive the **5024 Counter/Timer.**

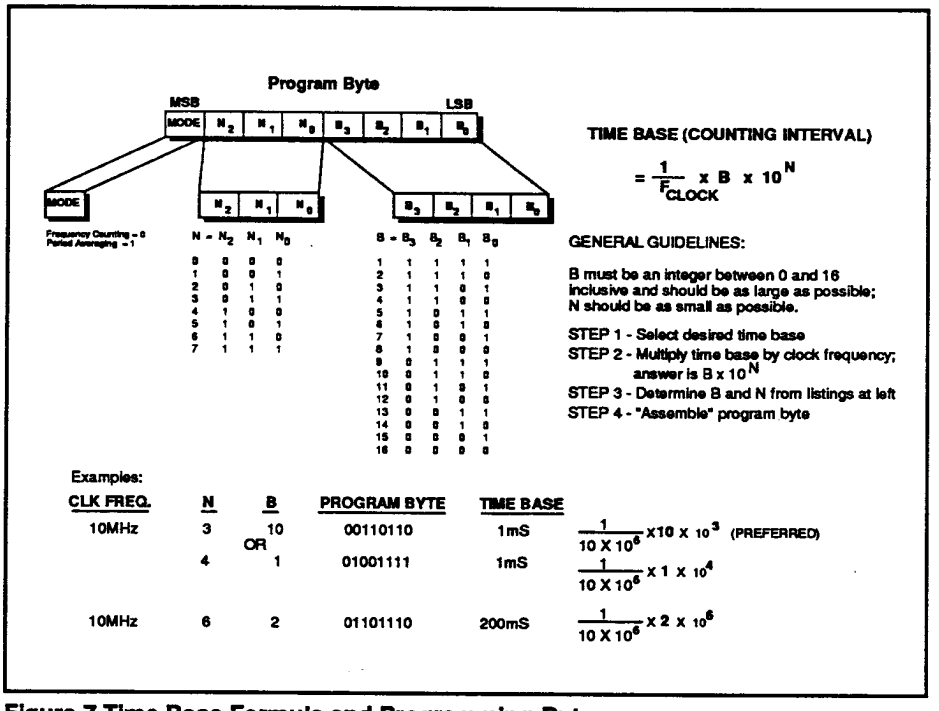


Figure 7.Time Base Formula and Programming Byte

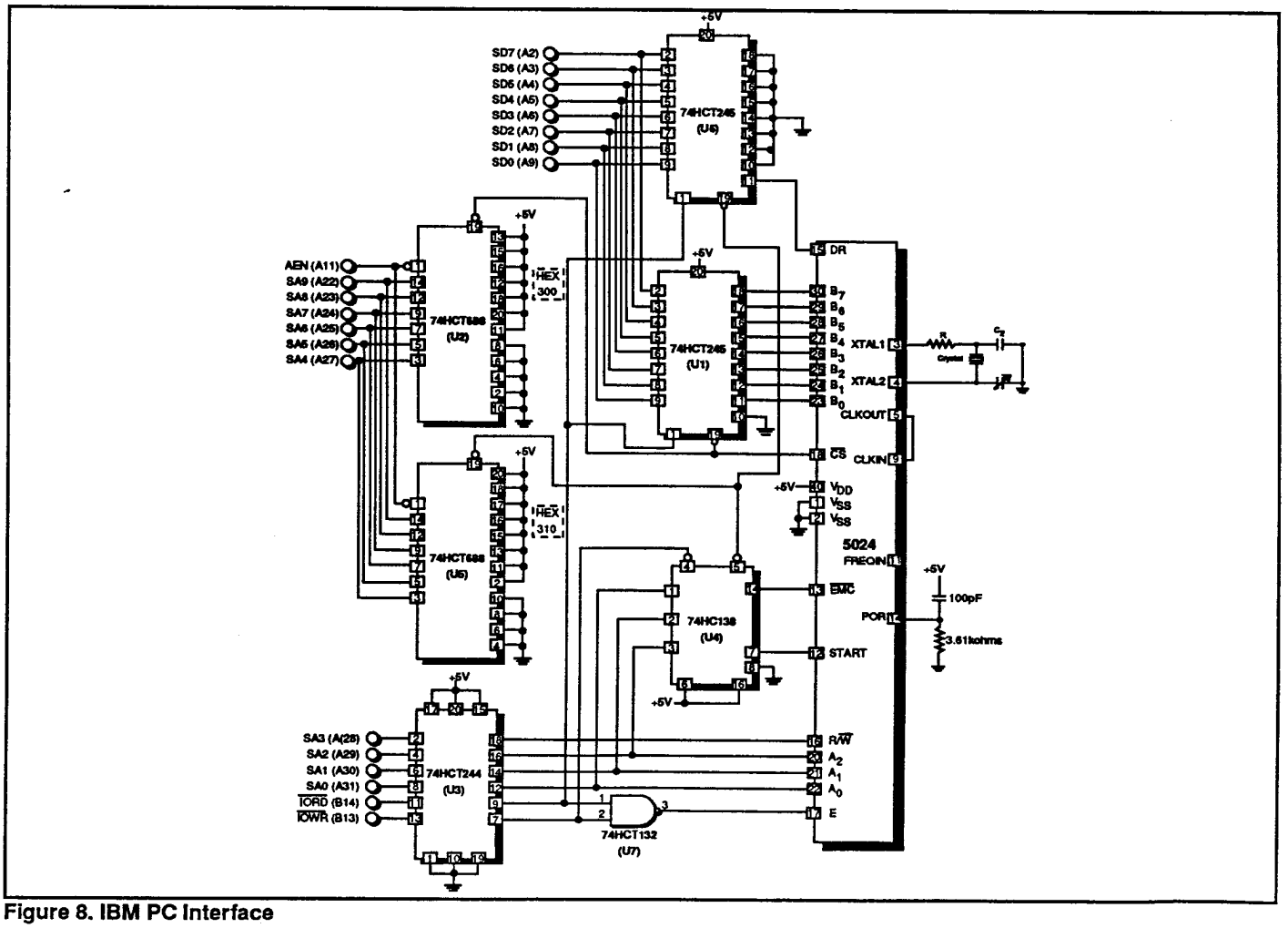
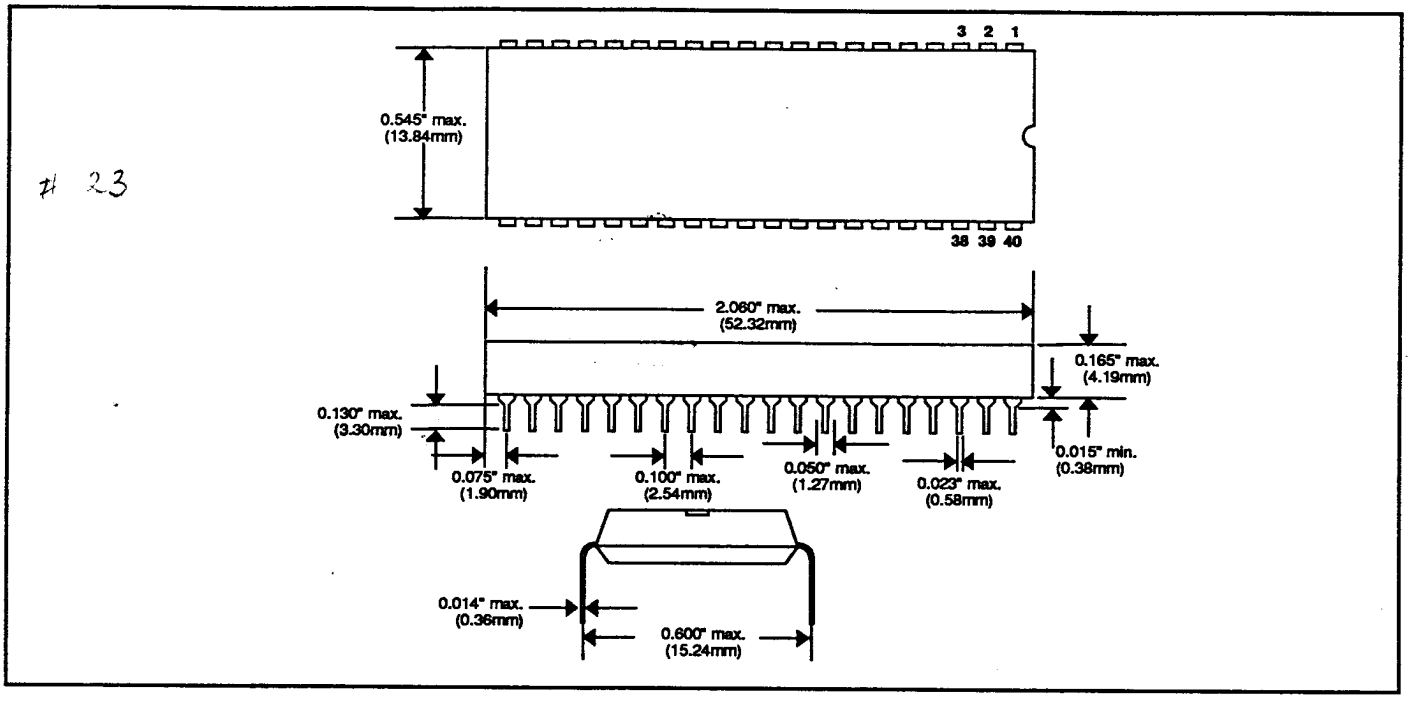


Figure 8. IBM PC Interface

Mechanical Dimensions & Pinout



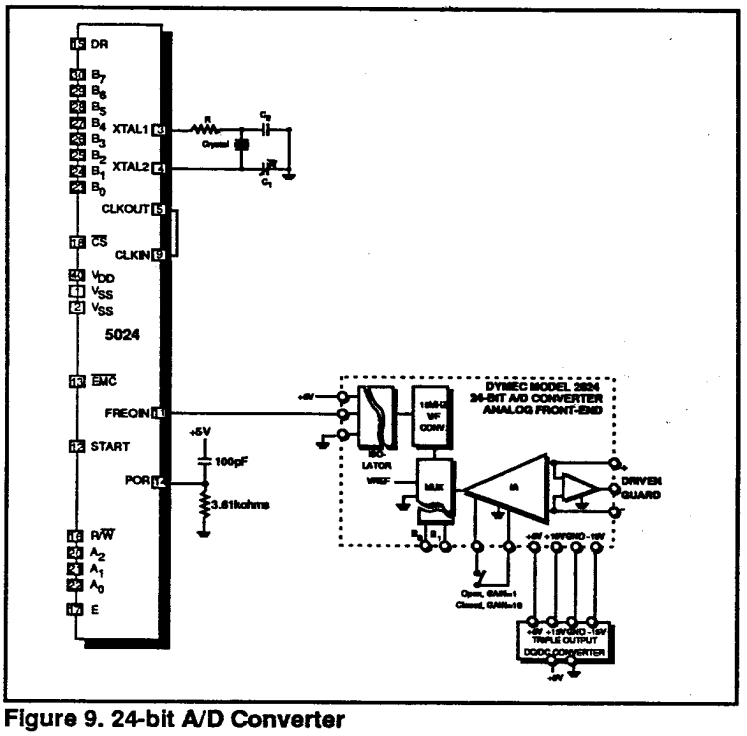


Figure 9. 24-bit A/D Converter

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