GL555
GENERAL PURPOSE BIPOLAR SINGLE TIMER

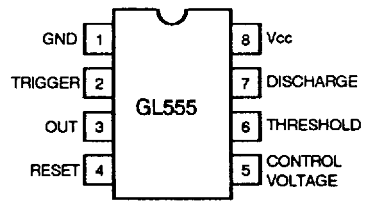
Description

The GL555 Timing Circuit is a very stable controller for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied ending the time-out. The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

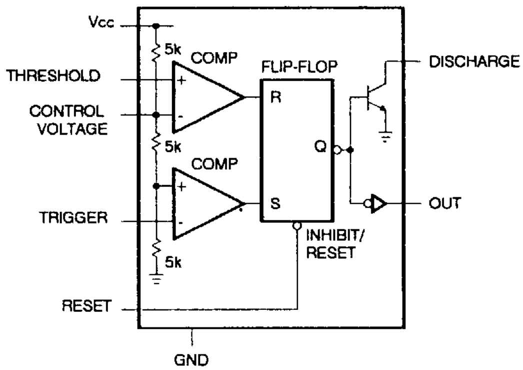
Feature

- Timing Control, μs to Hours.
- Astable or Monostable Operating Modes
- Adjustable Duty cycle
- 200 mA Sink or Source Output Current
- TTL Output Drive Capablilty
- Temperature Stablility of 0.005% / °C Typ
- Normally On or Normally Off Output
- Direct Replacement For SE555/NE555

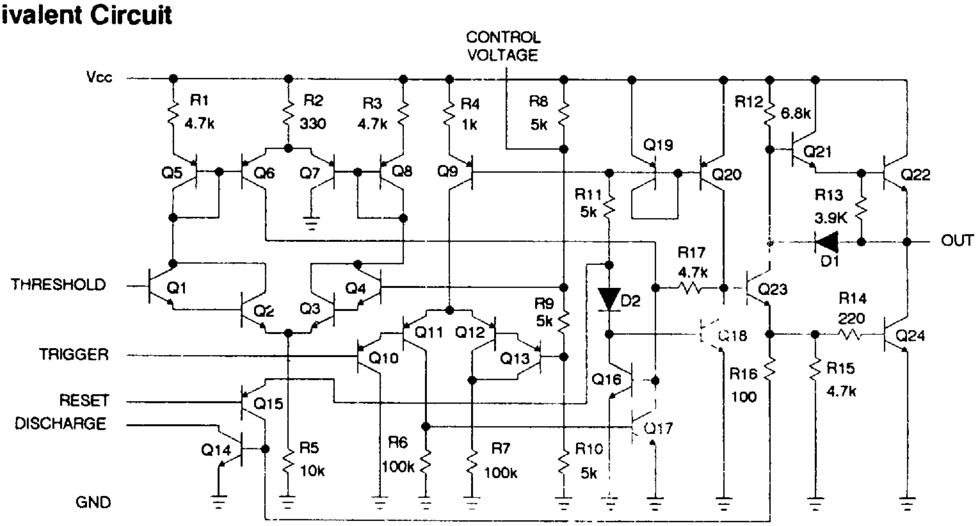
Pin Configuration



Block Diagram



Equivalent Circuit



Absolute Maximum Ratings

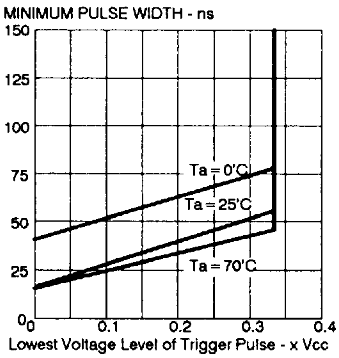
Supply Voltage	V_{CC}	+18	V
Power Dissipation	P_D	0.9	W
Storage Temperature Range	T_{STG}	-65 to +150	°C
Operating Temperature Range	T_{OPR}	0 to 70	°C

Electrical Characteristics : T_A=25°C, V^+ = +5.0 V to +15 V (unless otherwise specified)

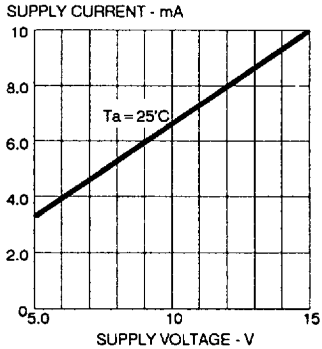
CHARACTERISTIC		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}		4.5		16	V
Supply Current		I_{CC}	V_{CC} = 5V, $R_L = \infty$		3.0	6.0	mA
			V_{CC} = 15V, $R_L = \infty$, LOW State		10	15	
Timing Error	Initial Accuracy	t_D	R1 = 2.0 kΩ to 100 kΩ		1.0		%
	Drift With Temperature		C = 0.1 uF		50		ppm / °C
	Drift With Supply Voltage				0.1	0.5	% / V
Threshold Voltage		V_{TH}	V_{CC} = 5.0 V	2.6	3.33	4.0	V
			V_{CC} = 15 V	9.0	10	11	
Trigger Voltage		V_{TR}	V_{CC} = 15 V	4.0	5.0	6.0	V
			V_{CC} = 5.0 V	1.1	1.67	2.2	
Trigger Current		I_{TR}			0.5	2.0	μA
Reset Voltage		V_R		0.4	0.7	1.0	V
Reset Current		I_R			0.1	0.4	mA
Threshold Current		I_{TH}			30	250	nA
Control Voltage Level		V_{CV}	V_{CC} = 15 V	9.0	10	11	V
			V_{CC} = 5.0 V	2.6	3.33	4.0	
Output Voltage LOW		V_{OL}	V_{CC} = 15 V, I_O^- = 10 mA		0.1	0.25	V
			I_O^- = 50 mA, V_{CC} = 15 V		0.4	0.75	
			I_O^- = 100mA, V_{CC} = 15V		2.0	2.5	
			I_O^- = 200 mA, V_{CC} = 15V		2.5	3.5	
			V_{CC} = 5.0 V, I_O^- = 8.0 mA		0.3		
			I_O^- = 5.0 mA, V_{CC} = 5.0 V		0.25	0.35	
Output Voltage HIGH		V_{OH}	I_O^+ = 200 mA, V_{CC} = 15 V	11.0	12.5		V
			I_O^+ = 100 mA, V_{CC} = 15 V	12.75	13.3		
			V_{CC} = 5.0 V, I_O^+ = 100 mA	2.75	3.3		
Rise Time of Output		t_r			100		ns
Fall Time of Output		t_f			100		ns
Discharge Leakage Current		I_{DIS}			20	100	nA

Typical Performance Curves

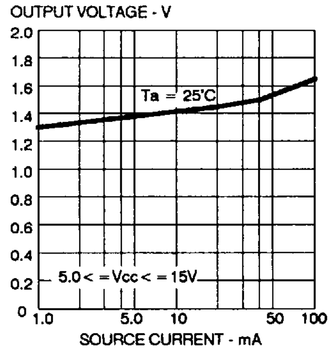
Minimum Pulse Width Required for Triggering



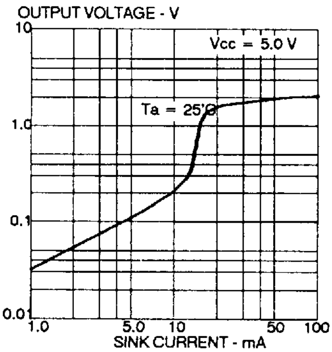
Total Supply Current vs Supply Voltage



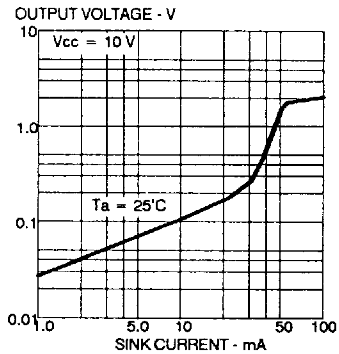
Output Voltage HIGH vs Output Source Current



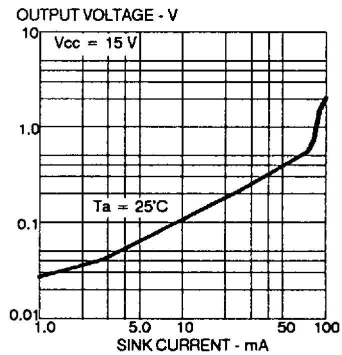
Output Voltage LOW vs Output Sink Current



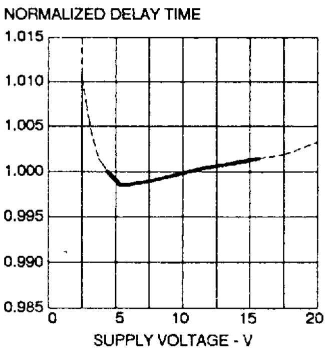
Output Voltage LOW vs Output Sink current



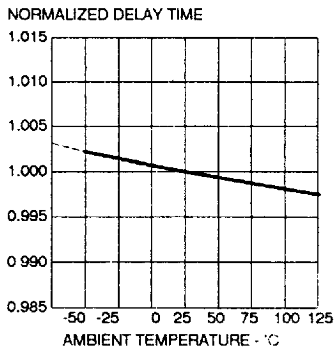
Output Voltage LOW vs Output Sink Current



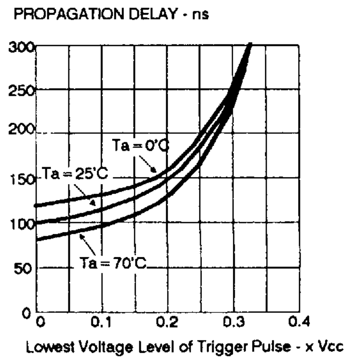
Delay Time vs Supply Voltage



Delay Time vs Ambient Temperature



Propagation Delay vs Voltage Level of Trigger Pulse

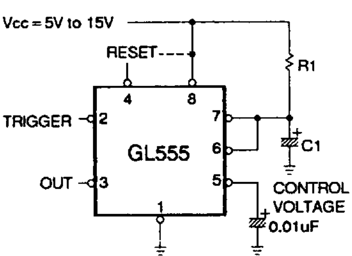


Typical Applications

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one shot. Referring to Figure 1 the external capacitor is initially held discharged by a transistor inside the timer.
When a negative trigger pulse is applied to lead 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R_1C_1$. When the voltage across the capacitor equals $^2/_3$ V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 2 shows the actual waveforms generated in this mode of operation.

Figure 1 Monostable Mode



The circuit triggers on a negative going input signal when the level reaches $^1/_3$ V_{CC}. Once triggered, the circuit remains in this state until the set time elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R_1C_1$ and is easily determined by Figure 3. Notice that since the charge rate and the threshold Level of the Comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the trigger terminal (lead 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.
when Reset is not used, it should be tied HIGH to avoid any possibility of false triggering.

Figure 2 Monostable Waveform

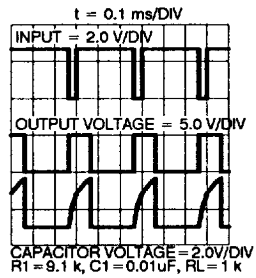
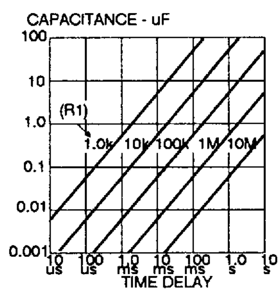


Figure 3 Time Delay vs R_1 and C_1



ASTABLE OPERATION

when the circuit is connected as shown in Figure 4 (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.
In the astable mode of operation, C_1 charges and discharges between $^1/_3$ V_{CC} and $^2/_3$ V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency anr independent of the supply voltage.
Figure 5 shows actual waveforms generated in this mode of operation.
the charge time (output HIGH) is given by :

$$t_1 = 0.693\ (R_1 + R_2)\ C_1$$

and the discharge time (output LOW) by :

$$t_2 = 0.693\ (R_2)\ C_1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R_1 + 2R_2)\ C_1$$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)\ C_1}$$

and may be easily found by Figure 6.
The duty cycle is given by :

$$DC = \frac{R_2}{R_1 + 2R_2}$$

Figure 4 Astable Mode

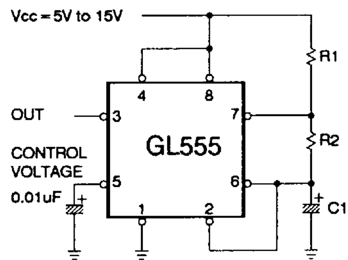


Figure 5 Astable Waveform

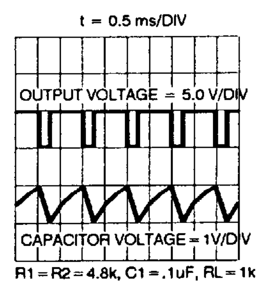


Figure 6 Free Running Frequency vs R_1, R_2, and C_1