19-3353; Rev 0; 8/04

300MHz to 450MHz Low-Power, Crystal-Based +10dBm ASK/FSK Transmitter

MAX1479

General Description

The MAX1479 crystal-referenced phase-locked-loop (PLL) VHF/UHF transmitter is designed to transmit ASK, OOK, and FSK data in the 300MHz to 450MHz frequency range. The MAX1479 supports data rates up to 100kbps in ASK mode and 20kbps in FSK mode (both Manchester coded). The device provides an adjustable output power of more than +10dBm into a 50Ω load. The crystal-based architecture of the MAX1479 eliminates many of the common problems of SAW-based transmitters by providing greater modulation depth, faster frequency settling, higher tolerance of the transmit frequency, and reduced temperature dependence. These improvements enable better overall receiver performance when using the MAX1479 together with a superheterodyne receiver such as the MAX1470, MAX1471, MAX1473, or MAX7033.

The MAX1479 is available in a 16-pin thin QFN package (3mm x 3mm) and is specified for the automotive temperature range from -40°C to +125°C.

Applications

Remote Keyless Entry
Tire Pressure Monitoring
Security Systems
Radio-Controlled Toys
Wireless Game Consoles
Wireless Computer Peripherals
Wireless Sensors
RF Remote Controls
Garage Door Openers

Features

- ♦ **ETSI-Compliant EN300 220**
- ♦ **+2.1V to +3.6V Single-Supply Operation**
- ♦ **Supports ASK, OOK, and FSK Modulations**
- ♦ **Adjustable FSK Shift**
- ♦ **+10dBm Output Power into 50Ω Load**
- ♦ **Low Supply Current (6.7mA in ASK Mode, and 10.5mA in FSK Mode)**
- ♦ **Uses Small Low-Cost Crystal**
- ♦ **Small 16-Pin Thin QFN Package**
- ♦ **Fast-On Oscillator—200µs Startup Time**
- ♦ **Programmable Clock Output**

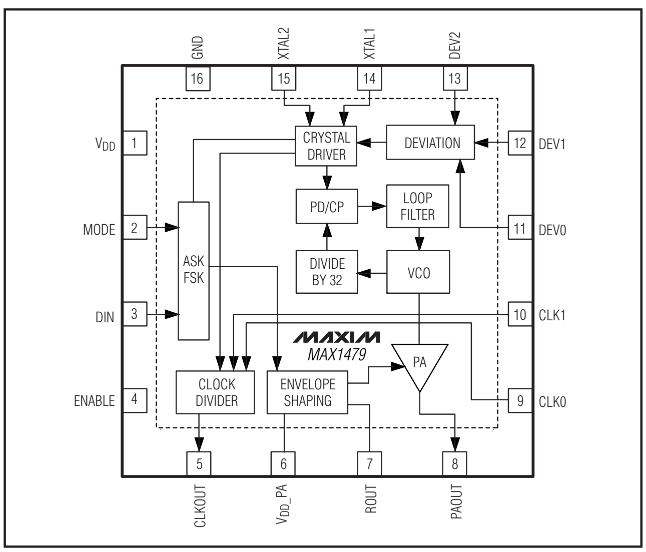
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1479ATE	-40°C to +125°C	16 Thin QFN-EP*

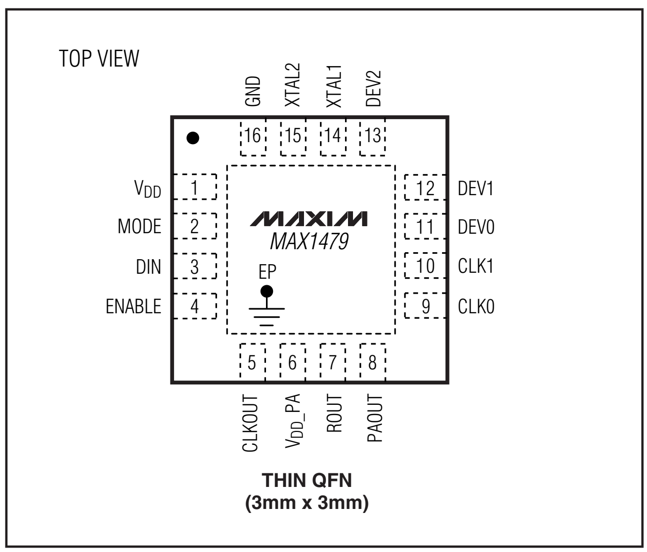
**EP = Exposed paddle.*

Typical Application Circuit appears at end of data sheet.

Functional Diagram



Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

300MHz to 450MHz Low-Power, Crystal-Based +10dBm ASK/FSK Transmitter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +4V
All Other Pins to GND ....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16-Pin Thin QFN (derate 14.7mW/°C above +70°C)...1176.5mW
Operating Temperature Range ....-40°C to +125°C
Junction Temperature...+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +2.1V to +3.6V, V_{ENABLE} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}			2.1		3.6	V
Supply Current	I_{DD}	PA off, V_{DIN} at 0% duty cycle (ASK or FSK) (Note 2)	f_{RF} = 315MHz		2.9	4.3	mA
			f_{RF} = 433MHz		3.3	4.8	
		V_{DIN} at 50% duty cycle (ASK) (Notes 3, 4)	f_{RF} = 315MHz		6.7	10.7	
			f_{RF} = 433MHz		7.3	11.4	
		V_{DIN} at 100% duty cycle (FSK)	f_{RF} = 315MHz (Note 2)		10.5	17.1	
			f_{RF} = 433MHz (Note 4)		11.4	18.1	
Standby Current	I_{STDBY}	V_{ENABLE} < V_{IL}	T_A = +25°C		0.2		nA
			T_A < +85°C (Note 4)		120	300	
			T_A < +125°C (Note 2)		700	1600	
DIGITAL INPUTS AND OUTPUTS							
Data Input High	V_{IH}	(Note 2)		V_{DD} - 0.25			V
Data Input Low	V_{IL}	(Note 2)				0.25	V
Maximum Input Current	I_{IN}				20		µA
Output Voltage High	V_{OH}	CLKOUT, load = 10kΩ ll 10pF (Note 4)		V_{DD} - 0.25			V
Output Voltage Low	V_{OL}	CLKOUT, load = 10kΩ ll 10pF (Note 4)				0.25	V

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +2.1V to +3.6V, V_{ENABLE} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE							
Frequency Range	f_{RF}	(Note 2)		300		450	MHz
Turn-On Time (Note 5)	t_{ON}	Settle to within 50kHz			200		µs
		Settle to within 5kHz			350		
Maximum Data Rate (Note 4)		ASK mode (Manchester coded)			100		kbps
		FSK mode (Manchester coded)			20		
Maximum FSK Frequency Deviation		DEV[2:0] = 111 (Note 6)	f_{RF} = 315MHz		55		kHz
			f_{RF} = 433MHz		80		
Output Power (Note 2)	P_{OUT}	T_A = +25°C, V_{DD} = +2.7V		6.8	10	12.0	dBm
		T_A = +125°C, V_{DD} = +2.1V		2.7	5.3		
		T_A = -40°C, V_{DD} = +3.6V			12.2	16.1	
Transmit Efficiency with CW Tone (Note 7)		f_{RF} = 315MHz			35		%
		f_{RF} = 433MHz			34		
Transmit Efficiency at 50% Duty Cycle		f_{RF} = 315MHz			27		%
		f_{RF} = 433MHz			25		
PHASE-LOCKED-LOOP PERFORMANCE							
VCO Gain	K_{VCO}				280		MHz/V
Phase Noise		f_{RF} = 315MHz	f_{OFFSET} = 100kHz		-75		dBc/Hz
			f_{OFFSET} = 1MHz		-98		
		f_{RF} = 433MHz	f_{OFFSET} = 100kHz		-74		
			f_{OFFSET} = 1MHz		-98		
Maximum Carrier Harmonics		f_{RF} = 315MHz			-50		dBc
		f_{RF} = 433MHz			-45		
Reference Spur					-40		dBc
Loop Bandwidth	BW				300		kHz
Crystal Frequency Range	f_{XTAL}				f_{RF}/32		MHz
Crystal Tolerance					50		ppm
Crystal Load Capacitance	C_{LOAD}	(Note 8)			4.5		pF
Clock Output Frequency		Determined by CLK0 and CLK1; see Table 1			F_{XTAL} / N		MHz

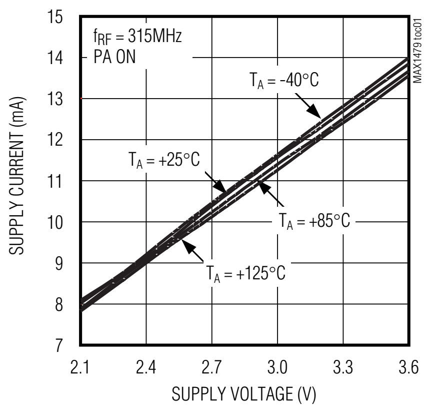
Note 1: Supply current, output power, and efficiency are greatly dependent on board layout and PAOUT match.
Note 2: 100% tested at T_A = +125°C. Guaranteed by design and characterization over temperature.
Note 3: 50% duty cycle at 10kHz ASK data (Manchester coded).
Note 4: Guaranteed by design and characterization, not production tested.
Note 5: V_{ENABLE} = V_{IL} to V_{ENABLE} = V_{IH}. f_{OFFSET} is defined as the frequency deviation from the desired carrier frequency.
Note 6: Dependent on crystal and PC board trace capacitance.
Note 7: V_{ENABLE} > V_{IH}, V_{DATA} > V_{IH}, Efficiency = P_{OUT} / (V_{DD} x I_{DD}).
Note 8: Dependent on PC board trace capacitance.

300MHz to 450MHz Low-Power, Crystal-Based +10dBm ASK/FSK Transmitter

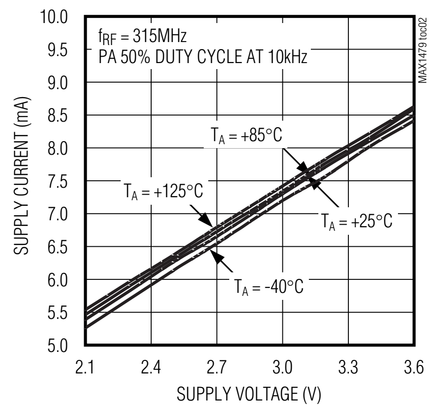
Typical Operating Characteristics

(*Typical Application Circuit*, V_{DD} = +2.7V, T_A = +25°C, unless otherwise noted.)

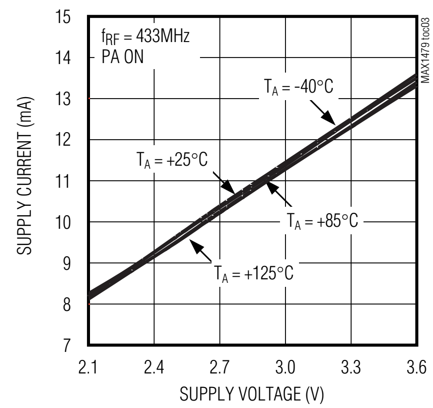
SUPPLY CURRENT vs. SUPPLY VOLTAGE



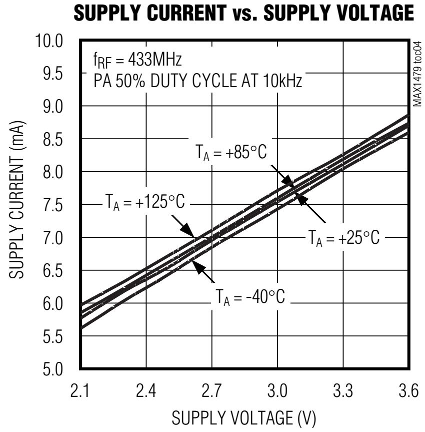
SUPPLY CURRENT vs. SUPPLY VOLTAGE



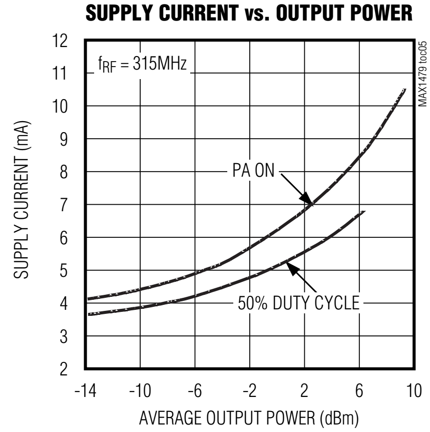
SUPPLY CURRENT vs. SUPPLY VOLTAGE



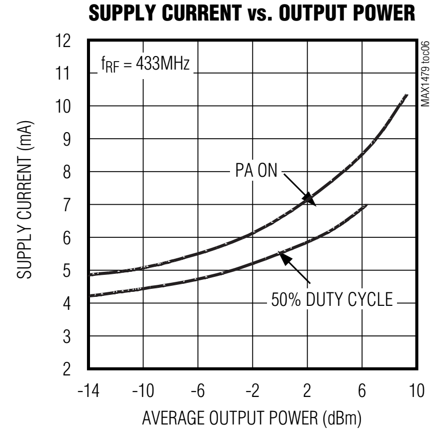
SUPPLY CURRENT vs. SUPPLY VOLTAGE



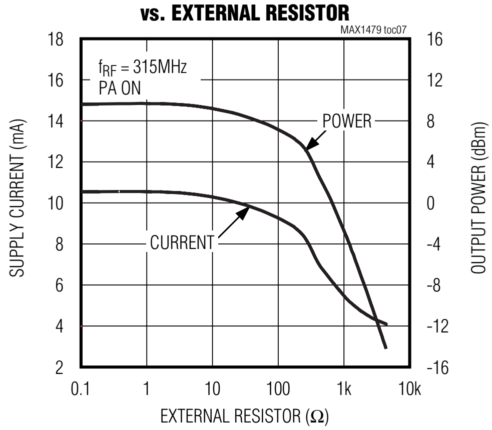
SUPPLY CURRENT vs. OUTPUT POWER



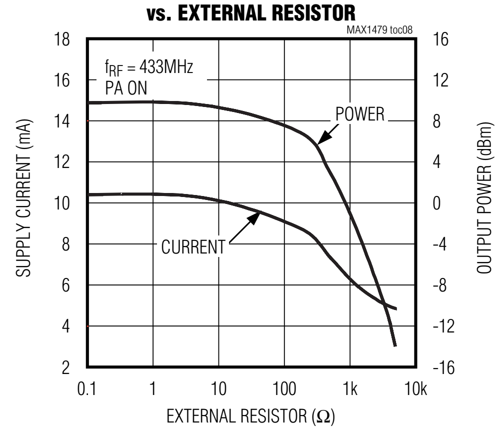
SUPPLY CURRENT vs. OUTPUT POWER



SUPPLY CURRENT AND OUTPUT POWER vs. EXTERNAL RESISTOR



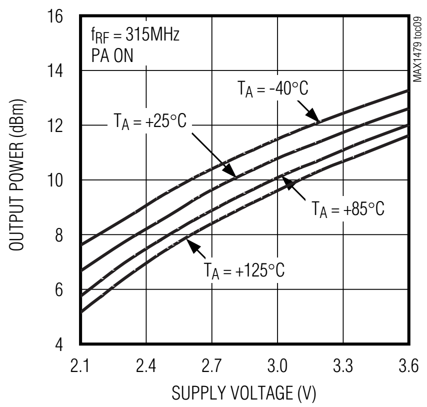
SUPPLY CURRENT AND OUTPUT POWER vs. EXTERNAL RESISTOR



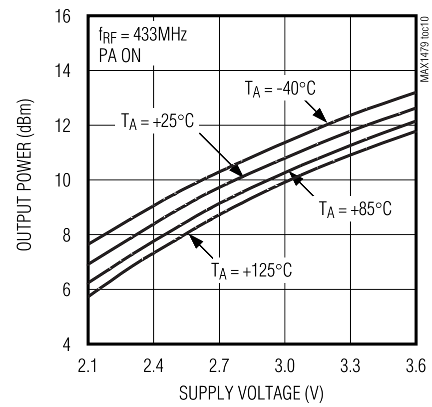
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{DD} = +2.7V, T_A = +25°C, unless otherwise noted.)

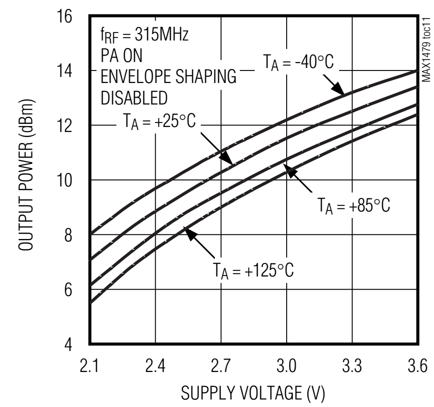
OUTPUT POWER vs. SUPPLY VOLTAGE



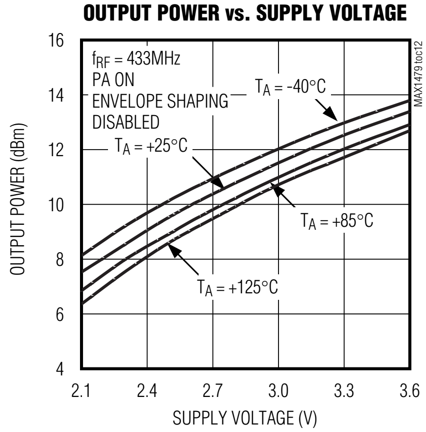
OUTPUT POWER vs. SUPPLY VOLTAGE



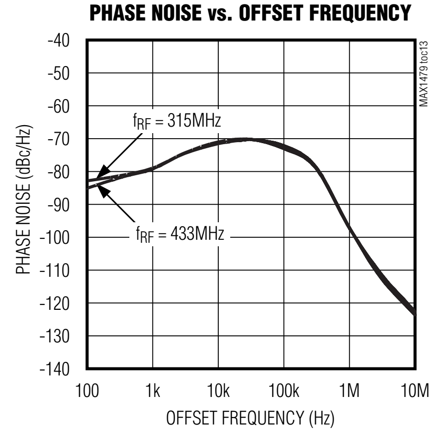
OUTPUT POWER vs. SUPPLY VOLTAGE



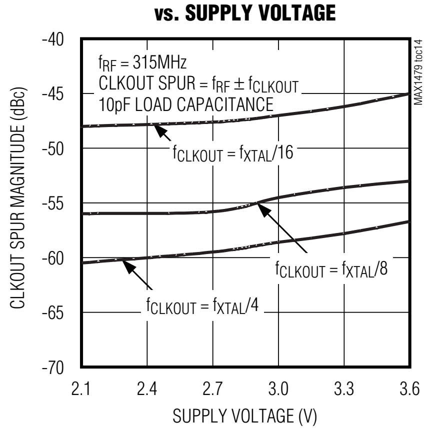
OUTPUT POWER vs. SUPPLY VOLTAGE



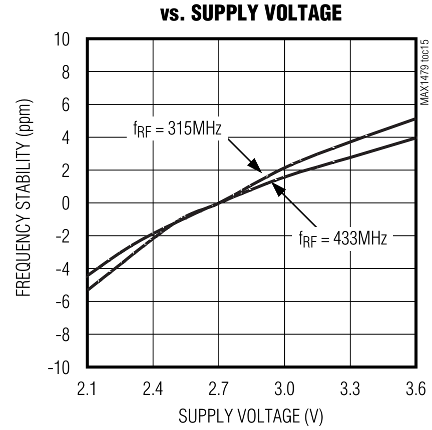
PHASE NOISE vs. OFFSET FREQUENCY



CLOCK SPUR MAGNITUDE vs. SUPPLY VOLTAGE



FREQUENCY STABILITY vs. SUPPLY VOLTAGE



300MHz to 450MHz Low-Power, Crystal-Based +10dBm ASK/FSK Transmitter

Pin Description

PIN	NAME	DESCRIPTION
1	V_{DD}	Supply Voltage. Bypass to GND with a 10nF and 220pF capacitor as close to the pin as possible.
2	MODE	Mode Select. A logic low on MODE enables the device in ASK mode. A logic high on MODE enables the device in FSK mode.
3	DIN	Data Input. Power amplifier is on when DIN is high in ASK mode. Frequency is high when DIN is high in FSK mode.
4	ENABLE	Standby/Power-Up Input. A logic low on ENABLE sets the device in standby mode.
5	CLKOUT	Buffered Clock Output. Programmable through CLK0 and CLK1. See Table 1.
6	V_{DD}_PA	Power-Amplifier Supply Voltage. Bypass to GND with a 10nF and 220pF capacitor as close to the pin as possible.
7	ROUT	Envelope-Shaping Output. ROUT controls the power-amplifier envelope rise and fall. Bypass to GND with a 680pF and 220pF capacitor as close to the pin as possible.
8	PAOUT	Power-Amplifier Output. Requires a pullup inductor to the supply voltage, which can be part of the output-matching network to an antenna.
9	CLK0	1st Clock Divider Setting. See Table 1.
10	CLK1	2nd Clock Divider Setting. See Table 1.
11	DEV0	1st FSK Frequency-Deviation Setting. See Table 2.
12	DEV1	2nd FSK Frequency-Deviation Setting. See Table 2.
13	DEV2	3rd FSK Frequency-Deviation Setting. See Table 2.
14	XTAL1	1st Crystal Input. $f_{RF} = 32 \times f_{XTAL}$.
15	XTAL2	2nd Crystal Input. $f_{RF} = 32 \times f_{XTAL}$.
16	GND	Ground. Connect to system ground.
—	EP	Exposed Ground Paddle. EP is the power amplifier's ground. It must be connected to PC board through a low-inductance path.

Detailed Description

The MAX1479 is a highly integrated ASK/FSK transmitter operating over the 300MHz to 450MHz frequency band. The device requires only a few external components to complete a transmitter solution. The MAX1479 includes a complete PLL and a highly efficient power amplifier. The device can be set into a 0.2nA low-power shutdown mode.

Shutdown Mode

ENABLE (pin 4) is internally pulled down with a 20µA current source. If it is left unconnected or pulled low, the MAX1479 goes into a low-power shutdown mode. In this mode, the supply current drops to 0.2nA. When ENABLE is high, the device is enabled and is ready for transmission after 200µs (frequency settles to within 50kHz).

The 200µs turn-on time of the MAX1479 is mostly dominated by the crystal oscillator startup time. Once the oscillator is running, the 300kHz PLL bandwidth allows fast frequency recovery during power-amplifier toggling.

Mode Selection

MODE (pin 2) sets the MAX1479 in either ASK or FSK mode. When MODE is set low, the device operates as an ASK transmitter. If MODE is set high, the device operates as an FSK transmitter. In the ASK mode, the DIN pin controls the output of the power amplifier. A logic low on DIN turns off the PA, and a logic high turns on the PA. In the FSK mode, a logic low on the DIN pin is represented by the low FSK frequency, and a logic-high input is represented by the high FSK frequency. (The ASK carrier frequency and the lower FSK frequency are the same.) The deviation is proportional to the crystal load impedance and pulling capacitance. The maximum frequency deviation is 55kHz for f_{RF} = 315MHz and 80kHz for f_{RF} = 433MHz.

Clock Output

The MAX1479 has a dedicated digital output pin for the frequency-divided crystal clock signal. This is to be used as the time base for a microprocessor. The frequency-division ratio is programmable through two digital input pins (CLK0, CLK1), and is defined in Table 1. The clock output is designed to drive a 3.5MHz CMOS rail-to-rail signal into a 10pF capacitive load.

Envelope-Shaping Resistor

The envelope-shaping resistor allows for a gentle turn-on/turn-off of the PA in ASK mode. This results in a smaller spectral width of the modulated PA output signal.

Phase-Locked Loop

The PLL block contains a phase detector, charge pump, integrated loop filter, VCO, asynchronous 32x clock divider, and crystal oscillator. The PLL requires no external components. The relationship between the carrier and crystal frequency is given by:

$$f_{XTAL} = f_{RF} / 32$$

Crystal Oscillator

The crystal oscillator in the MAX1479 is designed to present a capacitance of approximately 3pF to ground from the XTAL1 and XTAL2 pins in ASK mode. In most cases, this corresponds to a 4.5pF load capacitance applied to the external crystal when typical PC board parasitics are added. In FSK mode, a percentage (defined by bits DEV0 to DEV2) of the 3pF internal crystal oscillator capacitance is removed for a logic 1 on the DIN pin to pull the transmit frequency. The frequency deviation is shown in Table 2. **It is very important to use a crystal with a load capacitance that is equal to the capacitance of the MAX1479 crystal oscillator plus PC board parasitics**. If very large FSK frequency deviations are desired, use a crystal with a larger motional capacitance and/or reduce PC board parasitic capacitances.

Power Amplifier

The PA of the MAX1479 is a high-efficiency, open-drain, class-C amplifier. With a proper output-matching network, the PA can drive a wide range of impedances, including small-loop PC board trace antennas and any 50Ω antennas. The output-matching network for a 50Ω antenna is shown in the *Typical Application Circuit*. The output-matching network suppresses the carrier harmonics and transforms the antenna impedance to an optimal impedance at PAOUT (pin 8), which is about 250Ω.

When the output-matching network is properly tuned, the power amplifier is highly efficient. The *Typical Application Circuit* delivers +10dBm at a supply voltage of +2.7V, and draws a supply current of 6.7mA for ASK/OOK operation (V_{DIN} at 50% duty cycle) and 10.5mA for FSK operation. Thus, the overall efficiency at 100% duty cycle is 35%. The efficiency of the power amplifier itself is about 50%. An external resistor at ROUT sets the output power.

Table 1. Clock Divider Settings

CLK1	CLK0	CLKOUT
0	0	Logic 0
0	1	f_{XTAL} / 4
1	0	f_{XTAL} / 8
1	1	f_{XTAL} / 16

Table 2. Frequency-Deviation Settings

DEV2	DEV1	DEV0	DEVIATION
0	0	0	1/8 x max
0	0	1	1/4 x max
0	1	0	3/8 x max
0	1	1	1/2 x max
1	0	0	5/8 x max
1	0	1	3/4 x max
1	1	0	7/8 x max
1	1	1	Max

Applications Information

Output Matching to 50Ω

When matched to a 50Ω system, the MAX1479 PA is capable of delivering more than +10dBm of output power at V_{DD} = 2.7V. The output of the PA is an open-drain transistor that requires external impedance matching and pullup inductance for proper biasing. The pullup inductance from PAOUT to V_{DD} serves three main purposes: It forms a resonant tank circuit with the capacitance of the PA output, provides biasing for the PA, and becomes a high-frequency choke to reduce the RF energy coupling into V_{DD}. Maximum efficiency is achieved when the PA drives a load of 250Ω. The recommended output-matching network topology is shown in the *Typical Application Circuit*.

300MHz to 450MHz Low-Power, Crystal-Based +10dBm ASK/FSK Transmitter

Output Matching to PC Board Loop Antenna

In most applications, the MAX1479 power-amplifier output has to be impedance matched to a small-loop antenna. The antenna is usually fabricated out of a copper trace on a PC board in a rectangular, circular, or square pattern. The antenna has an impedance that consists of a lossy component and a radiative component. To achieve high radiating efficiency, the radiative component should be as high as possible, while minimizing the lossy component. In addition, the loop antenna has an inherent loop inductance associated with it (assuming the antenna is terminated to ground). For example, in a typical application, the radiative impedance is less than 0.5Ω, the lossy impedance is less than 0.7Ω, and the inductance is approximately 50nH to 100nH.

The objective of the matching network is to match the power-amplifier output to the impedance of the small-loop antenna. The matching components thus tune out the loop inductance and transform the low radiative and resistive parts of the antenna into the much higher value of the PA output. This gives higher efficiency. The low radiative and lossy components of the small-loop antenna result in a higher Q matching network than the 50Ω network; thus, the harmonics are lower.

Table 3. Component Values for Typical Application Circuit

COMPONENT	VALUE FOR f_{RF} = 433MHz	VALUE FOR f_{RF} = 315MHz
L1	22nH	27nH
L3	18nH	22nH
C1	6.8pF	15pF
C2	10pF	22pF
C3	10nF	10nF
C4	680pF	680pF
C6	6.8pF	15pF
C8	220pF	220pF
C10	10nF	10nF
C11	220pF	220pF
C12	220pF	220pF
C14	100pF	100pF
C15	100pF	100pF

Layout Considerations

A properly designed PC board is an essential part of any RF/microwave circuit. On the power-amplifier output, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation.

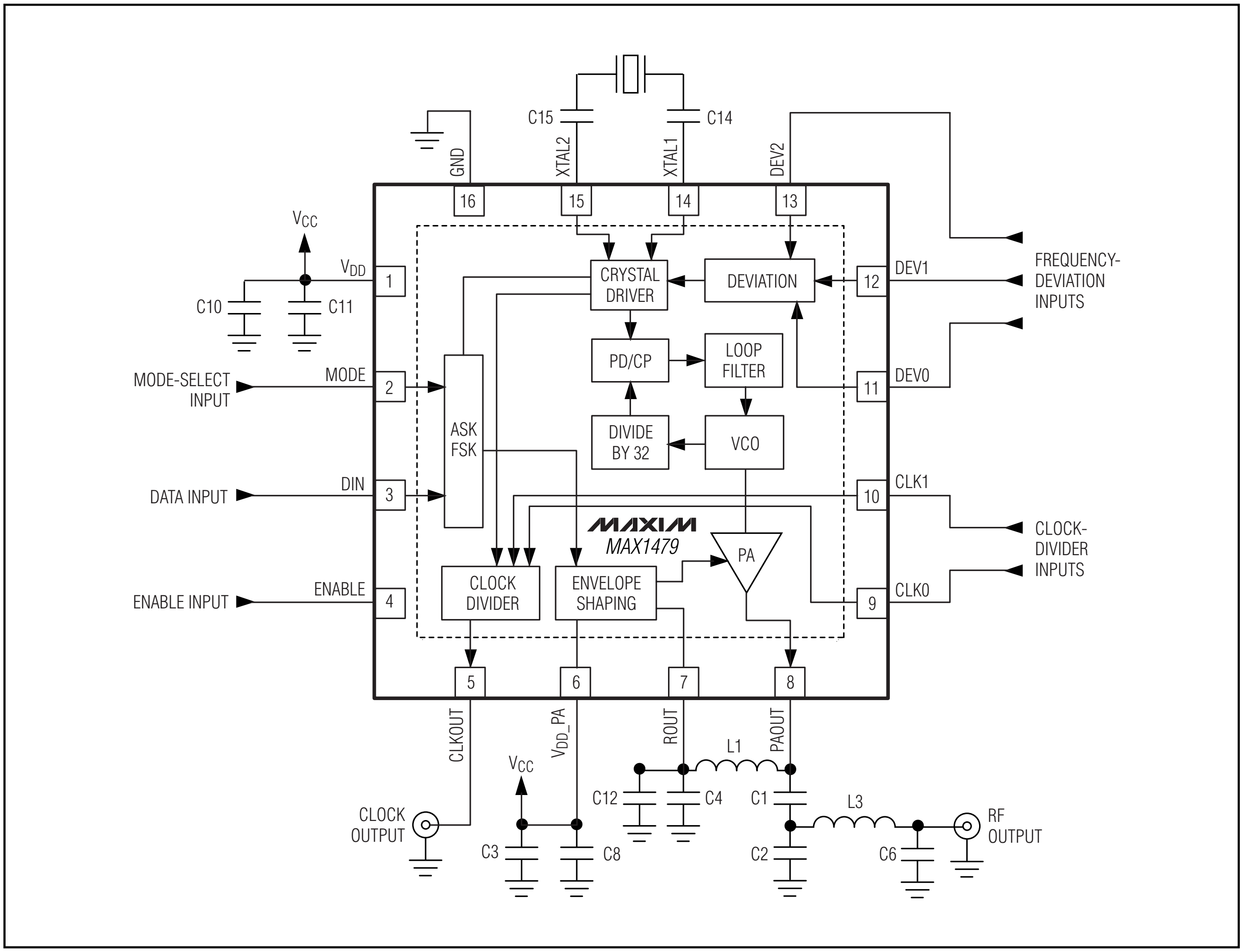
Keeping the traces short reduces parasitic inductance. Generally, 1in of PC board trace adds about 20nH of parasitic inductance. Parasitic inductance can have a dramatic effect on the effective inductance. For example, a 0.5in trace connecting a 100nH inductor adds an extra 10nH of inductance, or 10%.

To reduce the parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Using a solid ground plane can reduce the parasitic inductance from approximately 20nH/in to 7nH/in. Also, use low-inductance connections to ground on all GND pins and place decoupling capacitors close to all V_{DD} connections.

Chip Information

TRANSISTOR COUNT: 2369
PROCESS: CMOS

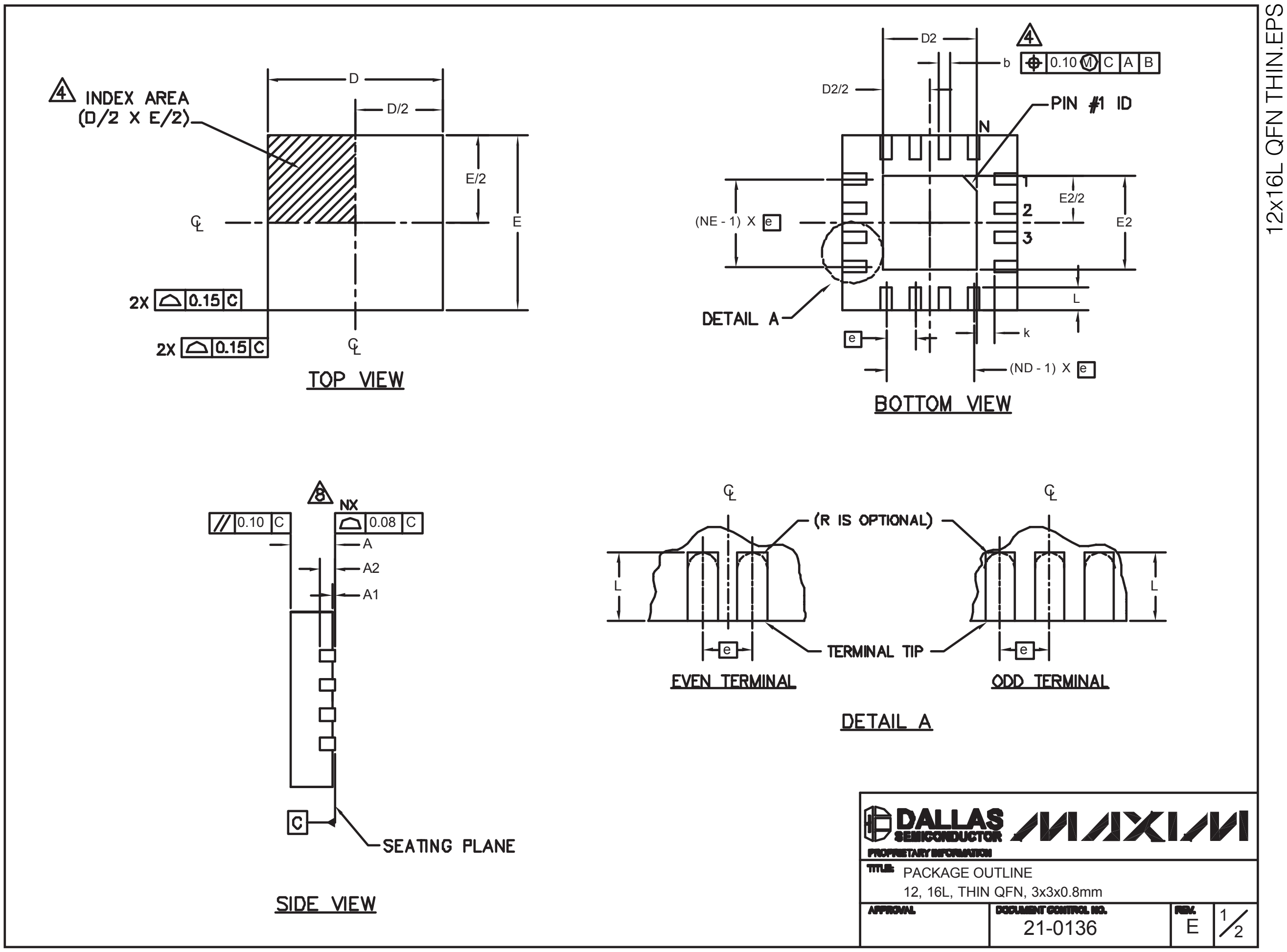
Typical Application Circuit



300MHz to 450MHz Low-Power, Crystal-Based +10dBm ASK/FSK Transmitter

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
12, 16L, THIN QFN, 3x3x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	E	2/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

© 2004 Maxim Integrated Products Printed USA MAXIM is a registered trademark of Maxim Integrated Products.