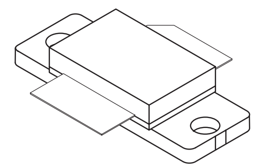
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF6522-70
MRF6522-70R3

921 – 960 MHz, 70 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465D–04, STYLE 1
(NI–600)

Designed for GSM 900 frequency band, the high gain and broadband performance of these devices make them ideal for large–signal, common source amplifier applications in 26 volt base station equipment.

- Specified Performance @ Full GSM Band, 921–960 MHz, 26 Volts
  Output Power, P1dB — 80 Watts (Typ)
  Power Gain @ P1dB — 16 dB (Typ)
  Efficiency @ P1dB — 58% (Typ)
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	7	Adc
Total Device Dissipation @ $T_C \geq 25°C$ Derate above 25°C	P_D	159 0.9	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	°C/W

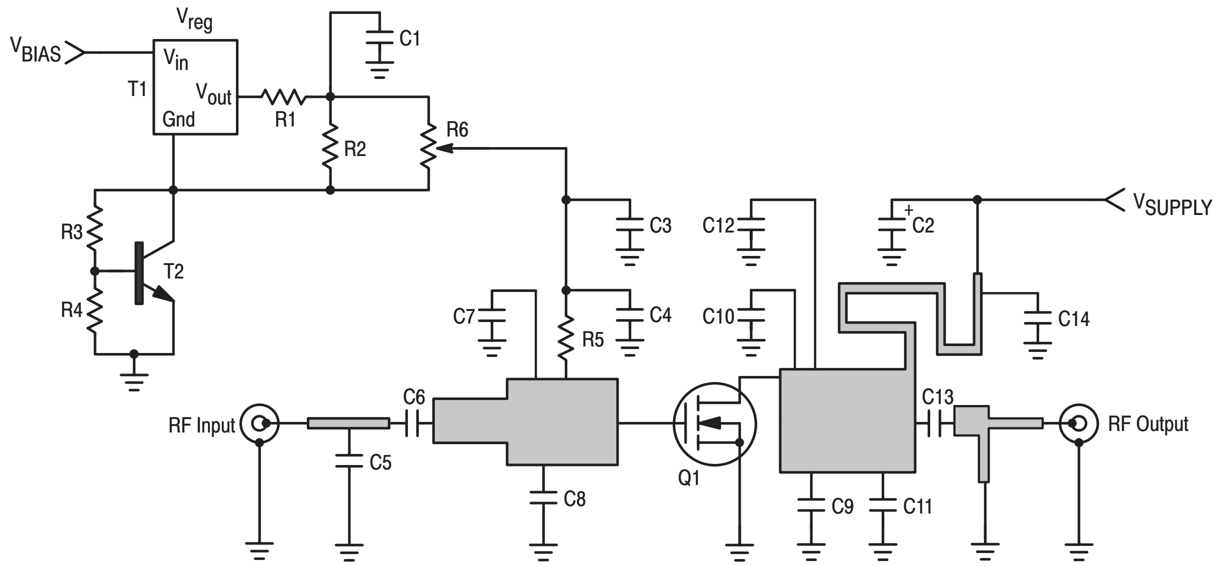
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 400 mAdc)	$V_{GS(Q)}$	3	4	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.15	0.6	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	2	3	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	130	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	41	47	52	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	2.4	3	3.4	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Output Power (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	P1dB	73	80	—	W
Common–Source Amplifier Power Gain @ P1dB (Min) (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	G_{ps}	14	16	18	dB
Drain Efficiency @ P_{out} = 50 W (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	η_1	47	51	—	%
Drain Efficiency @ P1dB (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	η_2	—	58	—	%
Input Return Loss @ P_{out} = 50 W (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = 921 MHz and 960 MHz f = 940 MHz)	IRL	 — —	 — —	 –10 –15	dB
Output Mismatch Stress (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz, VSWR = 5:1, All Phase Angles)	Ψ	No Degradation In Output Power Before and After Test			

(1) Value excludes the input matching.

(2) To meet application requirements, Motorola test fixtures have been designed to cover full GSM 900 band ensuring batch–to–batch consistency.



C1	1.0 μF Chip Capacitor (0805)	R3	1.2 kΩ Chip Resistor (0805)
C2	10 μF, 35 Vdc Tantalum Capacitor	R4	2.2 kΩ Chip Resistor (0805)
C3	100 nF Chip Capacitor	R5	220 Ω Chip Resistor (0805)
C4, C6, C14	22 pF Chip Capacitors, ACCU–P (0805)	R6	5.0 kΩ SMD Potentiometer
C5	2.7 pF Chip Capacitor, ACCU–P (0805)		
C7, C8, C13	4.7 pF Chip Capacitors, ACCU–P (0805)	T1	LP2951 Micro–8
C9, C10	8.2 pF Chip Capacitors, ACCU–P (0805)	T2	BC847 SOT–23
C11, C12	2.2 pF Chip Capacitors, ACCU–P (0805)		
R1	10 Ω Chip Resistor (0805)	SUBSTRATE	GI180 0.8 mm
R2	1.0 kΩ Chip Resistor (0805)		

Figure 1. MRF6522–70 Test Circuit Schematic

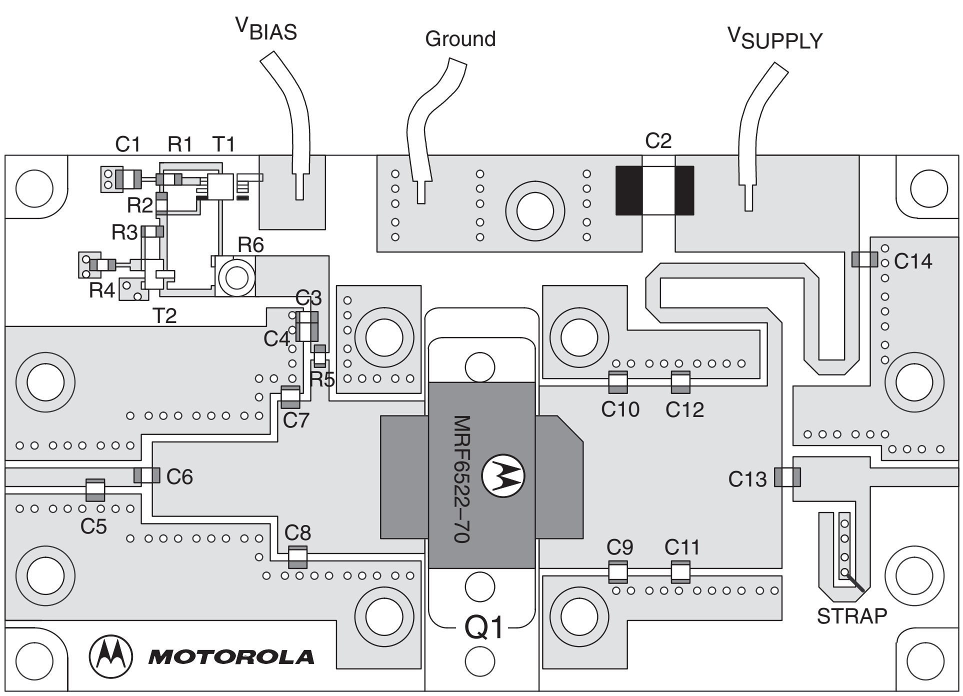


Figure 2. MRF6522–70 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

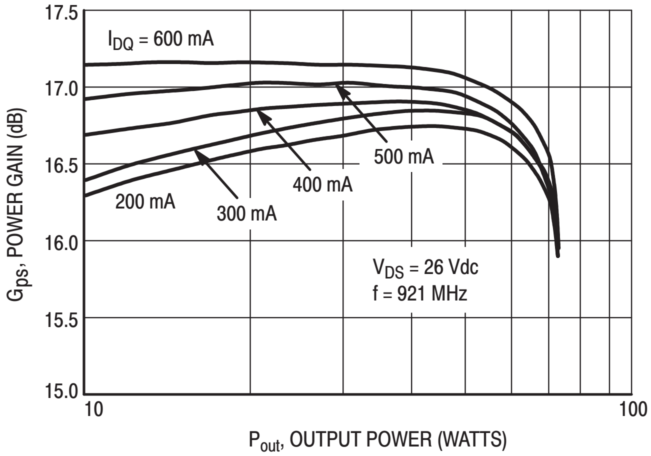


Figure 3. Power Gain versus Output Power

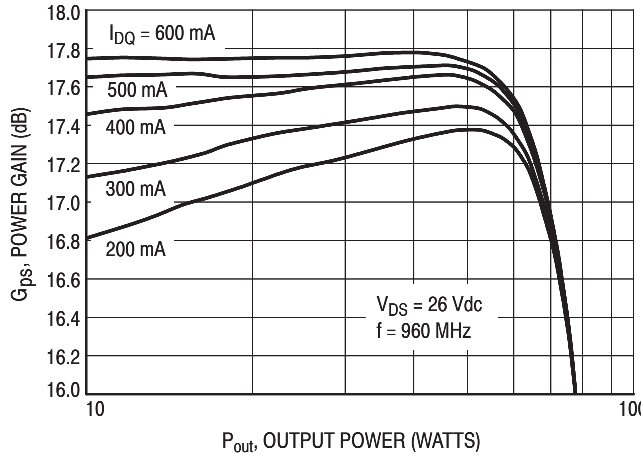


Figure 4. Power Gain versus Output Power

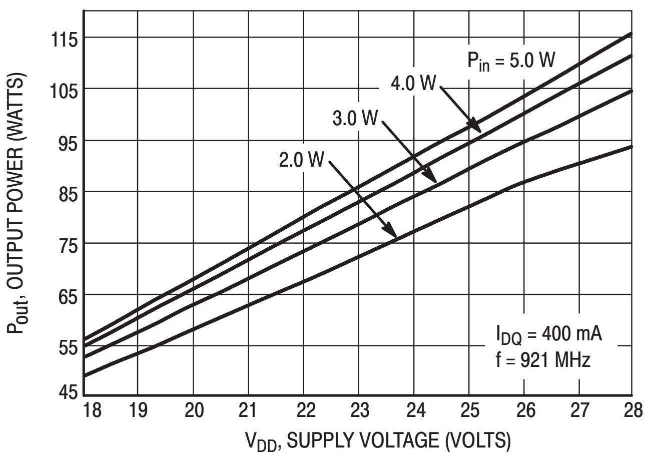


Figure 5. Output Power versus Supply Voltage

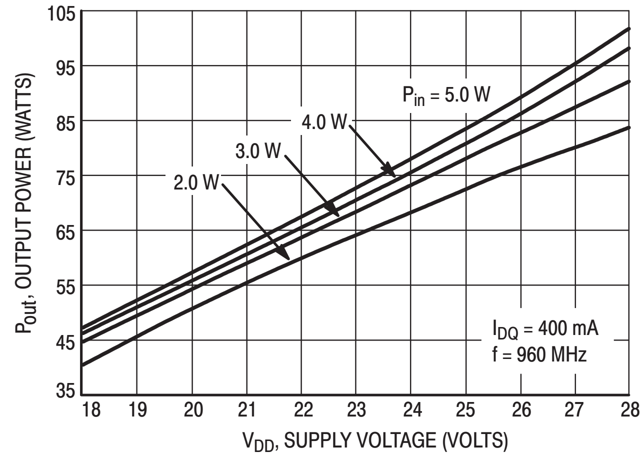


Figure 6. Output Power versus Supply Voltage

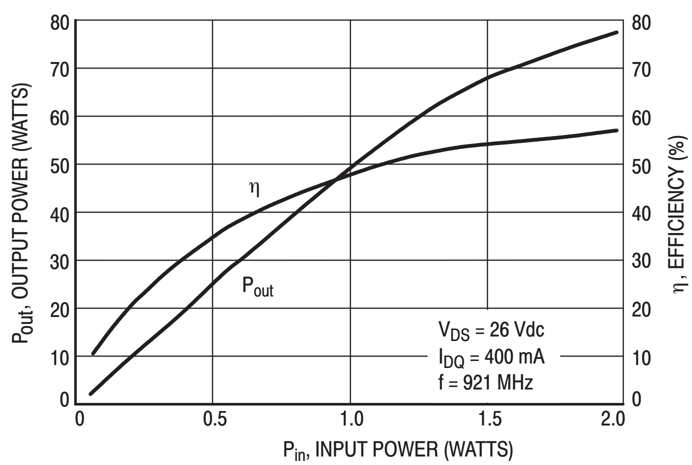


Figure 7. Efficiency and Output Power versus Input Power

TYPICAL CHARACTERISTICS

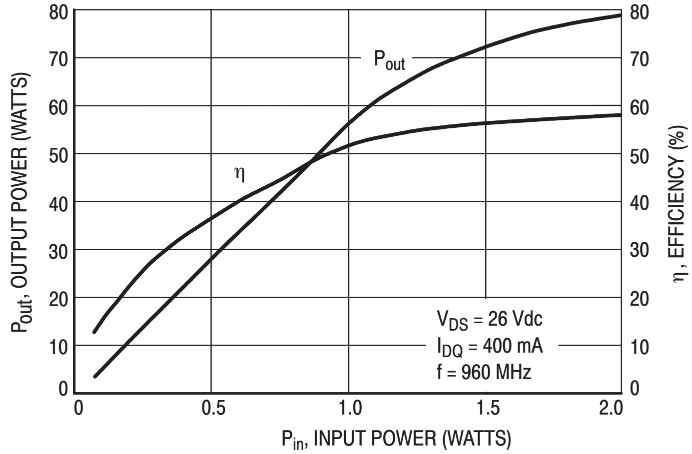


Figure 8. Efficiency and Output Power versus Input Power

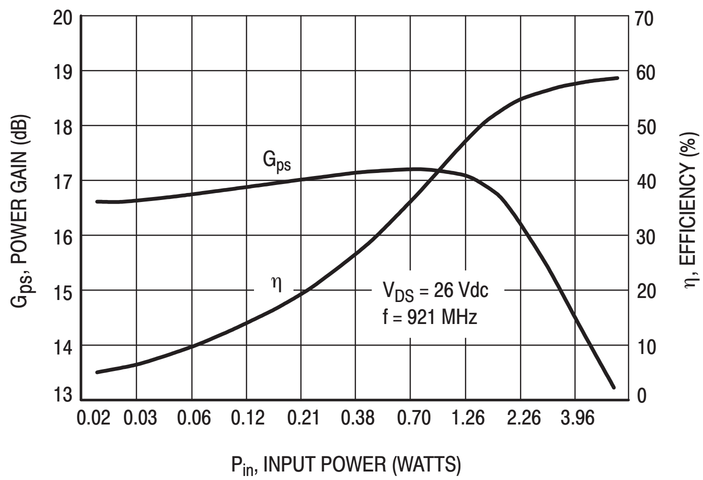


Figure 9. Power Gain and Efficiency versus Input Power

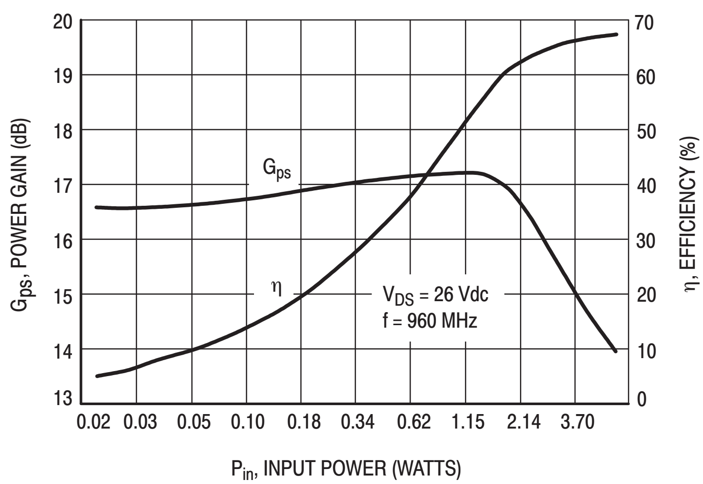


Figure 10. Power Gain and Efficiency versus Input Power

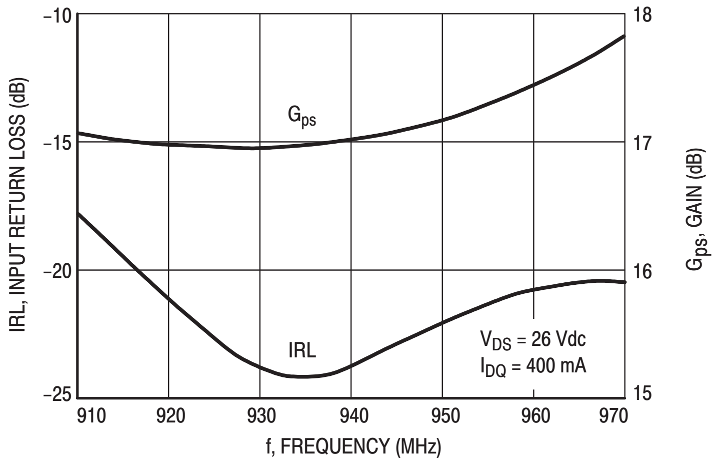
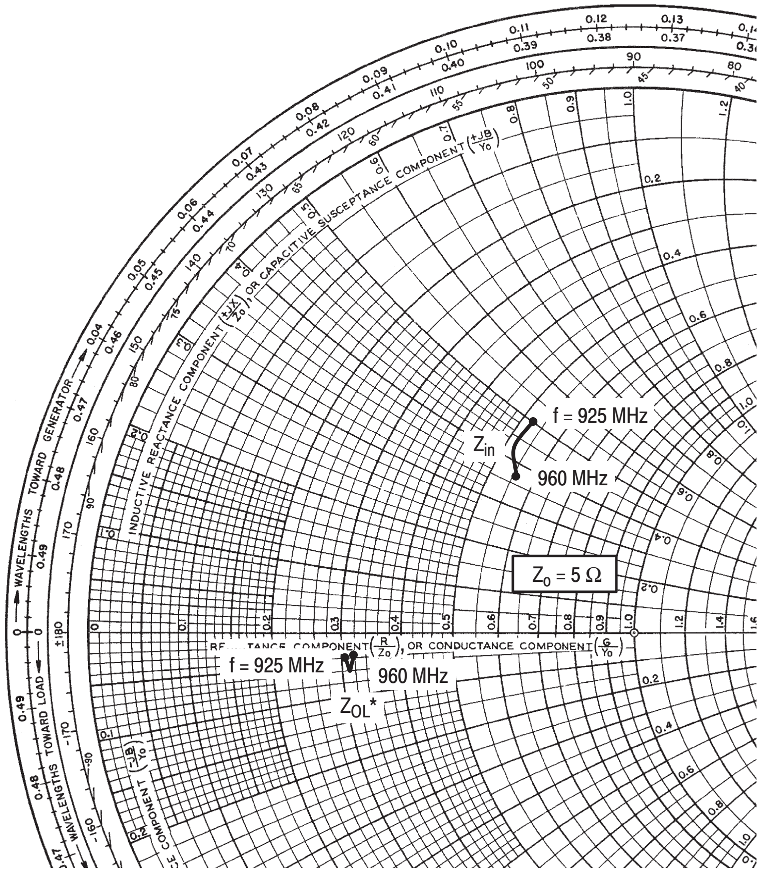


Figure 11. Performance in Broadband Circuit (at Small Signal)



V_{SUPPLY} = 26 Vdc, I_{BIAS} = 400 mA, CW = Room Temperature

f MHz	Z_{in} Ω	$Z_{OL}{}^*$ Ω
925	2.65 + j2.53	1.62 – j0.2
940	2.67 + j2.14	1.56 – j0.34
960	2.85 + j1.87	1.55 – j0.2

Z_{in} = Complex conjugate of source impedance.

$Z_{OL}{}^*$ = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: $Z_{OL}{}^*$ was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

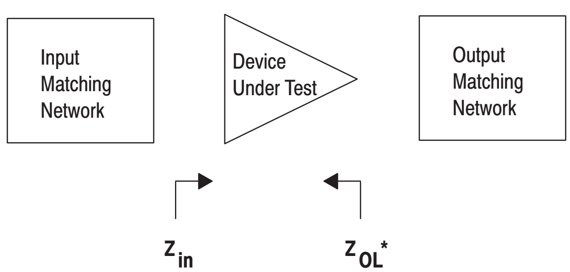
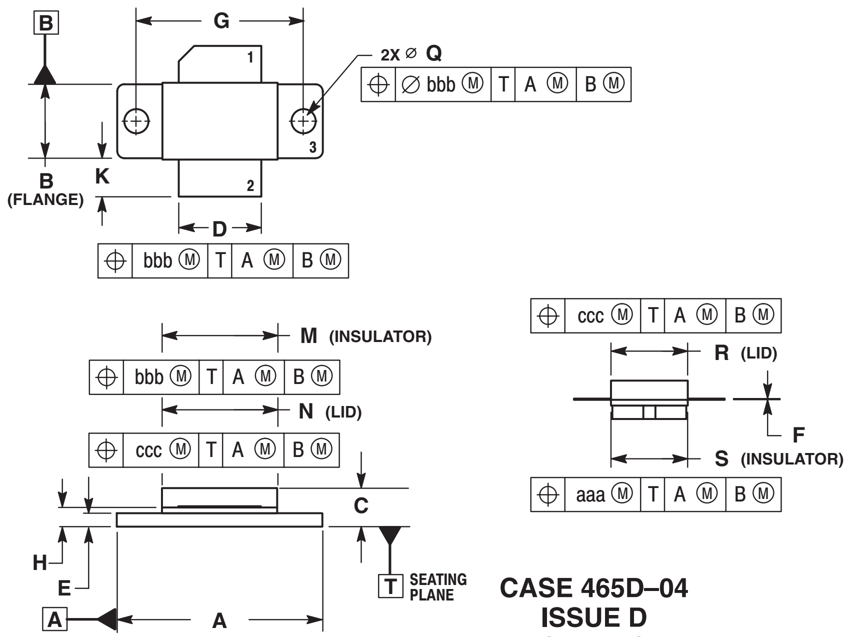


Figure 12. Series Equivalent Input and Output Impedance

PACKAGE DIMENSIONS



CASE 465D–04
ISSUE D
(NI–600)

NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.065	1.075	27.05	27.30
B	0.380	0.390	9.65	9.91
C	0.160	0.205	4.06	5.21
D	0.425	0.435	10.80	11.05
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	0.870 BSC		22.10 BSC	
H	0.096	0.106	2.44	2.69
K	0.190	0.223	4.83	5.66
M	0.594	0.606	15.09	15.39
N	0.591	0.601	15.01	15.27
Q	0.124	0.130	3.15	3.30
R	0.394	0.404	10.01	10.26
S	0.395	0.405	10.03	10.29
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

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