mosaic

Mosaic Semiconductor Inc.

PUMA 2F4002

PUMA 2F4002-90/12/15/20

Issue 1.1 : April 1991

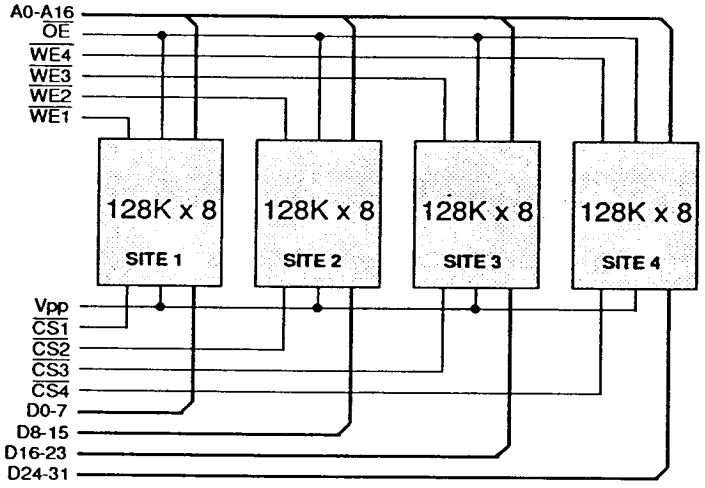
ADVANCE PRODUCT INFORMATION

4,194,304 bit CMOS FLASH Memory Module

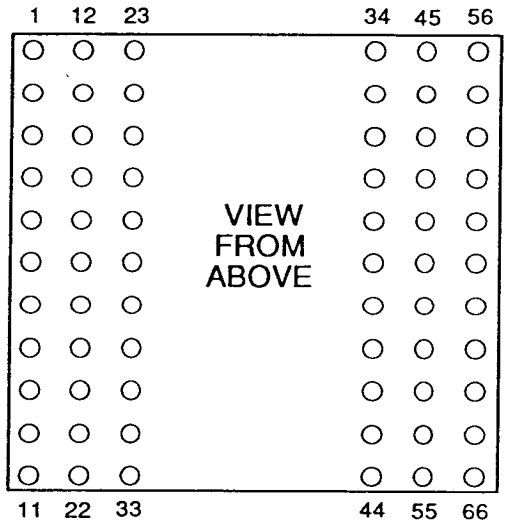
Features

FLASH Eraseable Non-Volatile Memory Module.
User Configurable as 8, 16 or 32 bit wide.
Fast access times of 120/150/200 ns (90ns in development)
Operating Power 726 mW (max), 32 bit mode.
374 mW (max), 16 bit mode.
198 mW (max), 8 bit mode.
Low Power Standby 2.2 mW (max).
Single High Voltage for Erase/Write : V_{PP}=12.0V±5%.
Byte Program (10µs typ) and Chip Erase (2 sec. typ).
More than 10^4 Erase/Write Cycle Endurance.
On board decoupling capacitors.
May be screened in accordance with MIL-STD-883C.

Block Biagram



Pin Definition

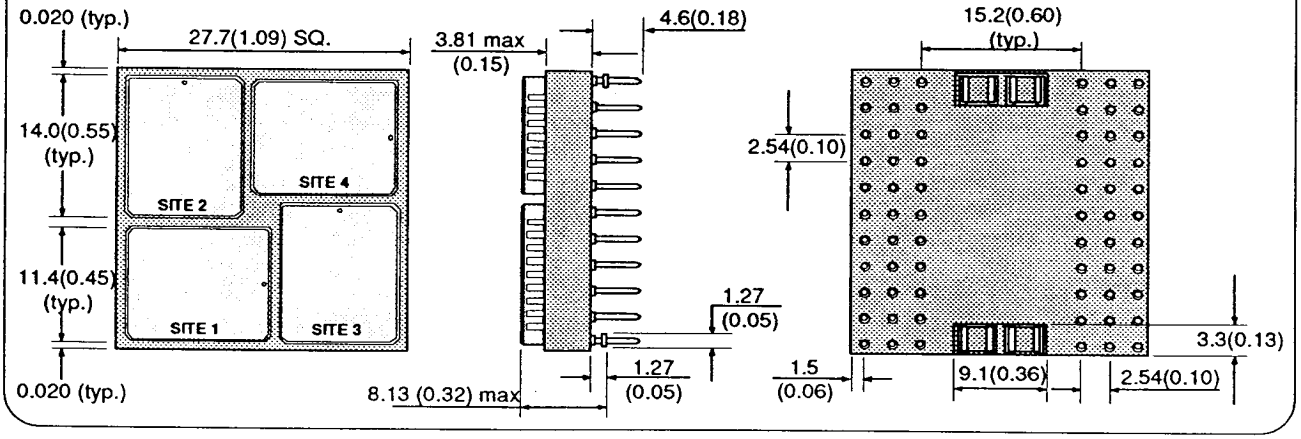


For pinout see page 11

Pin Functions

A0-A16	Address Inputs
D0-D31	Data Input/Output
$\overline{CS1\text{-}4}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{WE1\text{-}4}$	Write Enables
V_{PP}	Write/Erase Input Voltage
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



GENERAL DESCRIPTION

The PUMA 2F4002 is a 4,194,304 bit CMOS FLASH Memory which is configurable as 8, 16 or 32 bit wide output using $\overline{CS1}$-4, allowing flexibillty in a wide range of applications.

FLASH memory combines the functionality of EPROM with on-boad electrical Write/Erasure. The PUMA 2F4002 utilises devices which use a Command Register to manage these functions, allowing fixed power supply during Write/Erase and maximum EPROM compatibilty. During Write cycles, the command register internally latches address and data needed for the Write and Erase operations, thus simplifying the external control circuitry.

FLASH technology reliably stores data even after 10,000 Write/Erase cycles and utilises a single program supply of 12V±5%. Additionally, the interactive program algorithm allows a typical room temperature program time of 2 seconds for the entire module (in 32 bit mode). The typical module erasure time is less than 1 second.

Absolute Maximum Ratings (1)

Temperature Under Bias	T_{OPR}	-55 to +125 °C
Storage Temperature	T_{STG}	-65 to +150 °C
Voltage on Any Pin with respect to GND (2)	V_{T1}	-2.0 to +7.0 V
Voltage on A9 pin with respect to GND (3)	V_{T2}	-2.0 to 14.0 V
Voltage on V_{PP} pin with respect to GND (3)	V_{PT}	-2.0 to +14.0 V
V_{CC} Supply Voltage (2)	V_{CC}	-2.0 to +7.0 V
Output Short Circuit Current (4)	I_{SC}	200 mA

Notes : (1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Minimum DC input voltage is -0.5V. During transitions inputs may undershoot to -2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC}+0.5V, which may overshoot to V_{CC}+2.0V for periods less than 20 ns.

(3) Minimum DC input voltage is -0.5V. During transitions inputs may undershoot to -2.0V for periods less than 20 ns. Maximum DC input voltage is +13.5V, which may overshoot to +14.0V for periods less than 20 ns.

(4) Output shorted for no more than one second. No more than one output shorted at any one time.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Programming Voltage Read	V_{PPR}	-0.5	5.0	12.6	V
Write/Erase/Verify	V_{PPW}	11.4	12.0	12.6	V
Input High Voltage TTL	V_{IH}	2.0	-	V_{CC}+0.5	V
CMOS	V_{IHC}	V_{CC}-0.5	-	V_{CC}+0.5	V
Input Low Voltage TTL	V_{IL}	-0.5	-	0.8	V
CMOS	V_{ILC}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (-I suffix)
	T_{AI}	-55	-	125	°C (-M,-MB suffix)

Capacitance (T_A=25°C,f=1MHz)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Address, $\overline{OE}$	C_{IN1}	V_{IN}=0V	32	40	pF
	V_{PP}	C_{IN2}	V_{IN}=0V	32	48	pF
	Other pins	C_{IN3}	V_{IN}=0V	8	12	pF
Output Capacitance	32 bit	C_{OUT32}	V_{OUT}=0V	8	12	pF
	16 bit	C_{OUT16}	V_{OUT}=0V	16	24	pF
	8 bit	C_{OUT8}	V_{OUT}=0V	32	48	pF

Note: These parameters are calculated, not measured.

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
I/P Leakage Current	Address, $\overline{OE}$, V_{PP}	I_{LI1}	$V_{CC}=V_{CC}$ max, V_{IN}=0V or V_{CC}, $V_{PP}=V_{PPL}$	-	±4	µA
	Other Pins	I_{LI2}	$V_{CC}=V_{CC}$ max, V_{IN}=0V or V_{CC}	-	±1	µA
Output Leakage Current		I_{LO}	$V_{CC}=V_{CC}$ max, V_{OUT}=0V or V_{CC}, 8 bit	-	±4	µA
V_{PP} Read Current		I_{PP1}	$V_{PP}=V_{PPH}$	-	800	µA
Device Identifier Current		I_{ID}	A9=V_{ID}	-	200	µA
V_{CC} Operating Supply Current	32 bit	I_{CC32}	$\overline{CS}=V_{IL}$(1), $\overline{OE}=V_{IH}$, I_{OUT}=0mA, f=8MHz(2)	-	132	mA
	16 bit	I_{CC16}	As above	-	68	mA
	8 bit	I_{CC8}	As above	-	36	mA
V_{CC} Write/Erase Supply Current	32 bit	I_{CC32}	$\overline{CS}=V_{IL}$(1), Write/Erase in progress	-	120	mA
	16 bit	I_{CC16}	As above	-	62	mA
	8 bit	I_{CC8}	As above	-	33	mA
V_{PP} Write/Erase Current	32 bit	I_{PP32}	$V_{PP}=V_{PPH}$, Write/Erase in progress	-	120	mA
	16 bit	I_{PP16}	As above	-	61	mA
	8 bit	I_{PP8}	As above	-	31	mA
Standby Supply Current	TTL levels	I_{SB1}	$V_{CC}=V_{CC}$ max, $\overline{CS}=V_{IH}$(1)	-	4	mA
	CMOS levels	I_{SB2}	$V_{CC}=V_{CC}$ max, $\overline{CS}=V_{IHC}$(1)	-	400	µA
Device Identifier Voltage		V_{ID}	A9=V_{ID}	11.5	13.0	V
V_{PP} Voltage During	Read Only	V_{PPL}	Write/Erase Inhibited if $V_{PP}=V_{PPL}$	0	V_{CC}+2.0	V
	Read/Write	V_{PPH}		11.4	12.6	V
Output Low Voltage		V_{OL}	I_{OL}=2.1mA.	-	0.45	V
Output High Voltage	TTL loading	V_{OH1}	I_{OH}=-2.5mA.	3.8	-	V
	CMOS loading	V_{OH2}	I_{OH}=-100µA.	V_{CC}-0.4	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1}$-4. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) For a single device on the PUMA 2F4002, I_{CC} total = 20mA + 1.6mA/MHz.

(3) Maximum active current is the sum of I_{CC}(I_{CP}) and I_{PP}.

(4) **CAUTION**: the PUMA 2F4002 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

ERASE AND PROGRAMMING PERFORMANCE

Parameter		*min*	*typ*	*max*	*Units*	*Comments*
Erase Times	32 bit	-	0.5	10	sec	Excludes 00_H Programming Prior to Erasure
Program Times	32 bit	-	2	24	sec	Excludes System-Level Overhead
Write/Erase Cycles		10^4	-	-	cycles	Not 100% tested

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V.
* Input rise and fall times: ≤ 10ns.
* Input and Output timing reference levels: 0.8V and 2.0V
* Output load : 1 TTL gate plus 100 pF.

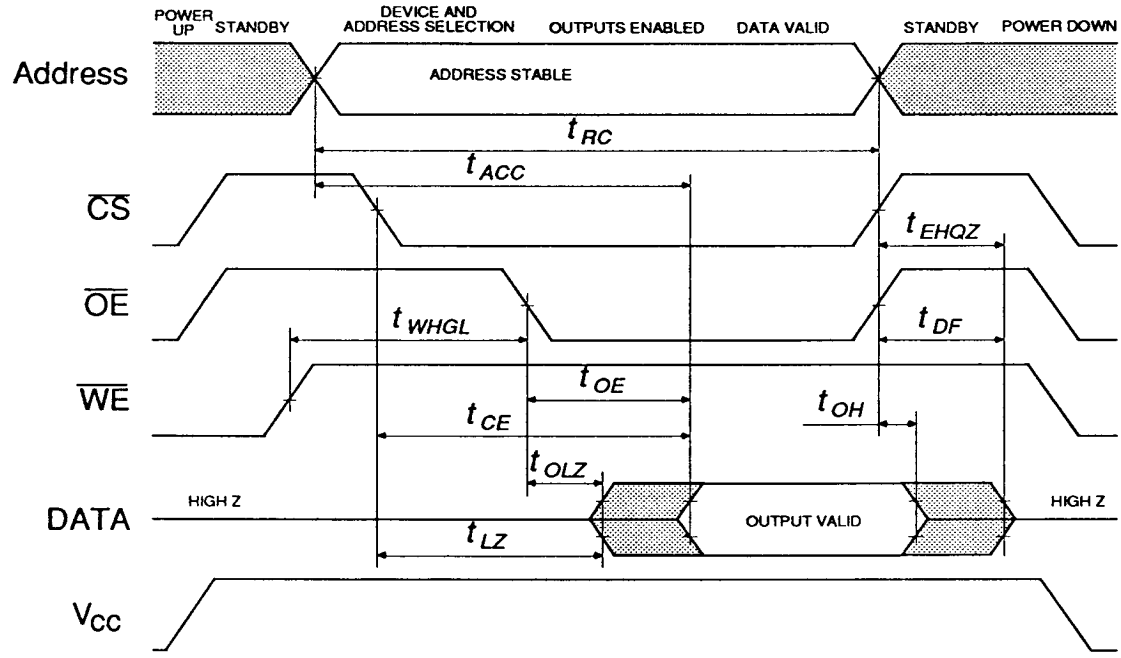
READ

AC Characteristics

Parameter	Symbol	-12 min	-12 max	-15 min	-15 max	-20 min	-20 max	Unit
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns
Chip Select Access Time	t_{CS}	-	120	-	150	-	200	ns
Address Access Time	t_{ACC}	-	120	-	150	-	200	ns
Output Enable Access Time	t_{OE}	-	50	-	55	-	55	ns
Chip Select to Output in Low Z(2)	t_{LZ}	0	-	0	-	0	-	ns
Output Enable to Output in Low Z(2)	t_{OLZ}	0	-	0	-	0	-	ns
Output Disable to Output in High Z(1,2)	t_{DF}	-	30	-	35	-	35	ns
Output Hold Time	t_{OH}	0	-	0	-	0	-	ns
Write Recovery Time	t_{WHGL}	6	-	6	-	6	-	µs

Notes: (1) t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
(2) These parameters are sampled and not 100% tested.

Read Cycle Timing Waveform



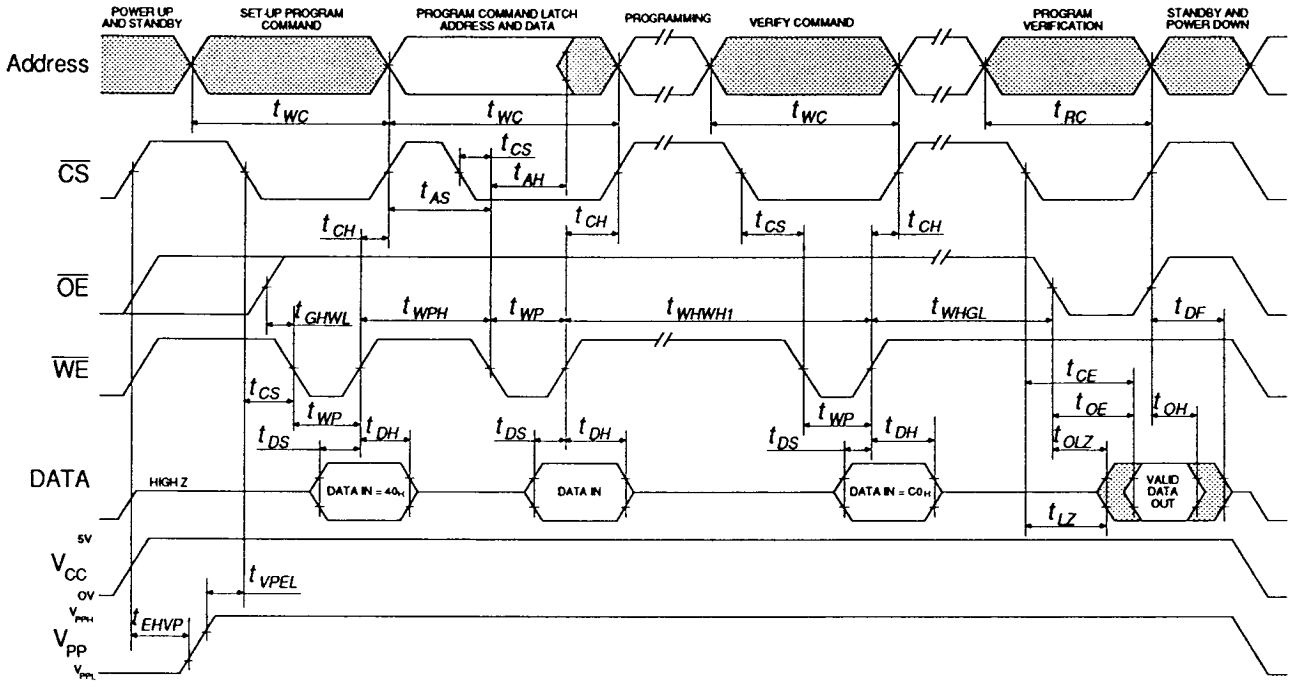
WRITE/ERASE/PROGRAM (1)

AC Characteristics

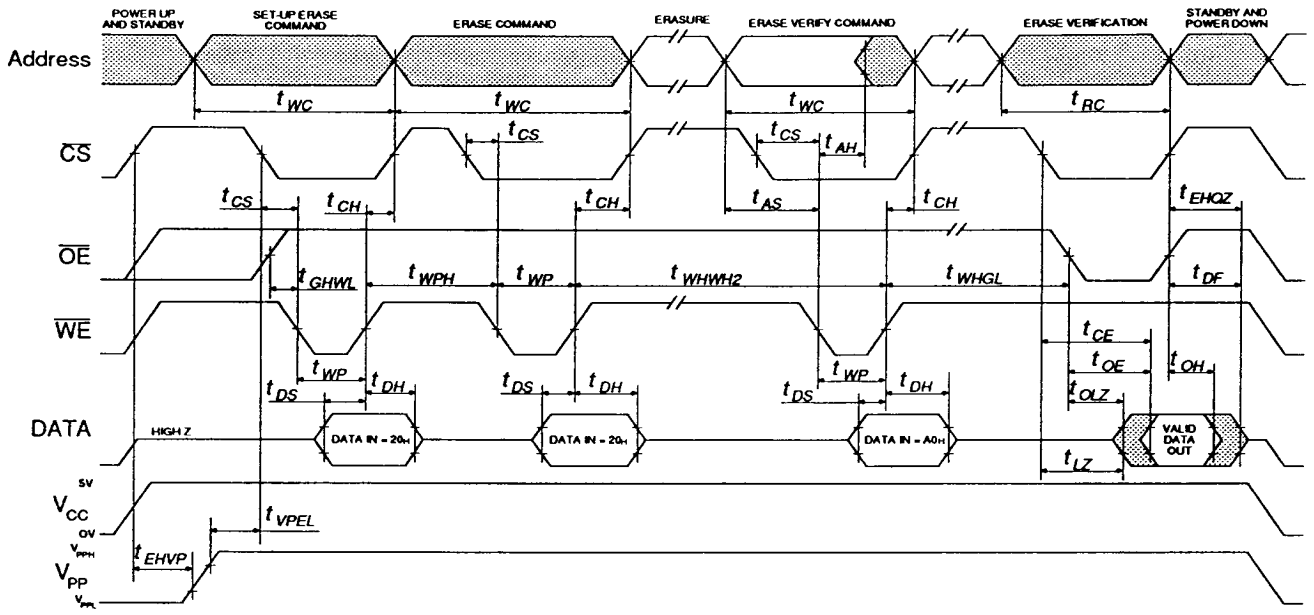
Parameter	Symbol	-12 min	-12 max	-15 min	-15 max	-20 min	-20 max	Unit
Write Cycle Time	t_{WC}	120	-	150	-	200	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Address Hold Time	t_{AH}	50	-	60	-	75	-	ns
Data Setup Time	t_{DS}	50	-	50	-	50	-	ns
Data Hold Time	t_{DH}	10	-	10	-	10	-	ns
Write Recovery Time	t_{WHGL}	6	-	6	-	6	-	µs
Read Recovery Time	t_{GHWL}	0	-	0	-	0	-	µs
Chip Select Setup Time	t_{CS}	0	-	0	-	0	-	ns
Chip Select Hold Time	t_{CH}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	50	-	50	-	50	-	ns
Write Pulse Width High	t_{WPH}	20	-	20	-	20	-	ns
Duration of Programming Operation	t_{WHWH1}	10	25	10	25	10	25	µs
Duration of Erase Operation	t_{WHWH2}	9.5	10.5	9.5	10.5	9.5	10.5	ms
Chip Enable Setup to V_{PP} ramp	t_{EHVP}	100	-	100	-	100	-	ns
V_{PP} Setup Time to Chip Select Low	t_{VPEL}	100	-	100	-	100	-	ns
V_{CC} Setup Time	t_{VCS}	2	-	2	-	2	-	µs
V_{PP} Rise Time	t_{VPPR}	500	-	500	-	500	-	ns
V_{PP} Fall Time	t_{VPPF}	500	-	500	-	500	-	ns

Notes (1) Read timing characteristics during read/write operations are the same as during read only operations. Refer to AC Characteristics for read only operations.

Programming Timing Waveform



Erase Timing Waveform



MODULE DESCRIPTION

When normal TTL/CMOS logic levels are applied to the V_{PP} pin, the module displays normal EPROM Read, Standby, Output Disable and Device Identifier operations. However, when high voltage (V_{PPH}) is applied to V_{PP} the Write /Erase options are available as well as the Read.

BUS OPERATIONS

Read Two control functions are provided, both of which must be logically active to obtain data at the outputs. $\overline{CS}$ selects the module and controls the power, while $\overline{OE}$ gates data from the output pins - see the Read Cycle Timing Waveform for details.

Write Module Write/Erasure are accessed via the command register while V_{PP} is at V_{PPH}. Note that the register itself does not occupy an addressable memory location, but is simply a latch used to store the command and address/data information required to execute the command.

With $\overline{CE}$ and $\overline{WE}$ at V_{IL} the command register is accessed; addresses are latched on the falling edge of WE and data latched on the rising edge of WE. The three most significant register bits (D7- D5) encode the command function while all other bits (D4-D0) must be zero. The exception to this is the Reset command when data FF_H is written to the register and Identifier mode when 80_H or 90_H is written to the register.

Output Disable When $\overline{OE}$ is at V_{IH} the output pins are placed in a high impedance state and output from the module is disabled.

Standby If $\overline{CS}$ is held at V_{IH} the power consumption of the module is substantially reduced because most of the on-board circuitry is disabled. The outputs are placed in a high impedance state (independent of $\overline{OE}$).

If the PUMA 2F40002 module is deselected and placed in Standby mode during Write/Erase and Verify cycles, the module will continue to draw normal active current until the operation is terminated.

Device Identifier Placing a high voltage (V_{ID}) on pin A9 of the module causes the manufacturer and device codes to be output. This can be used to match the correct Write/Erase algorithms to the module.

PUMA 2F4002 Bus Operations

OPERATION		Vpp (1)	A0	A9	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	D0 - D7
READ ONLY	Read	V_{PPL}	A0	A9	V_{IL}	V_{IL}	V_{IH}	Data out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	Manufacturer Identifier(2)	V_{PPL}	V_{IL}	V_{ID} (3)	V_{IL}	V_{IL}	V_{IH}	Data = 01_H
	Device Identifier(2)	V_{PPL}	V_{IH}	V_{ID} (3)	V_{IL}	V_{IL}	V_{IH}	Data = $A7_H$
READ/WRITE	Read	V_{PPH}	A0	A9	V_{IL}	V_{IL}	V_{IH}	Data Out (4)
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A0	A9	V_{IL}	V_{IH}	V_{IL}	Data In (5)

Notes (1) V_{PPL} may be GND, a NC with a resistor tied to GND, or $\leq V_{CC}+2.0V$. V_{PPH} is the programming voltage specified for the device - refer to the DC Characteristics. When $V_{PP}=V_{PPL}$ memory contents can be read but not Written or Erased

(2) Manufacturer and Device codes may also be accessed via the command register. In this mode all addresses except A0 and A9 must be at V_{IL}.

(3) $11.5V \leq V_{ID} \leq 13.0V$

(4) Read operations with $V_{PP}=V_{PPH}$ may access array data or identifier codes (see page 7).

(5) Refer to Command Definition table for valid Data In during a Write operation.

(6) X can be V_{IL} or V_{IH}.

COMMAND DEFINITIONS

With the V_{PP} pin at a low voltage the Command Register contents default to 00_H, enabling Read-only operations. A high voltage on V_{PP} enable Read/Write modes with device operation selected by writing data into the Register - see the Command Definition table for details.

Note that the following descriptions refer to the commands for the PUMA 2F4002 operating in 8 bit mode. The actual data presented to the module will change with the configured word width i.e. for the Erase Verify command of $A0_H$, if the PUMA is in 16 bit mode $A0A0_H$ will be placed on the data bus and in 32 bit mode the data would be $A0A0A0A0_H$.

Read While V_{PP} is high the memory contents can be Read by first writing 00_H into the Command Register. A delay of 6µs is required before reading the first location, but all subsequent Read operations take t_{ACC}. This mode remains enabled until the Command Register contents are altered.

On power up the Register contents will be 00_H, ensuring that the memory contents are not changed during the V_{PP}/V_{CC} power transition. If the V_{PP} pin is hard wired to a high voltage the memory will power up enabled for Read until the Register contents are altered.

Intelligent Identifier In order to use the correct programming and erase algorithms on PROM devices, these parts usually have built in codes to identify manufacturer and specific device. However, to access these codes address line A9 has to be placed at a high voltage, which is not considered good practise and can lead to complications on PCB design.

The PUMA 2F4002 module uses both of these codes to suppliment traditional PROM programming methodology, but the identifiers are accessed through the Command Register without placing a high voltage on A9. Writing 80_H or 90_H into the Register starts this process with a subsequent Read from 00000_H retrieving the manufacturer code of 01_H and a Read from 00001_H giving the device code $A7_H$. To terminate this sequence another valid command must be written to the Register.

Set-up Program/Program Set-up program is a command only operation which prepares the memory for byte programming, initiated by writing 40_H into the command register.

Once Set-up program has been performed, the next $\overline{WE}$ pulse causes data to be latched on the rising edge and the address is latched on the falling edge of this pulse. Internal programming begins on the rising edge and is terminated with the next rising edge of Write Enable used to write the program-verify command.

Program-Verify This module is programmed byte by byte, which can occur sequentially or at random, but the byte just written must be verified.

Writing $C0_H$ to the command register begins this operation, which also terminates the programming operation. The last byte written will be verified; no new address information is required as the previous address is latched. A Read Cycle can now be performed in order to compare the data just written with the byte contents. This process is shown by the Programming Algorithm.

Set-up Erase/Erase Set-up erase is a command only operation which prepares the memory for electrical erasure of all contents, initiated by writing 20_H to the Command Register.

In order to start erasure 20_H must again be written to the register; this two-step sequence ensures that accidental erasure will not occur. Additionally, if the V_{PP} pin is not at a high voltage the memory contents are protected against erasure.

Erase-Verify The Erase command erases all the contents of the memory, but after this operation all bytes must be verified. This is accomplished by writing $A0_H$ to the Command Register, with the address of the byte to be verified supplied as it is latched on the falling edge of the Write-Enable pulse. Reading FF_H from the addressed byte indicates that it is erased. This command must be issued prior to each byte verification to latch its address.

If the data read is not FF_H another erase operation must be performed. Verification can then continue from the address of the last verified byte, and once all bytes have been verified the erase procedure is complete. This process is shown by the Erase algorithm.

The verify operation is halted by writing another valid command e.g. Set-up Program, into the command register.

Reset This command, which consists of two consecutive writes of FF_H, will safely abort either Erase or Program operations after the Set-up commands. Memory contents will not be altered, and a valid command must then be written to place the device in the desired state.

ALGORITHM NOTES

It can be seen that the Programming and Erase algorithms both terminate with the Command Register being loaded with a Read command. If devices on the PUMA 2F4002 are being Programmed/Erased sequentially (i.e. it is configured in 8 bit mode) then at the termination of the sequence all devices which have been accessed must be returned to the Read mode before correct operation can resume.

PUMA 2F4002 Command Definitions

COMMAND	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation (1)	Addr (2)	Data (3)	Operation (1)	Addr (2)	Data (3)
Read Memory(8)	1	Write	X	00_H	Read	RA	RD
Read Identifier Codes(4)	2	Write	X	$80/90_H$	Read	IA	ID
Set-up Erase/Erase(5)	2	Write	X	20_H	Write	X	20_H
Erase Verify (5)	2	Write	EA	$A0_H$	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40_H	Write	PA	PD
Program Verify (6)	2	Write	X	$C0_H$	Read	X	PVD
Reset (7)	2	Write	X	FF_H	Write	X	FF_H

Notes (1) See Bus Operations Table.

(2) IA = Identifier address. 00_H for Manufacturers code and 01_H for device code.
EA = Address of memory location to be read during Erase Verify.
PA = Address of memory location to be programmed.
RA = Address of memory location to be Read.
Addresses are latched on the falling edge of Write Enable pulse.

(3) ID = Data read from location IA during device identification. (Manufacturer = 01_H, Device = $A7_H$)
EVD = Data read from location EA during Erase Verify.
PD = Data to be programmed at location PA. Data is latched on the rising edge of Write Enable.
RD = Data to be read from location RA during Read operation.
PVD = Data to be read from location PA during Program Verify. PA is latched on the Program command.

(4) Following the Read Identifier command, two read operations access the manufacturer and device codes.

(5) See the Erase Algorithm.

(6) See the Programming Algorithm.

(7) The second bus cycle must be followed by the desired command register write.

(8) Wait 6µs after the first Read command before accessing data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.

Parallel Erase If the PUMA 2F4002 is used in 32 or 16 bit mode then two or four devices will be accessed simultaneously. This reduces the total Erase time, but because individual devices will erase at different rates care must be taken that each device is verified separately. When a device is completely erased and verified a masking code should be used to prevent further erasure e.g. writing the Read Command to the appropriate device. Any other devices will continue to Erase until verified.

Timing Delays Four timing delays are associated with the Program and Erase algorithms described:

(1) When V_{PP} first turns on the capacitors on the V_{PP} line cause an RC ramp, the rise time of which is proportional to the number of devices being erased and the capacitance per device. V_{PP} must reach its final value 100ns before any commands are excecuted.

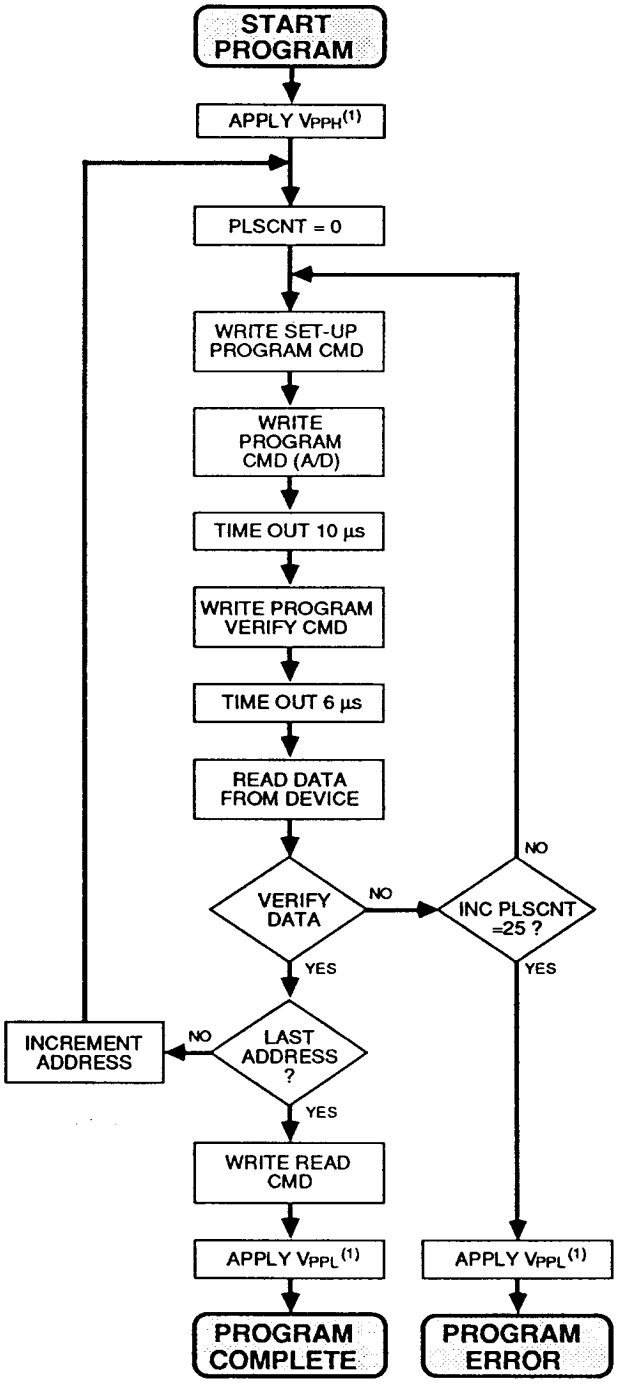
(2) The second timing delay is the erase time pulse width of 10ms, which should be timed by a routine run by the local microprocessor. This operation must be terminated before servicing any system interrupts which may occur during the routine. An Erase/Verify command should be written after each erase pulse, otherwise the device(s) may continue to erase until the memory cells are driven into depletion. A symptom of this over erasure is an error attempting to Write the next time; occasionally it may be possible to recover this situation by programming all of the locations with 00_H.

(3) Each Write pulse width is 10µs, and since the algorithm is interactive each byte is verified after a Write pulse. The program operation must be terminated at the conclusion of the timing routine or prior to sevicing any interrupts which may occur during this operation.

(4) A fourth delay is assocaited with both the Write and Erase algorithms is the Write recovery time of 6µs. In order to improve memory cell operation, an internally generated margin voltage is applied to the addressed cell during Write/Erase Verify. It is during this 6µs delay that the internal circuitry is changing voltage levels between the Erase/Write level and those used for Verify and Read operations. Any attempt to Read the device(s) during this period will result in possible false data appearing on the outputs.

PROGRAMMING ALGORITHM

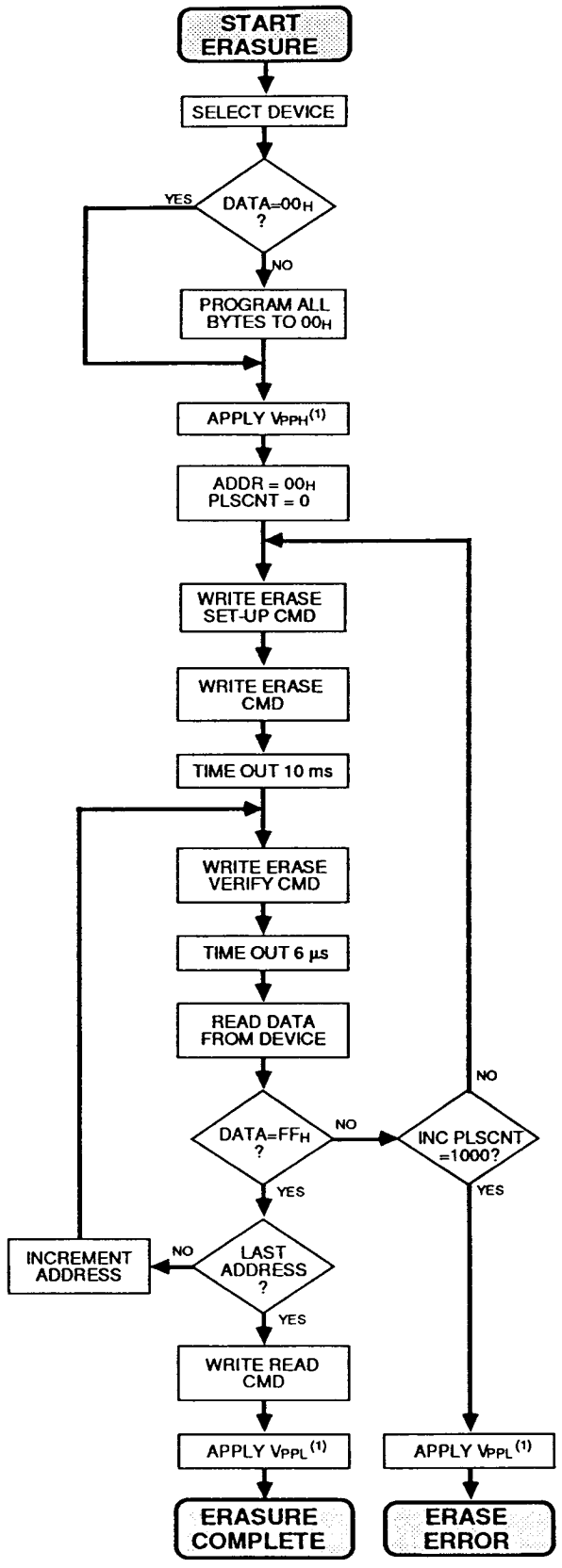
These algorithms **MUST BE FOLLOWED** to ensure proper and reliable operation, and are shown for a single device only.



Notes

(1) See DC Characteristics for the value of V_{PPH}. The V_{PP} supply can be hard wired to the device or switchable.When V_{PP} is switched, V_{PPL} may be GND, NC with a resistor tied to GND or less than V_{CC}+2.0V

ERASE ALGORITHM



DESIGN CONSIDERATIONS

Two Line Control Two Read signals are provided for output control to accommodate large memory arrays, giving the lowest possible memory power dissipation and ensuring bus contention does not occur.

To use this feature efficiently, an address decoder output should drive the $\overline{CS}$ line while the system read signal controls all memories in parallel. This ensures that only enabled memories have active outputs and deselected devices are in the low power Standby condition.

Supply Decoupling Flash memory power-switching characteristics require careful decoupling. Three supply current issues have to be considered - Standby, Active and transient current peaks caused by rising and falling edges of $\overline{CS}$.

Two line control and correct decoupling capacitor selection will help to suppress these transient voltage peaks. This module has four on-board decoupling capacitors of 0.1µF connected between V_{CC} and GND. Additionally, a 0.1µF or larger capacitor should be placed close to the module between V_{PP} and GND.

It is recommended that a 4.7µF electrolytic capacitor should be placed between V_{CC} and GND every two PUMA2F4002 modules. This capacitor will smooth out voltage dips in the supply caused by PCB track inductance and will supply charge to the onboard capacitors as needed.

V_{PP} Trace Because Flash memories are designed to be programmed in situ, the PCB designer must be made aware of the V_{PP} supply trace. This should be made similar to the V_{CC} bus as the V_{PP} pin supplies the memory cell current for Programming and Erase.

Power Up/Down This Flash module is protected against accidental writes caused by power transitions, powering up in the Read only mode. Additionally, by using two step command register sequences this protection is further enhanced. While these functions are sufficient in most cases, it is recommended that V_{CC} should reach a steady state value before V_{PP} is greater than V_{CC}+2.0V, and during power down V_{PP} should be less than V_{CC}+2.0V before lowering V_{CC}.

Connection Table

PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name
1	D8	2	D9	3	D10	4	A14	5	A16
6	A11	7	A0	8	NC	9	D0	10	D1
11	D2	12	$\overline{WE2}$	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A9	18	A15	19	V_{CC}	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	NC	29	$\overline{WE1}$	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A7	38	A12	39	V_{PP}	40	A13
41	A8	42	D16	43	D17	44	D18	45	V_{CC}
46	$\overline{CS4}$	47	$\overline{WE4}$	48	D27	49	A4	50	A5
51	A6	52	$\overline{WE3}$	53	$\overline{CS3}$	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A1
61	A2	62	A3	63	D23	64	D22	65	D21
66	D20								

Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at T_A = +25°C (optional)	100%
Burn-In	Method 1015, Condition D, T_A = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T_A=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per HMP or customer specification	

Ordering Information

PUMA 2F4002MB-12

Speed	90	= Under Development
	12	= 120 ns
	15	= 150 ns
	20	= 200 ns
Temp. range/screening	Blank	= Commercial Temperature
	I	= Industrial Temperature
	M	= Military Temperature
	MB	= Screened in accordance with MIL-STD-883C
Organisation	40002	= 4Mbit array, user configurable
Technology	F	= FLASH MEMORY

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