

Integrated V.22 bis/V.42 bis Data/Fax/Voice Modem Device Set with Telephone Answering Machine (TAM) Support

INTRODUCTION

The merging of the personal computer and telephone is the first step in the evolution of the PC to a full-fledged communications tool. Rockwell modems provide this all-important link between the PC and the desktop or portable phone. Using the RCV229ATF/2-BA modem, the OEM can cost-effectively develop products that, in addition to data and facsimile modem capabilities, support a variety of voice applications such as voice annotation, voice mail, and telephone answering machine (TAM).

The integrated Rockwell RCV229ATF/2-BA data/fax/voice modem device set consists of a modem data pump (MDP) and a microcontroller unit (MCU). Optimized for low-cost desk-top designs, the RCV229ATF/2-BA with OEM-supplied 32k-byte EPROM, provides maximum integration and functionality through a low power, small footprint, minimum supporting component design.

As a data modem, the RCV229ATF/2-BA transmits and receives at communication speeds up to 2400 bps.

As a fax modem, the RCV229ATF/2-BA transceives at Group 3 communication speeds up to 9600 bps, controlled by a built-in EIA-578 Class 1 command interface.

As a voice modem, the RCV229ATF/2-BA uses linear pulse code modulation (PCM) and samples audio data at 11025 or 7200 Hz for record and playback. When DTMF detection is on, the modem will record and playback at 7200 Hz. When DTMF detection is off, the modem will record and playback voice at 11025 Hz. OEM-provided audio control and status register logic supports record and playback functions.

A dedicated DMA channel passes audio data between the host bus and the modem. Latches in the OEM-supplied DMA control logic support DMA data transfer using terminal count signaling, DMA requests, and DMA acknowledgements.

An enhanced "AT" command set, is implemented along with AT+F fax, AT# voice, and caller ID commands.

The modem operates over a dial-up or leased telephone line, provides auto-dial and auto-answer capabilities, and can operate in asynchronous modes.

Full error correction (V.42 LAPM, MNP2-4) and data compression (V.42 bis, MNP 5) capabilities are supported through the Rockwell Protocol Interface (RPI™) and host communication software supporting the RPI. A list of communication software supporting the RPI can be obtained from your local Rockwell sales representative.

The 16C450-compatible interface allows direct connection to a notebook, laptop, or PC-compatible bus without an external UART.

FEATURES

- Data modes
 - CCITT V.22 bis (2400 bps), V.22 (1200 bps),
 V.23 (1200 HDX), V.21 (300 bps)
 - Bell 212A (1200 bps) and 103 (300 bps)
- Group 3 fax modes
 - V.29 (9600/7200 bps) transmit and receive
 - V.27 ter (4800/2400 bps) transmit and receive
 - V.21 Channel 2 (300 bps) transmit and receive
- Voice
 - DMA channel for audio data record and playback
 - Linear PCM sampling at 11025 or 7200 Hz
 - DTMF detection concurrent with record/playback
- Supports Business Audio applications, e.g., digital answering machine (TAM), voice mail, voice annotation, audio file (xxx.WAV) play and record, and text-to-speech
- · Caller ID support
- Enhanced "AT" command set
- Fax Class 1 commands (EIA/TIA 578)
- Error correction (V.42 LAPM, MNP 2-4) and data compression (V.42 bis, MNP 5) supported through RPI™ and host software without additional hardware
- High-speed HDLC commands support Binary File Transfer (BFT) and Error Correction Mode (ECM) facsimile
- · Programmable speaker volume control
- Automatic adaptive/ fixed compromise equalization
- Auto retrain
- Parallel host/DTE interface
 - 16450 UART-compatible interface
 - Support for DMA transfer of audio data
 - Support for audio control and status registers
- Direct connect telco/transformer built-in hybrid
- Full-duplex data mode test capabilities: Analog loop, local digital loop, and remote digital loop
- Half-duplex fax mode test capabilities
- Power-on self test
 - User modification of transmit levels
- Single voltage operation: +5 VDC ± 5%
- Low power CMOS
 - Operating: 245 mW
 - Sleep: 25 mW
- Package options:
 - MCU: 68-pin plastic leaded chip carrier (PLCC) or 80-pin plastic quad flat pack (PQFP)
 - MDP: 68-pin PLCC or 100-pin PQFP

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Data/Fax/Voice Modem

TECHNICAL OVERVIEW

GENERAL DESCRIPTION

The RCV229ATF/2-BA modem is a full-featured. self-contained data/fax solution. Dialing, call progress, and telephone line interface functions are fully supported and controlled through the AT command set and the Audio Control Register.

Data modes perform complete handshake and data rate negotiations. All tone and pattern detection required by the applicable CCITT or Bell standard are supported.

Fax modes support Group 3 fax requirements. Fax data and fax control (V.21 Channel 2, 300 bps) performed by the modem is controlled and monitored through the fax EIA-578 Class 1 command interface. Full HDLC formatting, flag insertion/deletion, and CRC generation/checking is provided.

Modem Data Pump (MDP)

The MDP is a Rockwell single device RC223DP data/fax modem data pump. The MDP includes both digital signal processor and integrated analog functions.

Digital Signal Processor (DSP). The DSP performs the digital signal processing and line control functions.

integrated Analog (IA). The IA includes transmitter, receiver, and telephone line interface sections. The transmitter provides transmitter digital-to-analog (D/A) conversion, bandsplit and lowpass filtering, guard tone generation, and transmit level attenuation. The receiver provides automatic gain control (AGC), bandsplit filtering, and analog-to-digital (A/D) conversion. The telephone interface circuitry provides off-hook and caller ID relay drivers.

Microcontroller (MCU)

The MCU is a Rockwell C19 microcomputer. The MCU connects to the host/DTE via a 16450 UART-compatible parallel microcomputer bus. Interface signals are provided to connect to external DMA control logic and DMA control and status registers which also connect to the parallel microcomputer bus. The MCU connects to the modem data pump via dedicated lines and an external bus.

MCU Firmware

The RCV229ATF/2 MCU firmware performs processing of general modem control; AT, AT+F, and AT#V command: audio control and status register; and DTE interface functions. The MCU firmware is provided by Rockwell in object code form for the OEM to program into an external 32k x 8 EPROM.

SUPPORTED INTERFACES

The major hardware signal interfaces of the RCV229ATF/2 modem device set are illustrated in Figure 1.

Parallel DTE/Host Interface

Eight bidirectional data lines (HD0-HD7), three address input lines (HA0-HA2, three control inputs (HCS, HRD, and HWT), a host interrupt output (HINT), and a reset input (RESET) are supported. A 16C450 UART-compatible parallel interface is provided.

DMA Control Logic Interface

Two 8-bit data latches are supported to transfer audio data via direct memory access (DMA) between the host bus and memory connected to the modem external bus. The DMA Read Latch transfers audio playback data from the host bus and the DMA Write Latch transfers audio record data to the host bus. Two D-flip-flops are also supported: one to control the DMA request to the host bus and one to generate an interrupt request to the MCU when the terminal count of the DMA transfer is complete.

Four dedicated signals are supported: a DMA latch chip select output (ES3) to enable latch operation, DMA enable and DMA request outputs, and a terminal count interrrupt input.

Audio Control and Status (C/S) Registers Interface

Two 8-bit audio control and status registers are supported. The Audio Control Register (ACR) is written by the host to enable record, playback, speaker, and handset functions. select 11.025 kHz or 7.2 kHz sampling rate, and four levels of speaker volume. The Audio Status Register (ASR) is written by the modem to report DTMF enable/disable. busy/idle, sample overrun, and terminal count conditions.

Three dedicated signals are supported: an audio C/S chip select (ES2) output to enable register operation and C/S read and C/S write status inputs to determine host read and write status.

MCU External Bus Interface

The MCU external bus connects to the MDP, ROM, RAM, the DMA latches, and the audio C/S registers The bus supports eight dedicated address line outputs (A0-A3 and A12-A15), eight multiplex bidirectional data lines and address line outputs (A4/D0-A11/D7), and three control outputs (ALE, READ, and WRITE).

Line Interface

MDP. The MDP connects to the line interface circuitry via a receive analog input (RXA), two transmit analog outputs (TXA1 and TXA2), two relay driver outputs (CALLID and OH), and a ring (RING) input. The CALLID and OH relay outputs may be used to drive Caller ID and voice relays, respectively.

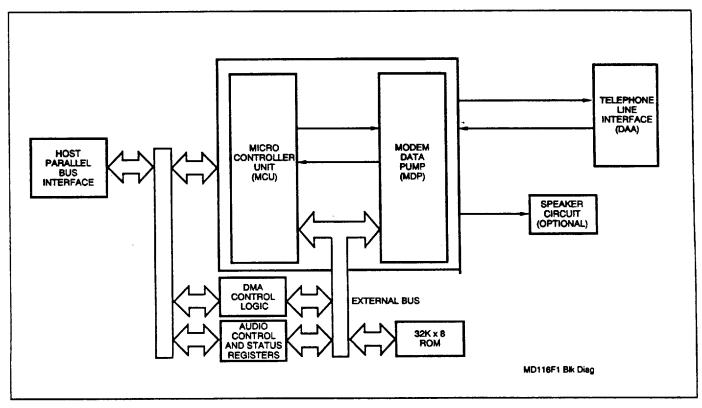


Figure 1. RCV229ATF/2-BA Modem Functional Interface

MCU. The MCU provides two relay control outputs (LINE and POWER) to the line interface. When a line connection does not exist, the LINE output can be used to control a relay which disconnects the line from the hanset and the POWER output can be used to control a relay which connects power to the handset. The MCU also accepts ring (RING) and loop current sense (LCS) signals from the line interface.

Speaker Interface

An interface to an OEM-supplied speaker circuit is provided. The speaker can be used to monitor call progress. The AT Ln command can be used to adjust the volume.

CONFIGURATIONS AND LINE RATES

The supported modern configurations and telephone line rates are listed in Table 1.

HOST/DTE RATES

Data Modem Modes

Automatic Speed/Format Sensing

The modem can automatically determine the speed and format of the data coming into the modem from the DTE. The modem senses speeds of 300, 1200, 2400, 4800, 9600, and 19200 bps and the following data format:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Character Length (No. of Bits)
None	8	1	10

Fax Mode

In fax modes, the DTE rate is 19200 bps.

AT COMMANDS

The modem supports data modem, fax class 1 and voice commands and S Registers (see Tables 2 and 3) depending on the modem model.

Data Modem Operation. Data modem functions operate in response to AT commands when +FCLASS=0.

Fax Modem Operation. Facsimile functions operate in response to fax class 1 commands when +FCLASS=1.

Voice Operation. Voice mode functions operate in response to voice commands when #CLS = 8.

Table 1. Telephone Line Connection Speed Options

Configuration	Data Rate (bps)
Data Mode	
V.22 bis	2400 or 1200
V.22	1200
V.21	0-300
Bell 212A	1200
Bell 103	300
Fax Mode	
V.29	9600 or 7200
V.27 ter	4800 or 2400
V.21 Channel 2	300

AT Command Format

AT commands are interpreted via the parallel host interface. Each command line must start with the AT prefix and be terminated with a carriage return (CR). Several commands may be included on one command line. A command line may contain up to 40 characters excluding the AT prefix and the terminating CR. A separator is not required between data commands. A semicolon (;) separator is required between fax commands.

DATA MODEM OPERATION

Dialing

DTMF Dialing. DTMF (dual tone multi-frequency) dialing using DTMF tone pairs is supported in accordance with CCITT Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Blind Dialing. Blind dialing allows the modem to dial in the absence of a dial tone. The calling unit waits the number of seconds specified in the S6 register (minimum 2 seconds) after going off-hook before reading the dial string initiating the dialing sequence. Blind dialing can be enabled by issuing the ATX0, ATX1, or ATX3 command.

Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

Call Progress Tone Detection

Ringback, equipment busy, and progress tones can be detected in accordance with the applicable standard.

Answer Tone Detection

Answer tone detection can be detected over the frequency range of 2100 \pm 40 Hz in CCITT modes and 2225 \pm 40 Hz in Bell modes.

Ring Detection

A ring signal can be detected from a TTL-compatible 15.3 Hz to 68 Hz square wave input.

Billing Protection

When an incoming call is answered, both transmission and reception of data are prevented for at least 2 seconds after the modern transfers to the off-hook state to allow transmission of the telephone company's billing signal.

Table 2. "AT" Command Set Summary

Basic	
AT	Attention Code.
A	Go off-hook and attempt to answer a call.
À	Re-execute command.
B0	Select V.22 2100 Hz answer tone.
B1	Select Bell 212A 2225 Hz answer tone.
B3 C1	Select V.23 modulation. Return OK message.
Dn	Dial Modifier.
E0	Turn off command echo.
E1	Turn on command echo.
F1	On-line character echo disabled.
H0 H1	Initiate a hang-up sequence. If on-hook, go off-hook and enter command mode.
l 10'	Identify product via product code.
iii	ROM checksum request.
12	ROM checksum status request.
13	ROM part number and revision level request.
14 15	OEM string request. PROM revision level request.
LO	Set low speaker volume.
L1	Set low speaker volume.
12	Set medium speaker volume.
L3	Set high speaker volume.
M0 M1	Turn speaker off. Turn speaker on during handshaking, and turn
'' ''	speaker off while receiving carrier.
M2	Turn speaker on during handshaking and
1	while receiving carrier.
M3	Turn speaker off during dialing and receiving carrier, and turn speaker on during answering.
00	Go on-line.
01	Go on-line and initiate a V.22 bis retrain sequence.
P	Force pulse dialing.
Q0	Allow result codes to DTE.
Q1 Sn	Inhibit result codes to DTE. Select S Register as default.
Sn?	Return the value of S Register n.
T	Force DTMF dialing.
V0	Report short form (terse) result codes.
V1 X0	Report long form (verbose) result codes. CONNECT result codes are enabled, CONNECT
Λ0	XXXX result codes are disabled, and busy signal
	and dial tone are not detected.
X1	The modern blind dials, CONNECT XXXX result
	codes are enabled, and busy signal and dial tone
X2	are not detected. The modern waits for dial tone before dialing,
~	CONNECT XXXX result codes are enabled, and
1	busy signal is not detected.
ХЗ	The modern blind dials, CONNECT XXXX result
	codes are enabled, and the modern sends the
X4	BUSYresult code if busy signal is detected. The modern waits for dial tone before dialing,
^7	CONNECT XXXX result codes are enabled, and the
1	modern sends the BUSY result code if busy signal
1	is detected.
Y0	Disable long space disconnect before on-hook. Enable long space disconnect before on-hook.
Y1 Z0	Restore stored profile 0 after warm reset.
Z1	Restore stored profile 1 after warm reset.
+++	Escape code sequence.
?	Returns last addressed S Register.
	

Table 2. "AT" Command Set Summary (Cont'd)

Command	i Function
+Hn	Rockwell Protocol Interface (RPI) Enable.
Dial Modifier	Function
P	Select pulse dialing.
	Dial Stored Telephone Number (n=0:1)*.
	Touch Tone Dial.
	Wait for Dial Tone.
•	Return to Idle State.
_	Wait for silence.
•	Flash.
	Pause.
0-9	DTMF digits 0 to 9.
A-D	DTMF digits A, B, C, and D.
#	The 'gate digit' (tone dialing only).
*	The 'star' digit (tone dialing only).
& Comman	d Function
	Force RLSD active regardless of carrier state.
	Allow RLSD to follow the carrier state.
&DO	The modern ignores DTR.
&DI	Asynchronous escape.
&D2	The modern hangs-up and autoanswer is disabled.
&D3	The modern performs soft reset.
&F	Load factory defaults.
&G0	No guard tone selected.
&G1	No guard tone selected.
&G2	1800 Hz guard tone selected.
&LO	Select dial-up operation.
&MO	Asynchronous Communications Mode selected.
&Pn	Make to Break Ratio Selection.
&Q0	Select direct asynchronous mode.
&S0	DSR is always active.
&S1	DSR is limited active.
&TO	Terminate any test in progress.
&T1	Initiate local analog loopback.
&T3	Initiate local digital loopback.
&T4	Allow remote digital loopback.
&T5	Disallow remote digital loopback request.
&T6	Request remote digital loopback without self-test.
&T7	Request remote digital loopback with self-test.
&T8	Initiate local analog loop with self-test.
&V	Display current configurations.
&X0	Select internal timing for the transmit clock.
%	
Comman	d Function
%Dn	DTMF level attenuation
%Ln	Transmit level attenuation
%J	Load secondary defaults

Table 2. AT Command Set Summary (Cont'd)

#		
Comman		Function
#CLS	Select data	, fax, or voice.
1	0	Data modem
ļ	1	Fax modem
I	8	Voice
#VTD=i		detection/report enable (i = hex value
l		g functions enabled/disabled for voice).
ŀ	Bit 0	DTMF tone
ł	Bit 1	V.25 1300 Hz tone
	Bit 2	T.30 1100 Hz tone
	Bit 3	V.25/T.30 21:00 Hz tone
	Bit 4	Bell 2225 answer tone
	Bit 5	Call progress tone and cadence
	Bit 6-7	Reserved
Voice me	odem respor	
	0-9, A-D, #,	
	b	Busy tone detected
	C	Calling tone detection
	d	Dialtone detected
	e	European data modem calling
		tone detected
	h	Handset hang up detected
	S	Silence detected
	t	Handset out of cradle detected
	×	ептог
#CID		er ID detection and select report format.
	Ō	Disable caller ID (default)
	4	Enable formatted caller ID
Fax Cor	nmand	Function
+FCLAS	S=n	Select Service Class
+F <com< td=""><td>mand>?</td><td>Report Active Configuration</td></com<>	mand>?	Report Active Configuration
	mand>=?	Report Operating Capabilities
+FAA=n		Data/Fax Auto Answer
+FF		Enhanced Flow Control
+FTS=n		Stop Transmission and Wait
+FRS=n		Receive Silence
+FTM=n		
+FRM=n Receive Data		
+FTH=n		Transmit Data with HDLC Framing
+FRH=n		Receive Data with HDLC Framing
+ <u>FRT</u> n		Receive Test Data
+FTTn=r	n	Transmit Test Data
		

Table 3. S Register Summary

Register	Function
SO	Rings to Answer On
S1	Ring Counter
S2	Escape Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Backspace Character
S6	Wait Time for Dial Tone
S7	Wait Time for Carrier
S8	Pause Time for Dial Delay Modifier
S9	Carrier Detect Response Time
S10	Carrier Loss Disconnect Time
S11	DTMF Dialing Speed
S12	Escape Code Guard Time
S14	Bit Mapped Options Register
S16	Test Mode Bit Mapped Options
S17	Fax Mode Null Byte Timer
S18	Test Timer
S19	Bit Mapped Options Register
S20	Fax Mode Inactivity Timer
S21	Bit Mapped Options Register
S22	Bit Mapped Options Register
S23	Bit Mapped Options Register
S24	Sleep Mode Inactivity Timer
S 25	Delay to DTR Off
S26	RTS to CTS Delay
S27	Bit Mapped Options Register
S28	Bit Mapped Options Register
S29	Flash Duration

Connection Speeds

The possible modem to modem connection data modes/speeds are Beil 103 300 bps. Bell 212A 1200 bps. V.21 300 bps, V.22 1200 bps, and V.22 bis 2400 bps. Data rate selection is determined by the speed of the originating and answering modems per the appropriate AT command as follows:

AT Command: B0

A. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.	Connect Speed Based on			
Originate Modem	Answer Modem Rate (bps)			
Rate (bps)	300	1200	2400	
300	300	300	300	
1200	300	1200	1200	
2400	300	1200	2400	

AT Command: B1

	Conne	ct Speed Ba	sed on	
Originate Modem	Answer Modem Rate (bps)			
Rate (bps)	300	1200	2400	
300	300	300	300	
1200	1200	1200	1200	
2400	1200	1200	2400	

Transmit Tones

Answer Tone: An answer tone of 2100 Hz (V.22 bis, V.22, or T.30) or 2225 Hz (Bell 212A or 103) is generated.

Guard Tone: An 1800 Hz guard tone can be generated in all PSK data modes.

Calling Tone: A 1100 Hz (0.5 seconds on, 3 seconds off) calling tone (T.30) is generated in the originate fax mode.

Modem Handshaking Protocol

An abort call timer is initiated when the last digit is dialed and is reset when the modern detects either answer tone or busy. If a tone is not detected during the time specified in the S7 register (default is 30 seconds), the modem aborts the call attempt.

Receive Level

The receiver satisfies performance requirements for a received signal from -9 dBm to -43 dBm. The carrier detect is ON at -43 dBm and OFF at -48 dBm with a minimum of 2 dB hysterisis.

Receiver Tracking

The modem can accommodate carrier frequency offset up to ±7 Hz, and a transmit timing error of ± 0.01% (V.22 bis or V.27 ter) or ± 0.02% (V.22 or Bell 212A).

Equalization

Automatic adaptive equalization and fixed compromise equalization compensate for line distortions and minimize the effects of intersymbol interference.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler satisfying the applicable CCITT or Bell requirements.

Transmit Level

The transmit level is adjustable (see S91 in Table 4).

DATA MODE

Data mode exists when a telephone line connection has been established between moderns and all handshaking has been completed.

Escape Sequence Detection

The S2 register holds the decimal value of the ASCII code used for the escape character. The default character is a '+'. Detection of the escape sequence can be disabled by setting the S2 register to a value greater than 127. When the escape sequence is executed, the escape characters are also transmitted to the telco line in all modes.

BREAK Detection

The modern can detect a BREAK signal from either the DTE or the remote modem. The \Kn command determines the modern response to a received BREAK signal.

Telephone Line Monitoring

Loss of Carrier. If carrier is not detected for time specified in the S10 register, the modern disconnects from the line.

Receive Space Disconnect. If selected by the ATY1 command, the modern disconnects after receiving 1.6 seconds ± 10% of continuous SPACE.

Send Space on Disconnect. If selected by the ATY1 command, the modem sends 4 seconds ± 10% of continuous SPACE If DTR goes OFF or if ATH is issued.

Retrain

The modem may lose synchronization with the received line signal under poor line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modern continues to retrain until an acceptable connection is achieved or until 30 seconds elapse which will result in telephone line disconnect.

FAX MODE

Fax Commands

In the fax mode, the on-line behavior of the modem is different compared to the data (non-fax) mode. After dialing, the modem behaves as controlled by the fax commands. Some AT commands are still valid but may operate differently than in the data mode.

Fax Mode

The possible modem to modem connection fax modes are V.21 Channel 2, V.29, and V.27 ter depending on the selected configuration.

Fax modes are negotiated as defined in T.30 and are implemented by AT+F commands. The AT+FCLASS=1 command causes entry into the fax mode from the data mode. Most other fax class 1 commands, which start with the AT+F prefix, are valid only in the fax mode. All data commands are valid in the fax mode except A/, On, &Tn, and the escape sequence (+++). The AT+FCLASS=0 command terminates the fax mode and causes entry into the data mode.

Fax Mode Buffers. Each terminal and modem buffer contains 100 bytes. For the modem buffer, the high water mark is reached when the buffer is 80% full (80 characters) and the low water mark is reached when the buffer is 20% full (20 characters).

Data/Fax Auto Answering

The modem can automatically determine if the incoming call is from a data or fax modem, make the appropriate connection, and inform the DTE of the connection type.

LOW POWER SLEEP MODE

To conserve power, the modem has a sleep (power down) mode. If enabled by the IDLEN0 and IDLEN1 inputs, sleep mode is entered whenever the modem is inactive. The sleep mode indicator output, SLEEP, is provided to allow external circuits to be powered down when the modem is in sleep mode.

DIAGNOSTICS

Modem diagnostics comply with EIA TR30.2. Diagnostics are performed in response to AT &T commands.

Analog Loopback. Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

Analog Loop Self Test. An internally generated test pattern of alternating 1s and 0s (reversals) is sent to the modern. An error detector within the modern checks for errors in the string of reversals.

Remote Digital Loopback (RDL). Data from the local DTE is sent to the remote modem which loops the data back to the local DTE.

Remote Digital Loopback with Self Test. An internally generated pattern is sent from the local to the remote modern which loops the data back to the local modern.

Digital Loopback. When digital loop is requested from the local DTE, two data paths are set up in the local modem. Data from the local DTE is looped back to the local DTE (path 1) and data received from the remote modem is looped back to the remote modem (path 2).

POWER ON RESET DIAGNOSTICS

Upon power on, or receipt of the ATZ command, the modem performs diagnostic testing.

HARDWARE INTERFACE SIGNALS

The modem hardware interface signals are shown in Figure 2.

MCU pin assignments are listed in Table 5 and shown in Figure 3 for the 68-pin PLCC and are listed in Table 6 and shown in Figure 4 for the 80-pin PQFP.

MDP pin assignments are listed in Table 7 and shown in Figure 5 for the 68-pin PLCC and are listed in Table 8 and shown in Figure 6 for the 100-pin PQFP.

The MCU and MDP hardware interface signals are defined in Tables 9 and 10, respectively.

Digital and analog electrical characteristics for the hardware interface signals are listed in Tables 11 and 12, respectively.

The modem device current and power requirements are listed in Table 13.

The absolute maximum ratings are listed in Table 14.

Table 15 shows the parallel interface registers and the corresponding bit assignments.

Table 16 shows the audio control and status registers and corresponding bit assignments.

A schematic for a typical application circuit is shown in Figure 7.

ADDITIONAL INFORMATION

The RCV229ATF/2-BA Designer's Guide (Order No. 1026) provides detailed interface information. The RC229ATF AT Command Reference Manual (Order No. 1027) provides detailed AT command and S register information.



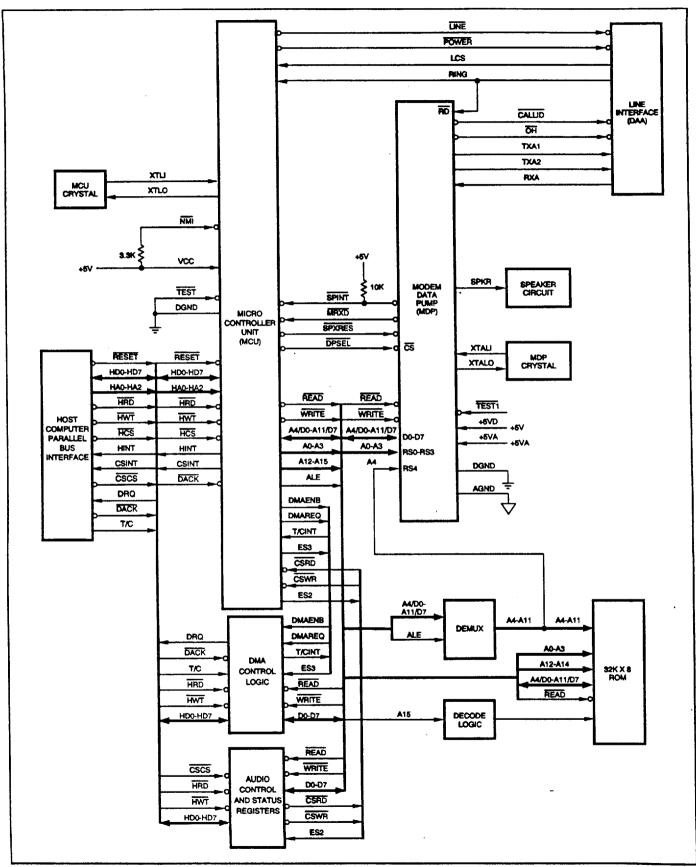


Figure 2. RCV229ATF/2-BA Interface Signals

Table 5. MCU Signals - 68-Pin PLCC

Pin No.	MCU Signal	VO Type	RCV229ATF/2 Signal
1	PB0		NU (Note 5)
2	PB1	ا 🔒 ا	NU (Note 5)
3 4	PB2 PB3	IA IA	CSRD RING
5	PB4	OÃ	POWER
6	PB5	•	NU (Note 5)
7	PB6	1	NC
8	PB7	OA	HINT
9 10	A13 WT	OA OA	A13 WRITE
11	RD	OA	READ
12	ALE	OA	ALE
13	XTLI	IE	XTU
14	XILO	OE	XTLO
15 16	NMI VSS2	GND	NU (Note 5) DGND
17	VSS1	GND	DGND
18	PCO	IA/OA	HD0
19	PC1	IA/OA	HD1
20	PC2	IA/OA	HD2
21 22	PC3 PC4	IA/OA IA/OA	HD3
23	PC5	IAVOA	HD4 HD5
24	PC6	IA/OA	HD6
25	PC7	IA/OA	HD7
26	SYNC		NC
27	PD0	I IA	HAO
28 29	PD1 PD2	IA IA	HA1 HA2
30	PD3	^	NC_
31	PD4	I IA	HČS
32	PD5	IA	HWT
33	PD6	IA	HRD
34 35	PD7	IA I	DACK
36	PA0 PA1	OA OA	DMAREQ DMAENB
37	PA2	I ÖÄ	CSINT
38	PA3	ΪÂ	CSWR
39	PA4	OA	LINE
40 41	PA5 PA6	I IA I	LCS
42	PA0 PA7	I IA	T/C INT SPINT (Note 6)
43	A15	ÖÄ	A15
44	PE0/ES1	OA	NC
45	PE1/ES2	OA	ES2
46	PE2/ES3	OA	ES3
47	PE3/ES4	OA	DPSEL
48 49	RES TEST	IC	RESET TEST (Note 4)
50	VCC	PWR	VCC(+5V)
51	VSS3	GND	DGND
52	A4/D0	IA/OA	A4/D0
53	A5/D1	IA/OA	A5/D1
54 55	A6/D2 A7/D3	IA/OA IA/OA	A6/D2 A7/D3
56	A8/D4	IAVOA	A8/D4
57	A9/D5	IA/OA	A9/D5
58	A10/D6	IAVOA	A10/D6
59	A11/D7	IA/OA	A11/D7
60 61	A14 PF0/A0	OA OA	A14
62	PF1/A1	I OA I	A0 A1
63	PF2/A2	I ÖÄ	A2
64	PF3/A3	QA	A3
65	PF4/A12	OA	A12
66 67	PF5		NC CRYDEC
67 68	PF6 PF7	MI	SPXRES NC
- 55		<u> </u>	110
Notes:			
1.	MI = Modern interco		diagana askad dan ant
2. NC = No connection; leave pin disconnected (open).			

- NU = Not used; connect as noted. Connect to GND. Connect to +5 VDC through 3.3 KΩ. Connect to +5 VDC through 10 KΩ.

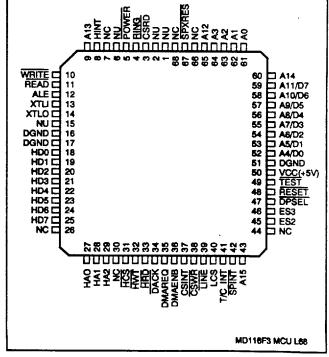


Figure 3. MCU Signals - 68-Pin PLCC

Table 6. MCU Signals - 80-Pin PQFP

	MOUSI		
Pin No.	MCU Signal NC	I/O Type	RCV229ATF/2 Signal
1 2	PE0/ES1	OA	NC
3	PE1/ES2	OA	ES2 ES3
5	PE2/ES3 PE3/ES4	OA OA	DPSEL
6	RES	IC	RESET
7 8	TEST VCC	PWR	TEST (Note 4) VCC(+5V)
9	VCC	PWR	VCC(+5V)
10	VSS VSS	GND	DGND DGND
12	A4/D0	IAVOA	A4/D0
13 14	A5/D1 A6/D2	IA/OA IA/OA	A5/D1 A6/D2
15	A7/D3	IAVOA	A7/D3
16	A8/D4	IAVOA	A8/D4
17	A9/D5 A10/D6	IA/OA IA/OA	A9/D5 A10/D6
19	A11/D7	IA/OA	A11/D7
20 21	A14 NC	OA	A14 NC
22	NC		NC
23 24	PF0/A0 PF1/A1	OA OA	A0 A1
25	PF2/A2	OA	A2
26	PF3/A3	OA OA	A3 A12
27 28	PF4/A12 PF5	J 00	NC
29	PF6	MI	SPXRES NC
30 31	PF7 PB0		NU (Note 5)
32	PB1	1	NU (Note 5)
33 34	PB2 PB3	IA IA	CSRD
35	PB4	ÖÄ	POWER
36 37	PB5 PB6		NU (Note 5) NC
38	PB7	OA	HINT
39 40	A13 NC	OA	A13 NC
41	NC NC		NC NC
42	<u> </u>	OA	WRITE READ
43 44	RD ALE	OA OA	ALE
45	XTLI	IE	XTLI
46 47	XTLO NMI	OE MI	XTLO NU (Note 5)
48	VSS	GND	DGND
49 50	VSS VSS	GND	DGND DGND
51	VSS	GND	DGND
52 53	PC0 PC1	IA/OA IA/OA	HD0 HD1
54	PC2	IA/OA	HD2
55 56	PC3 PC4	IA/OA IA/OA	HD3 HD4
57	PC5	IA/OA	HD5
58	PC6 PC7	IA/OA IA/OA	HD6 HD7
59 60	SYNC	1 1/2/04	NC
61	NC	1	NC NC
62 63	NC PD0	IA.	NC HA0
64	PD1	IA	HA1
65 66	PD2 PD3	IA.	HA2 NC
67	PD4	IA.	HCS
68 69	PD5 PD6	IA IA	HWT
70	PD7	IA	DACK
71 72	PA0 PA1	OA OA	DMAREQ DMAENB
73	PA2	OA	CSINT
74 75	PA3 PA4	IA OA	LINE
	F/14	1 0	I #114F

Table 6. MCU Signals - 80-Pin PQFP

Pin No.	MCU Signal	I/O Type	RC229ATF/2-W Signal	
76	PA5	IA	LCS	
77	PA6	i ia	T/C INT	
78	PA7	Mi	SPINT (Note 6)	
79	A15	OA	A15	
80	NC	i	NC	
Notes: 1. MI = Modern interconnect. 2. NC = No connection; leave pin disconnected (open). 3. NU = Not used; connect as noted. 4. Connect to GND. 5. Connect to +5 VDC through 3.3 KΩ. 6. Connect to +5 VDC through 10 KΩ.				

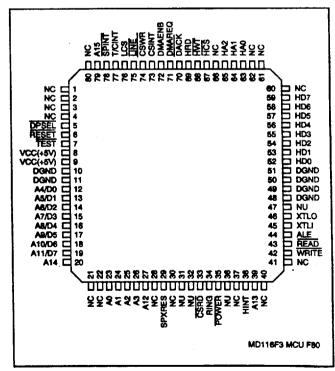


Figure 4. MCU Signals - 80-Pin PQFP

Table 7. MDP Signals - 68-Pin PLCC

Pin No.	Signal Name	124	T DAI MAR ATEM Alamat
		I/O Type	RCV229ATF/2 Signal
1 2	RS2 RS1	IA IA	A2 A1
3 4	RS0 TEST	IA	A0 TEST (Note 3)
5	SLEEP	OA	SLPIN
6 7	RING EYEY	IA OB	RING
l é	EYEX	OB	NC NC
9	EYESYNC RESET	OB Mi	NC SPXRES
11	XTALI	IE	XTALI
12 13	XTALO +5VD	OB PWR	XTALO +5VD
14	GP18	OA	NC
15 16	RLSD XTCLK	OA IA	NC NC
17	DGND	GND	DGND
18 19	TXD TDCLK	IA OA	NC NC
20	TRSTO	MI	TRSTO
21 22	TSTBO TDACO	MI MI	TSTBO TDACO
23	RADCI	Mi	RADCI
24 25	RAGCO MODEO	MI MI	RAGCO MODEO
26	RSTBO	MI	RSTBO
27 28	RRSTO RDCLK	MI OA	EYECLK NC
29 30	RXD TXA2	OA O(DD)	NC TYAO
31	TXA1	O(DD) O(DD)	TXA2 TXA1
32 33	RXA RFILO	I(DA) MI	RXA RFILO
34	AGCIN	MI	AGCIN
35 36	VC NC	OA	VC NC
37	NC		NC
38 39	NC RBDVR	QO	NC CALLID
40	AGND	GND	AGND
41 42	RADVR SLEEPI	OD IA	OH SLPIN
43	RAGCI	Mi	RAGCI
44 45	NC RSTBI	MI	NC RSTBI
46	RRSTI	MI	EYECLK
47 48	RADCO TDACI	MI MI	RADCO TDACI
49 50	TRSTI TSTBI	MI MI	TRSTI TSTBI
51	MODE	MI	MODE
52 53	+5VA SPKR	PWR O(OF)	+5VA SPKR
54	DGND	GND	DGND
55 56	D7 D6	IA/OB IA/OB	D7 D6
57	D5	IA/OR	D5
58 59	D4 D3	IA/OB IA/OB	D4 D3
60	D2	IA/OB	D2
61 62	D1 D0	IA/OB IA/OB	D1 D0
63	ĪRQ	MI	SPINT
64 65	WRITE CS	IA IA	WRITE DPSEL
66	READ	IA	READ
67 68	RS4 RS3	IA IA	A4 A3
Notos			

Notes:

- 1. Mi = Modem Interconnection.
- NC = No connection [may have internal connection; leave pin disconnected (open)].

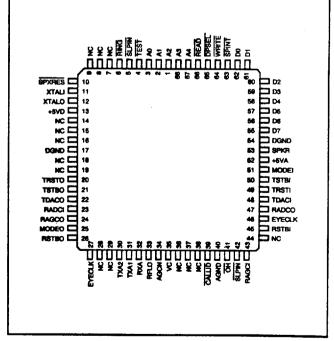


Figure 5. MDP Pin Signals - 68-Pin PLCC

Table 8. MDP Signals - 100-Pin PQFP

Pin No.	Signal Name	I/O Type	RCV229ATF/2 Signal
1 2	NC NC		NC NC
3	NC NC		NC
4	NC		NC
5 6	NC DGND	GND	NC DGND
7	DGND	GND	DGND
8 9	D7 D6	IA/OB IA/OB	D7 D6
10	D5	INOR	D5
11	D4	IA/OB	D4
12 13	D3 D2	IA/OB IA/OB	D3 D2
14	D1	IA/OB	D1
15 16	D0 DGND	IA/OB GND	D0 DGND
17	MODE	MI	MODEI
18	+5VA	PWR	+5VA
19 20	SPKR NC	O(OF)	SPKR NC
21	AGND	GND	AGND
22	TXA2	O(DD)	TXA2 TXA1
23 24	TXA1 NC	O(DD)	NC
25	RXA	I(DA)	RXA
26 27	NC RFILO	MI	NC RFILO
28	AGCIN	MI	AGCIN
29 30	VC AGND	OA GND	VC AGND
31	NC NC	GIVE	NC
32	NC NC		NC NC
33 34	NC NC		NC NC
35	NC		NC NC
36 37	RBDVR AGND	OD GND	CALLID AGND
38	RADVR	OD	OH
39 40	NC NC		NC NC
41	SLEEP	IA.	SLPIN
42	RAGCI	M!	RAGCI AGND
43 44	AGND RSTBI	GND MI	RSTBI
45	RRSTI	MI	EYECLK
46 47	RADCO TDACI	MI MI	RADCO TDACI
48	TRSTI	M	TRSTI
49	TSTBI	MI	TSTBI
50 51	IRQ NC	oc	SPINT NC
52	WRITE	IA.	WRITE
53 54	CS READ	IA IA	DPSEL READ
55	RS4	IA	A4
56 57	RS3 RS2	I IA	A3 A2
58	RS1	I IA	1 A1
59	RS0	IA	AO TEST (Nets 2)
60 61	TEST SLEEP	OA	TEST (Note 3) SLPIN
62	RD	IA	RING
63 64	EYEX	OB OB	NC NC
65	EYESYNC	ОВ	NC .
66 67	DGND NC	GND	DGND NC
68	RESET	MI	SPXRES
69	XTALI	IE OB	XTALI
70 71	XTALO +5VD	OB PWR	XTALO +5VD
72	+5VD	PWR	+5VD

Table 8. MDP Signals - 100-Pin PQFP (Cont'd)

Pin No.	Signal Name	VO Type	RCV229ATF/2 Signal				
73	+5VD	PWR	+5VD				
74 .	GP18	OA	NC				
75	RLSD	OA	NC I				
76	XTCLK	IA I	NC I				
77	DGND	GND	DGND				
78	DGND	GND	DGND				
79	TXD	IA I	NC				
80	DGND	GND	DGND				
81	DGND	GND	DGND				
82	NC		NC				
83	TDCLK	OA	NC				
84	TRSTO	Mi	TRSTO				
85	TSTBO	MI	TSTBO				
86	TDACO	MI	TDACO				
87	RADCI	MI	RADCI				
88	RAGCO	MI GND	RAGCO				
89	DGND	MI	DGND				
90	MODEO		MODEO				
	91 RSTBO MI RSTBO 92 RRSTO MI EYECLK						
92	RDCLK	I OA	NC				
94	RXD	OA	NC NC				
95	NC NC	0^	NC NC				
96	NC NC	1	l NC				
97	DGND	GND	DGND				
98	NC NC	1 3,40	NC				
99	NC NC	1	NC NC				
100	NČ		NC				
Notes:		1	4				
1.	Mi = Modem Inter						
2	NC = No connecti						
	connection; leave						
3.	Connect to +5V th	<u>irough 10K c</u>	hms.				

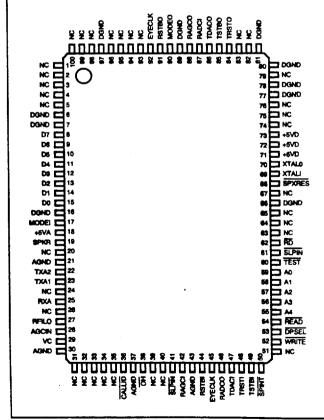


Figure 6. MDP Pin Signais - 100-Pin PQFP

Table 9. MCU Signal Definitions

Label	I/O Type	Signal Name/Description
		OVERHEAD
XTLI, XTLO	IE, OE	MCU Crystal/Clock in and Crystal Out. Connect the MCU XTLI and XTLO pins to an external crystal circuit consisting of a 8.064 MHz crystal and a suitable capacitance network. Alternatively, connect XTLI to a buffered clock and leave XTLO open.
RESET	IC	MCU Reset. The active low RESET input resets the MCU logic and returns the AT command set to the original factory default values and to "stored values" in NVRAM. The RESET input is typically connected to the host bus RESET line through an inverter.
VCC	PWR	+ 5V Digital Supply. Connect VCC to +5V ± 5%.
DGND	GND	Digital Ground. Connect DGND to ground.
		LINE INTERFACE
LINE	OA	Line Relay Driver. The active low LINE output controls a normally closed relay used to disconnect the handset from the line in local voice mode.
POWER	OA	Power Relay Driver. The active low POWER output controls a normally openrelay used to connect power to the handset in local voice mode.
LCS	IA.	Loop Current Sense. LCS is an active high input to the modern that indicates whether the associated handset is off-hook (loop current is flowing) or if the line is incorrectly connected to the handset jack.

PARALLEL HOST INTERFACE (SERIAL INTERFACE SELECTED)

The parallel interface emulates a 16C450 UART interface. The parallel interface is compatible with communications software designed to operate with a 16C450 interface on a PC. Table 15 identifies the parallel interface registers and bits.

Parallel interface operation is equivalent to 16C450 operation with CS0 and CS1 inputs high and DISTR, DOSTR, and ADS inputs low. The corresponding RCV229ATF/2 and 16C450 signals are shown below.

16C450 Signal	RCV229ATF/2 Signal
A0 - A2	HA0 - HA2
D0 - D7	HD0 - HD7
MR	RESET (Active low)
CS2	HCS
DISTR	HWT
DOSTR	HRD
INTRPT	HINT
DDIS	HDIS
OUT1	None (implemented internally)
OUT2	None (implemented internally)

Table 9. MCU Signal Definitions (Cont'd)

Label	I/O Type			Signal N	ame/Desc	eription			
HAO-HA2	IA	Host Bus Address Lines 0-2. During a host read or write operation, HA0-HA2 select an internal MCU 16C450-compatible register. The state of the divisor tatch access bit (DLAB) affects the selection of certain MCU registers. The register addresses are:							
		DLAB	HA2	HA1	HAO	Register			
		0	0	0	0 .	Receiver Buffer Register (Read), Transmitter Holding Register (Write)			
		0	0	0	1	Interrupt Enable Register			
		X	0	1	0	Interrupt Identification Register (Read Only)			
		×	0	1	1	Line Control Register			
		X	1	0	0	Modern Control Register			
		X	1	0	1	Line Status Register (Read Only)			
		X	1	1	0	Modern Status Register (Read Only)			
		X	1	1	1	Scratch Register			
		1	0	0	0	Divisor Latch Register (Least Significant Byte)			
		1	0	0	1	Divisor Latch Register (Most Significant Byte)			
HD0-HD7	IA/OA		ication t	etween t		prised of eight tri-state input/output lines providing bidi d the MCU. Data, control words, and status information			
HCS	IA	Host Bus Chip Select. HCS input low selects the host bus. HCS is usually derived from the host bus address lines in conjunction with the HAEN signal.							
HRD	IA	Host Bus Read. HRD is an active low, read control input. When HCS is low, HRD low allows the hos to read status information or data from a selected MCU register.							
HWT	IA	Host Bus Write. HWT is an active low, write control input. When HCS is low, HWT low allows the host to write data or control words into a selected MCU register.							
HINT	OA	transmitter holdin	g registe	er empty,	or modem	when the receiver error flag, received data available, status interrupt has an active high condition. HINT is ce or master reset operation.			
DACK	IA	DMA Acknowled issued by the DM			w DACK in	put is used to acknowledge receipt of the DMA reques			
CSINT	OA	Audio C/S Regis that the host bus				ne active high CSINT is asserted by the MCU to indicat Register (ASR).			
		EXERNAL BUS	INTERF	ACE					
						e signals implement a parallel microprocessor interface, and the Audio C/S Registers.			
A0-A3, A12-A15	OA	Address Lines ()-3 and 1	1 2-15. A 0	-A3 and A	12-A15 are the external bus dedicated address lines.			
A4/D0-A11/D7	IA/OA	Address Line 4/ tiplexed address			ress Line	11/Data Line 7. A4/D0-A11/D7 are the external bus m			
ALE	OA	Address Latch Enable. A negative transition on ALE output latches the address on the multiplexed address/data bus.							
READ	OA				nables dat	a to be transferred from the selected device onto the ex			
	OA	Read Enable. READ output low enables data to be transferred from the selected device onto the external bus A4/D0-A11/D7 lines. Write Enable. WRITE output low enables data to be transferred from the external bus A4/D0-A11/D7							

Data/Fax/Voice Modem

Table 9. MCU Signal Definitions (Cont'd)

an 8-bit DMA write latch), two D-type filp-flops (DMA request FF and T/C FF) and supporting gates. The DMA read latch is used to transfer playback data from the host bus to the modern all bus and the DMA write latch is used to transfer playback data from the host bus from the modern all bus. The DMA request FF controls the DMA request to the host bus and the T/C FF gene interrupt request to the MCU when the terminal count of the DMA transfer is complete. DMAENB OA DMA Énable. The active high DMAENB output is used to enable the DMA request flip-flop in DMA Control Logic. When enabled, this flip-flop asserts the FF DRQ output to the host bus the MCU DMAREO is asserted.! DMAREQ OA DMA Request. The active high DMAREQ output is used to request a DMA transfer from the 17/CINT IA Terminal Count interrupt Request. The active high T/CINT signal is asserted by the T/C flip the DMA Control Logic to indicate that the DMA transfer terminal count has been reached. ES3 OA DMA Latch Select. This active output is asserted when an MCU selects the DMA latches. AUDIO CONTROL AND STATUS REGISTERS INTERFACE The user-supplied Audio Control and Status Registers consist of two 8-bit registers, address logic, and supporting AND gates. These registers are located at address 0x534h on the host 1 Audio Control Register (ACR) is written by the host to enable record, playback, speaker, and functions, select 11.025 kHz or 7.2 k Hz sampling rate, and four levels of speaker volume. The Status Register (ASR) is written by the modern to report DTMF enable/disable, busy/fide, sar overrun, and terminal count conditions. CSRD IA Audio Control Register Read. The CSRD is active low when the host bus writes the Audio Register. CSWR IA Audio Control Register Write. The CSWR is active low when the host bus writes the Audio Register. SLEEP CONTROL INTERFACE RING IA BING input high removes the modern from the sleep mode. RING is typically connected wate when ringing is present. MDP INTERCONNECT DPSEL OA MDP Power-On Reset. Connec	Label	I/O Type	Signal Name/Description
an 8-bit DMA write latch), two D-type flip-Rops (DMA request FF and T/C FF) and supporting gates. The DMA read latch is used to transfer playback data from the host bus to the modern all bus and the DMA write latch is used to transfer playback data from the host bus from the modern all bus. The DMA request FF controls the DMA request to the host bus and the T/C FF gene interrupt request to the MCU when the terminal count of the DMA transfer is complete. DMAENB OA DMA Enable. The active high DMAENB output is used to enable the DMA request flip-flop in DMA Control Logic. When enabled, this flip-flop asserts the FF DRQ output to the host bus the MCU DMAREQ is asserted.! DMAREQ OA DMA Request. The active high DMAREQ output is used to request a DMA transfer from the 17/CINT IA Terminal Count Interrupt Request. The active high T/CINT signal is asserted by the T/C flip the DMA Control Logic to indicate that the DMA transfer terminal count has been reached. ES3 OA DMA Latch Select. This active output is asserted when an MCU selects the DMA latches. AUDIO CONTROL AND STATUS REGISTERS INTERFACE The user-supplied Audio Control and Status Registers consist of two 8-bit registers, address logic, and supporting AND gates. These registers are located at address 0x534h on the host I Audio Control Register (ACR) is written by the host to enable record, playback, speaker, and functions, select 11.025 kHz or 7.2 k Hz sampling rate, and four levels of speaker volume. The Status Register (ASR) is written by the modem to report DTMF enable/disable, busy/fide, sar overrun, and terminal count conditions. CSRD IA Audio Control Register Read. The CSRD is active low when the host bus writes the Audio Register. SUEEP CONTROL INTERFACE RING IA Audio Control Ringster Write. The CSWR is active low when the host bus writes the Audio Register. SLEEP CONTROL INTERFACE MDP INTERCONNECT MDP INTERCONNECT MDP INTERCONNECT MDP INTERCONNECT MDP Power-On Reset. Connect the MCU SPINT input to the MDP SPRES (RESET) outp			DMA CONTROL LOGIC INTERFACE
DMA Control Logic. When enabled, this flip-flop asserts the FF DRQ output to the host bus in the MCU DMAREQ is asserted. DMAREQ OA DMA Request. The active high DMAREQ output is used to request a DMA transfer from the intervent of the DMA Control Logic to indicate that the DMA transfer terminal count has been reached. ES3 OA DMA Latch Select. This active output is asserted when an MCU selects the DMA latches. AUDIO CONTROL AND STATUS REGISTERS INTERFACE The user-supplied Audio Control and Status Registers consist of two 8-bit registers, address logic, and supporting AND gates. These registers are located at address 0x534h on the host to Audio Control Register (ACR) is written by the host to enable record, playback, speaker, and functions, select 11.025 kHz or 7.2 k Hz sampling rate, and four levels of speaker volume. The Status Register (ASR) is written by the modern to report DTMF enable/disable, busy/fdle, san overrun, and terminal count conditions. CSRD IA Audio Status Register Read. The CSRD is active low when the host bus writes the Audio Segister. CSWR IA Audio Control Register Write. The CSWR is active low when the host bus writes the Audio Segister. CSWR IA Audio Register Select. This active low output is asserted when an MCU selects the Audio Selects the Select. RING IA Ring, RING input high removes the modern from the sleep mode. RING is typically connected vate when ringing is present. MDP INTERCONNECT DPSEL OA MDP Select. This active low output is asserted when the MCU selects the MDP. MDP Select. This active low output is asserted when the MCU selects the MDP. MDP INTERCONNECT MDP Select. This active low output is to the MDP SPINT output and to VC through 10K ohms. SPXRES			The user-supplied DMA Control Logic consists of two 8-bit data latches (an 8-bit DMA read latch and an 8-bit DMA write latch), two D-type flip-flops (DMA request FF and T/C FF) and supporting and gates. The DMA read latch is used to transfer playback data from the host bus to the modern external bus and the DMA write latch is used to transfer record data to the host bus from the modern external bus. The DMA request FF controls the DMA request to the host bus and the T/C FF generates an interrupt request to the MCU when the terminal count of the DMA transfer is complete.
T/CINT IA Terminal Count Interrupt Request. The active high T/CINT signal is asserted by the T/C flip the DMA Control Logic to indicate that the DMA transfer terminal count has been reached. ES3 OA DMA Latch Select. This active output is asserted when an MCU selects the DMA latches. AUDIO CONTROL AND STATUS REGISTERS INTERFACE The user-supplied Audio Control and Status Registers consist of two 8-bit registers, address logic, and supporting AND gates. These registers are located at address 0x534h on the host It Audio Control Register (ACR) is written by the host to enable record, playback, speaker, and functions, select 11.025 kHz or 7.2 k Hz sampling rate, and four levels of speaker volume. The Status Register (ASR) is written by the modern to report DTMF enable/disable, busy/idle, sar overrun, and terminal count conditions. CSRD IA Audio Status Register Read. The CSRD is active low when the host bus reads the Audio S Register. CSWR IA Audio Control Register Write. The CSWR is active low when the host bus writes the Audio Register. ES2 OA Audio Register Select. This active low output is asserted when an MCU selects the Audio (isters.) SLEEP CONTROL INTERFACE RING IA Ring, RING input high removes the modern from the sleep mode. RING is typically connected vate when ringing is present. MDP INTERCONNECT DPSEL OA MDP Select. This active low output is asserted when the MCU selects the MDP. SPINT IA MDP Interrupt Request. Connect the MCU SPINT input to the MDP SPINT output and to VC through 10K ohms. SPXRES IA MDP Power-On Reset. Connect the MCU SPXRES input to the MDP SPRES (RESET) outp	DMAENB	OA	DMA Enable. The active high DMAENB output is used to enable the DMA request flip-flop in the DMA Control Logic. When enabled, this flip-flop asserts the FF DRQ output to the host bus when the MCU DMAREQ is asserted.
ES3 OA DMA Latch Select. This active output is asserted when an MCU selects the DMA latches. AUDIO CONTROL AND STATUS REGISTERS INTERFACE The user-supplied Audio Control and Status Registers consist of two 8-bit registers, address logic, and supporting AND gates. These registers are located at address 0x534h on the host It Audio Control Register (ACR) is written by the host to enable record, playback, speaker, and functions, select 11.025 kHz or 7.2 k Hz sampling rate, and four levels of speaker volume. The Status Register (ASR) is written by the modern to report DTMF enable/disable, busy/idle, sar overrun, and terminal count conditions. CSRD IA Audio Status Register Read. The CSRD is active low when the host bus reads the Audio Segister. CSWR IA Audio Control Register Write. The CSWR is active low when the host bus writes the Audio Register. ES2 OA Audio Register Select. This active low output is asserted when an MCU selects the Audio (isters.) SLEEP CONTROL INTERFACE RING IA Ring. RING input high removes the modern from the sleep mode. RING is typically connected vate when ringing is present. MDP INTERCONNECT DPSEL OA MDP Select. This active low output is asserted when the MCU selects the MDP. SPINT IA MDP Interrupt Request. Connect the MCU SPINT input to the MDP SPINT output and to VC through 10K ohms. SPXRES IA MDP Power-On Reset. Connect the MCU SPXRES input to the MDP SPRES (RESET) outp	DMAREQ	OA	DMA Request. The active high DMAREQ output is used to request a DMA transfer from the host but
AUDIO CONTROL AND STATUS REGISTERS INTERFACE The user-supplied Audio Control and Status Registers consist of two 8-bit registers, address logic, and supporting AND gates. These registers are located at address 0x34h on the host in Audio Control Register (ACR) is written by the host to enable record, playback, speaker, and functions, select 11.025 kHz or 7.2 k Hz sampling rate, and four levels of speaker volume. The Status Register (ASR) is written by the modem to report DTMF enable/disable, busy/idle, san overrun, and terminal count conditions. CSRD IA Audio Status Register Read. The CSRD is active low when the host bus reads the Audio Sequence. Register. IA Audio Control Register Write. The CSWR is active low when the host bus writes the Audio Register. ES2 OA Audio Register Select. This active low output is asserted when an MCU selects the Audio Seters. SLEEP CONTROL INTERFACE Ring. RING input high removes the modem from the sleep mode. RING is typically connected vate when ringing is present. MDP INTERCONNECT DPSEL OA MDP Select. This active low output is asserted when the MCU selects the MDP. MDP Interrupt Request. Connect the MCU SPINT input to the MDP SPINT output and to VC through 10K ohms. SPXRES IA MDP Power-On Reset. Connect the MCU SPXRES input to the MDP SPRES (RESET) outp	r/cint	IA	Terminal Count Interrupt Request. The active high T/CINT signal is asserted by the T/C flip-flop in the DMA Control Logic to indicate that the DMA transfer terminal count has been reached.
The user-supplied Audio Control and Status Registers consist of two 8-bit registers, address logic, and supporting AND gates. These registers are located at address 0x534h on the host is Audio Control Register (ACR) is written by the host to enable record, playback, speaker, and functions, select 11.025 kHz or 7.2 k Hz sampling rate, and four levels of speaker volume. The Status Register (ASR) is written by the modern to report DTMF enable/disable, busy/idle, san overrun, and terminal count conditions. CSRD IA Audio Status Register Read. The CSRD is active low when the host bus reads the Audio Stegister. CSWR IA Audio Control Register Write. The CSWR is active low when the host bus writes the Audio Register. ES2 OA Audio Register Select. This active low output is asserted when an MCU selects the Audio Sters. SLEEP CONTROL INTERFACE RING IA Ring. RING input high removes the modern from the sleep mode. RING is typically connected vate when ringing is present. MDP INTERCONNECT DPSEL OA MDP Select. This active low output is asserted when the MCU selects the MDP. SPINT IA MDP Interrupt Request. Connect the MCU SPINT input to the MDP SPIRT output and to VC through 10K ohms. SPXRES IA MDP Power-On Reset. Connect the MCU SPXRES input to the MDP SPRES (RESET) output and the MDP space of the MDP space of the MDP space output to the MDP SPRES (RESET) output and the MDP space of the MDP space output to the MDP space output and to VC through 10K ohms.	ES3	OA	DMA Latch Select. This active output is asserted when an MCU selects the DMA latches.
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SPINT IA MDP Interrupt Request. Connect the MCU SPINT input to the MDP SPINT output and to VC through 10K ohms. SPXRES IA MDP Power-On Reset. Connect the MCU SPXRES input to the MDP SPRES (RESET) outp			MDP INTERCONNECT
through 10K ohms. SPXRES IA MDP Power-On Reset. Connect the MCU SPXRES input to the MDP SPRES (RESET) outp	DPSEL	OA	MDP Select. This active low output is asserted when the MCU selects the MDP.
	SPINT	IA	MDP Interrupt Request. Connect the MCU SPINT input to the MDP SPINT output and to VCC through 10K ohms.
	SPXRES	IA	MDP Power-On Reset. Connect the MCU SPXRES input to the MDP SPRES (RESET) output.
MRXD IA MDP Receive Data. Connect the MCU MRES input to the MDP RXD (RXD) output.	MRXD	i A	MDP Receive Data. Connect the MCU MRES input to the MDP RXD (RXD) output.

Table 10. MDP Signal Definitions

Label	I/O Type	Signal Name/Description
		OVERHEAD
XTALI, XTALO	IE, OE	MDP Crystal/Clock in and Crystal Out. Connect the MDP XTALI and XTALO pins to a external crystal circuit consisting of a 24.00014 MHz crystal and two capacitors. Alternatively, connect XTALI to a buffered clock or a sine wave oscillator and leave XTALO open.
RESET	IC	Reset Controller. The active low RESET input resets the MCU logic and returns the AT command set to the original factory default values and to "stored values" in NVRAM. The RESET input is typically connected to the host bus RESET line through an inverter.
+5VD (P5VD)	PW R	+ 5V Digital Supply. Connect +5VD to +5V ± 5%.
+5VA (P5VA)	PW R	+ 5V Analog Supply. Connect +5VA to +5V ± 5% is required by the data pump analog circuits.
DGND	GND	Digital Ground. Connect to ground.
AGND	GND	Analog Ground. Connect to ground.
		LINE INTERFACE (DAA)
RINGD	IA	Ring Frequency Detected. A falling edge on the RINGD input initiates an internal ring frequency measurement. The RINGD input is typically connected to the output of a 4N35 optoisolator or equivalent. The optoisolator output should not respond to a voltage less than 40 VRMS appearing across TIP and RING with respect to ground.
CALLID	OD	Caller ID Relay Control (MDP OHRC). Typically, the MDP CALLID output is connected to the normally closed Caller ID relay (DPDT). When Caller ID is enabled, the modern will assert this output to open the Caller ID relay and close the Off-hook relay in order to detect Caller ID information between the first and second rings.
VOICE	OD	Voice Relay Control (MDP TALK). Typically, the MDP VOICE output is connected to the normally open Voice relay (DPDT). In voice mode, VOICE active closes the relay to switch the handset from the telephone line to a current source to power the handset so it can be used as a microphone and speaker interface to the modern.
		The MDP CALLID and VOICE outputs can each directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor, such as an MPSA20, can be used to drive heavier loads (e.g., ejectro-mechanical relays).
• .		EXTERNAL FILTER COMPONENTS
TXA1, TXA2	I(DB)	Transmit Analog Output. The TXA1 and TXA2 outputs are differential outputs to the line interface of to an optional external hybrid circuit.
RXA	I(DA)	Receive Analog Input. RXA is a single-ended receive data input from the telephone line interface o an optional external hybrid circuit.
VC	OA	Centerpoint Voltage. Connect VC to ground through 0.1 μF.
		SPEAKER INTERFACE
SPKR	O(DF)	Speaker Analog Output. The SPKR output reflects the receive input signal. The SPKR on/off and three levels of attenuation are controlled by interface memory bits. When the speaker is turned off, the SPKR output is clamped to the voltage at the VC pin. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external LM386 audit power amplifier.
	<u> </u>	MCU INTERCONNECT
SPINT	OA	MDP Interrupt Request. Connect the MDP SPINT output to the MCU SPINT input and to VCC through 10K-ohms.
SPXRES	OA	MDP Power-On Reset. Connect the MDP SPXRES output to the MCU SPXRES input.
OI AITES		•

Data/Fax/Voice Modem

Table 11. Digital interface Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Units	Test Conditions ¹
Input High Voltage	ViH				Vdc	
Type IA		2.0	_	Voc		
Type IB		2.4	- :	Vcc	1	
Type IC	ļ	3.5	-	Vcc		1
Type ID		0.8 (Vcc)	-	Vcc		1
Type IE			4.0	•		Note 2.
Input Low Voltage	VıL				Vdc	
Type IA, IB, & ID		-0.3		0.8	1	
Type IE		-	1.0	· .		Note 2.
Input Leakage Current	IN				μAdc	
Type IA (Non-multiplexed)		<u> </u>	•	±10		V _{IN} = 0 to V _{CC}
Output High Voltage	Vон				Vdc	
Type OA		2.4	•	•		LOAD = -100 μA
Type OB & OC		3.5	-	-		ILOAD = -100 μA
Type OD			-	Vcc		ILOAD = 0 mA
Type OE						Note 3.
Output Low Voltage	Vol				Vdc	
Type OA		- 1	-	0.4		ILOAD = 1.6 mA
Type OB & OC	İ	-	•	0.4		ILOAD = 0.8 mA
Type OD		-	0.75			ILOAD = 15 mA
Three-State (Off) Current	Its				μAdc	
Type OA		-	-	±10		V _{IN} = 0.8 V to 4.5 V @ 500 kHz
Type OB & OC		- 1	-	±10		V _{IN} = 0.8 V to V _{CC} - 1 V

Notes:

- 1. Test Conditions: $V_{CC} = 5V \pm 5\%$, $T_A = 0\Delta C$ to $70\Delta C$, (unless otherwise stated).
- 2. Type IE inputs are centered approximately 2.5 V and swing 1.5 VPEAK in each direction.
- 3. Type OE outputs provide oscillator feedback when operating with an external crystal.

Table 12. Analog Interface Characteristics

Name	Туре	Characteristic
RXA	I(DA)	1458 type op amp output
TXA1, TXA2	O(DD)	1458 type op amp input
SPKR	O(OF)	LM386 type audio amp input

Table 13. Current and Power Requirements

	Curre	Current (ID)		r (Po)		
Mode	Typical Current @ 25°C	Maximum Current @ 0°C	Typical Power @ 25°C	Maximum Power @ 0°C	Notes	
MCU						
Normal mode .	11 mA	13.3 mA	55 mW	70 mW	finmou) = 7.3728 MHz @ XTLI	
Sleep mode	3 mA	3.8 mA	15 mW	20 mW	,	
MDP	ŀ	1				
Normal mode	38 mA	45.7 mA	190 mW	240 mW	fin(MDP) = 24.00014 MHz @ XTALI	
Sleep mode	2 mA	2.5 mA	10 mW	13 mW		
RCV229ATF/2-BA						
Normal mode	49 mA	59.0 mA	245 mW	310 mW		
Sleep mode	5 mA	6.3 mA	25 mW	33 mW		

1.Test conditions: VDD = 5.0 VDC for typical values; VDD = 5.25 VDC for maximum values.

Table 14. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	Voo	-0.5 to +7.0	V
Input Voltage	VIN	-0.5 to +5VD +0.5	V
Analog Inputs	VIN	-0.3 to +5VA + 0.3	V
Voltage Applied to Outputs in High Z State	VHZ	-0.5 to +5VD + 0.5	V
DC Input Clamp Current	lax l	±20	mA
DC Output Clamp Current	lox	±2 0	mA.
Static Discharge Voltage (@ 25°C)	VESD	±3000	V
Latch-Up Current (@ 25°C)	PTRIG	±200	mA
Operating Temperature Range	TA	0 to +70	•c
Storage Temperature Range	Tate	-55 to +125	*C

Table 15. Parallel Interface Registers

Register	Register				Bit	No.				
No.	Name	7	6	5	4	3	2	1	0	
7	Scratch Register (SCR)	Scratch Register								
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Carrier Indicator Set to Data Edge of Data Clearier (RI) Ready Send Carrier Ring Set t							
5	Line Status Register (LSR)	0	Transmitter Empty (TEMT)	Transmitter Holding Register (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)	
4	Modem Control Register (MCR)	0	0	0	Local Loopback	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)	
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)	
2	interrupt Identify Register (IIR) (Read Only)	0	0 0 0 0 Pending Pending Interrupt ID ID Bit 1 Bit 0							
1 DLAB = 0	Interrupt Enable Register (IER)	0	0	0	0	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)	
0 DLAB = 0	Transmitter Holding Register (THR)	Transmitter Holding Register (Write Only)								
0 DLAB = 0	Receiver Buffer Register (RBR)	Receiver Buffer Register (Read Only)								
1 DLAB = 1	Divisor Latch (MSB) Register (DLM)				Divisor L	atch (MS)				
0 DLAB = 1	Divisor Latch (LSB) Register (DLL)				Divisor	Latch (LS)				

Table 16. Audio Control and Status Registers

Register Name	Bit No.									
	7	6	5	4	3	2	1	0		
Audio Status Register (ASR)	Not Used	Not Used	Not Used	Not Used	DTMF Enable (DE)	Busy/Idle (B/I)	Sample Overrun (SOR)	Terminal Count (TC)		
Audio Control Register (ACR)	Record Enable (RE)	Playback Enable (PE)	Sampling Rate (SR)	Speaker Enable (SE)	Handset Enable (HE)	Not Used	Volume Level 2 (VL2)	Volume Level 1 (VL1)		

Audio Status Register (ASR) Bit Definitions

Bit	Description				
7-4	Not used.				
3	DTMF Enable (DE)				
	1 DTMF detection is enabled.				
	0 DTMF detection is not enabled.				
2	Busy/Idle (B/I)				
	1 The modern is busy with a fax or data task.				
	0 The modern is idle.				
1	Sample Overrun (SOR)				
	Sample overrun occurred. A DMA request was not serviced in time to serve the next sample. This bit indicates an overrun for record, or an underrun for playback.				
	0 Sample overrun did not occur.				
0	Terminal Count (TC)				
	1 The terminal count has been reached for the DMA transfer.				
	0 The terminal count has not been reached for the DMA transfer.				

Audio Control Register (ACR) Bit Definitions

Bit			Description					
7	Record Enable (RE)							
	1	Record is enabled. The MCU will request DMA cycles to transfer voice data from the MDP						
		to host men						
	0	Record is disabled						
6	Playback Enable (PE)							
	1	Playback is enabled. The MCU will request DMA cycles to transfer voice data from host memory to the MDP.						
	0 Playback is disabled.							
5	Sampling Rate (SR)							
	1	1 The sampling rate is 11.025 kHz.						
	0	0 The sampling rate is 7.2 kHz.						
4	Speaker Enable (SE)							
	1	The speaker is enabled (on).						
	0	The speaker is disabled (off).						
3	Handset Enable (HE)							
	1	1 The handset is enabled.						
	0 The handset is disabled.							
2	Not used	i						
1-0	Volume Level (VL)							
	VL2	VL1	Level					
	0	0	Low					
	0	1	Moderate					
	1	0	Moderate					
	1	1	High					

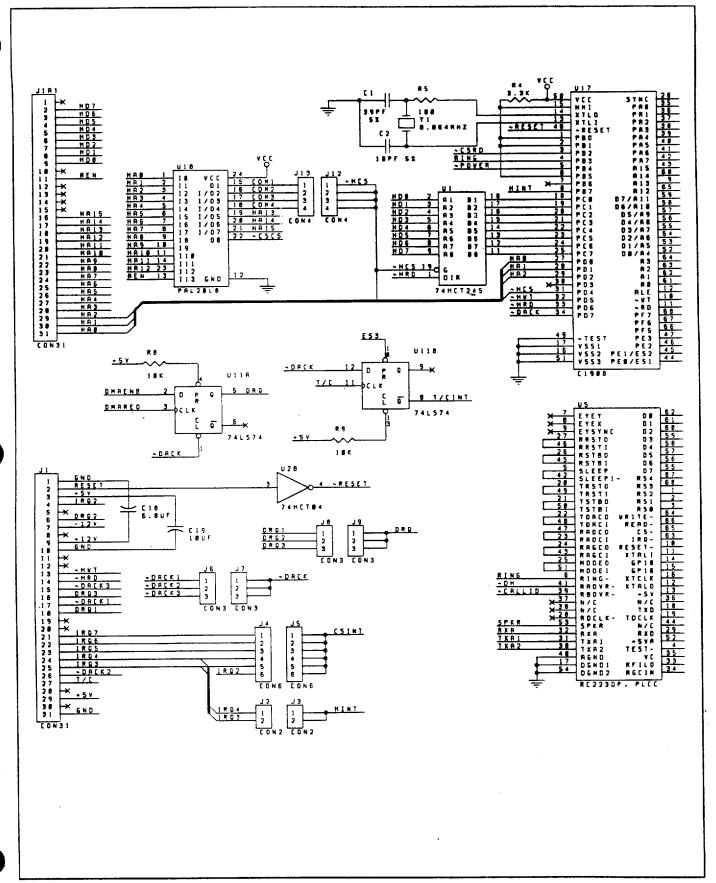


Figure 7. Typical Application Schematic

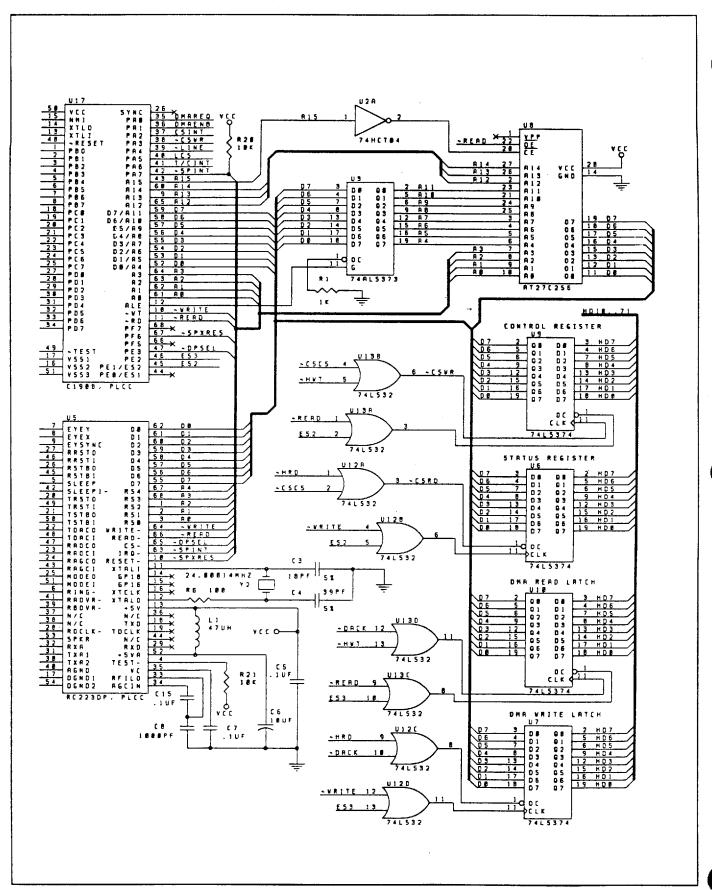


Figure 7. Typical Application Schematic (Cont'd)

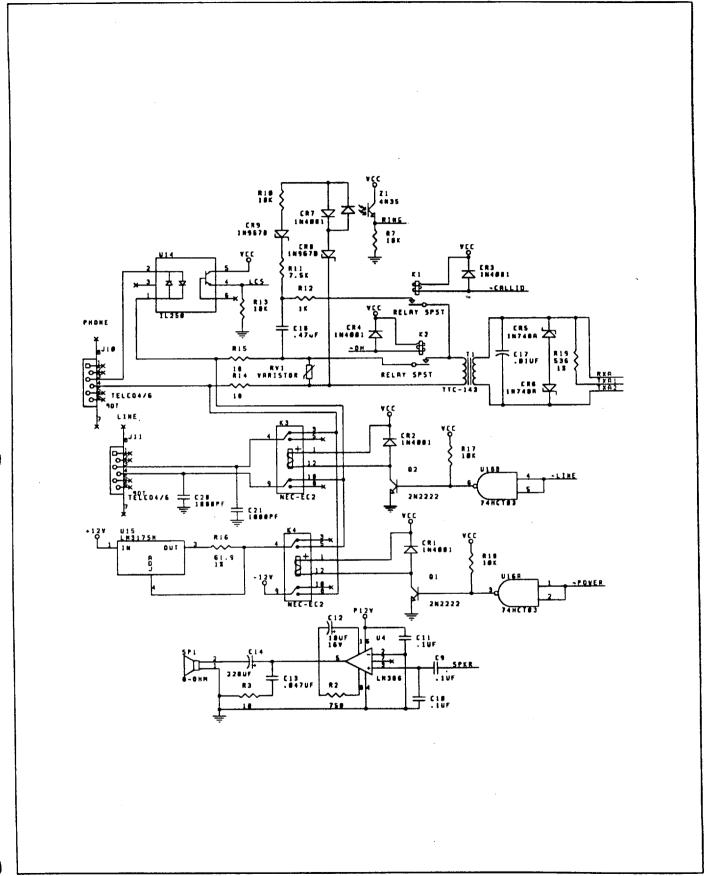


Figure 7. Typical Application Schematic (Cont'd)