

S6B0755

128 SEG / 65 COM DRIVER & CONTROLLER FOR STN LCD

JUNE. 2000.

Ver. 1.0

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| S6B0755 Specification Revision History | | |
|---|--|-------------|
| Version | Content | Date |
| 0.0 | Original | Dec.1999 |
| 0.1 | Append PAD configuration Append COG/ILB align key coordinates and TOM coordinate Append PAD center coordinates to table 1, 2 | Jan.2000 |
| 0.2 | Added 6800-mode interface description for data latch with (page 12) C2 CAP value : 0.1 to 0.47uF → 0.47 to 2.0uF (page 30) Added description of the column address operation. (page 35) Added that Display On/Off command has priority over Entire Display On/Off and Reverse Display On/Off. (page 39) Added N-line inversion command description (page 43) | Jan.2000 |
| 0.3 | Modify 6800 parallel interface timing | Feb.2000 |
| 1.0 | Fix the TBD Value of DC Characteristics. Modify dynamic current consumption value(Idd2.Idds1) | Jun.2000 |

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INTRODUCTION

The S6B0755 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 65 common and 128 segment driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip display data RAM of 65 x 128 bits. It provides a highly flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no externally operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

Driver Output Circuits

- 65 common outputs / 128 segment outputs

Applicable Duty Ratios

| Programmable duty ratio | Applicable LCD bias | Maximum display area |
|-------------------------|---------------------|----------------------|
| 1/17 to 1/65 | 1/4 to 1/9 | 65 × 128 |

- Various partial display
- Partial window moving & data scrolling

On-chip Display Data RAM

- Capacity: 65 x 128 = 8,320 bits
- Bit data "1": a dot of display is illuminated.
- Bit data "0": a dot of display is not illuminated.

Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series.
- SPI (Serial Peripheral Interface) available. (only write operation)

On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage converter (x3, x4 or x5)
- Voltage regulator (temperature coefficient: -0.05%/°C or external input)
- On-chip electronic contrast control function (64 steps)
- Voltage follower (LCD bias: 1/4 to 1/9)

Operating Voltage Range

- Supply voltage (V_{DD}): 1.8 to 3.3 V
- LCD driving voltage (V_{LCD} = V_O - V_{SS}): 4.0 to 15.0 V

Low power Consumption

- 120 μA Typ. (Internal power supply on and display OFF)

Package Type

- Gold bumped chip or TCP

BLOCK DIAGRAM

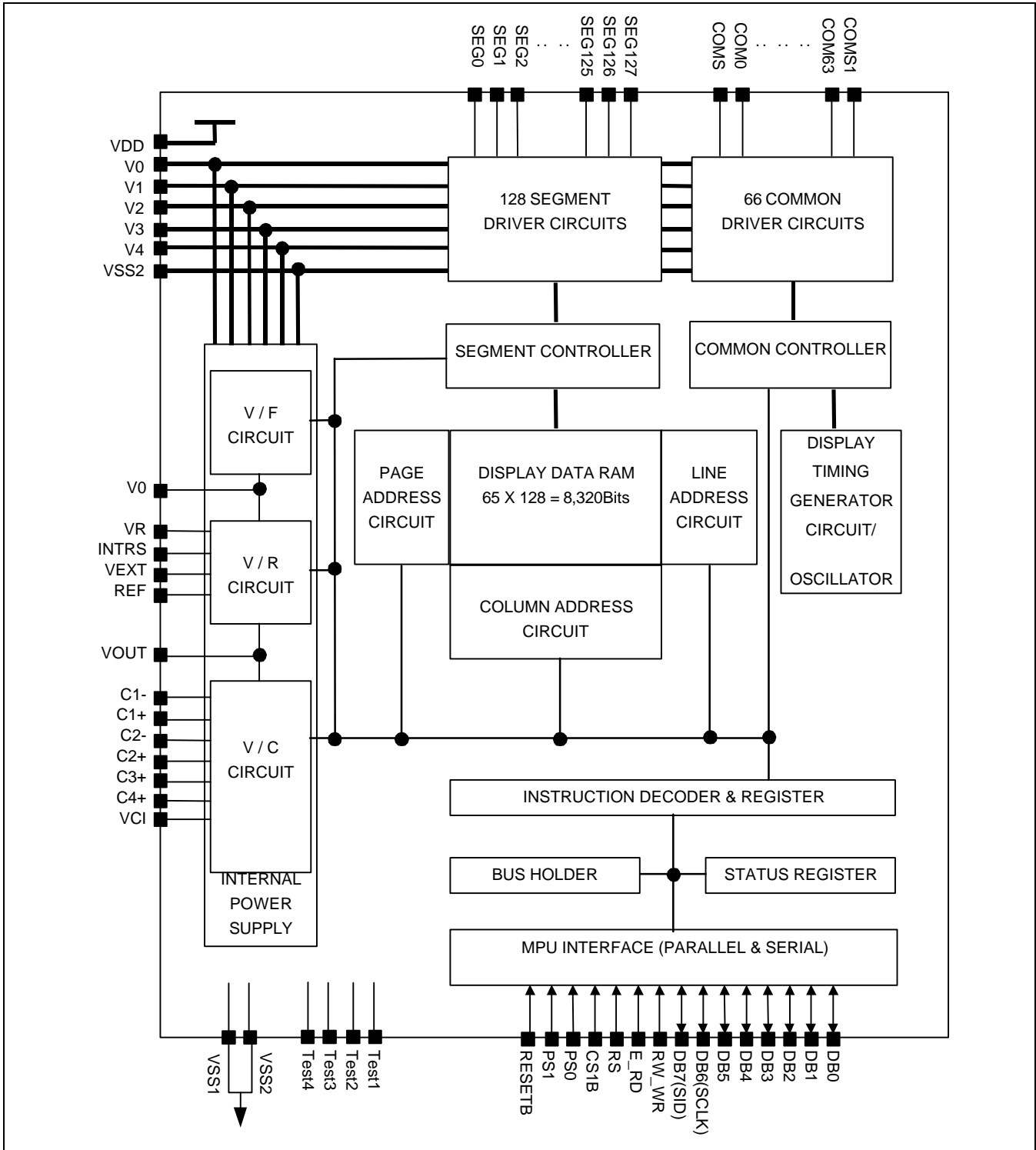


Figure 1. Block Diagram

PAD CONFIGURATION

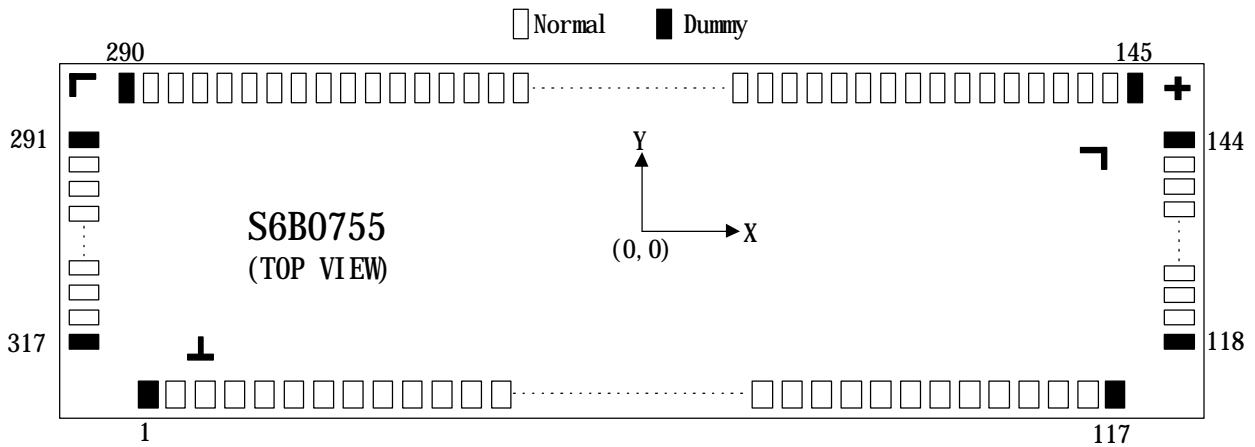


Figure 2. S6B0755 Chip Configuration

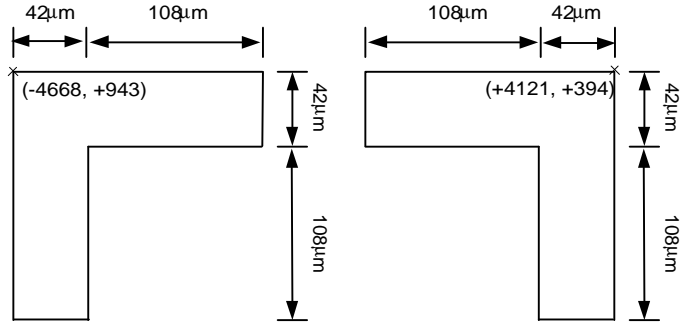
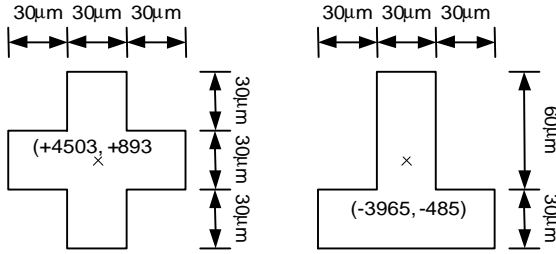
Table 1. S6B0755 Pad Dimension

| Item | Pad No. | | Size | | Unit |
|------------------------|-------------------------------|------------|-----------|------|------|
| | | | X | Y | |
| Chip size | - | | 9530 | 2080 | um |
| Pad pitch | Input | 1 to 117 | 70 | | |
| | Output | 119 to 143 | 60 | | |
| | | 146 to 289 | | | |
| | | 292 to 316 | | | |
| NC* | 1,117,118,144,145,290,291,317 | 80 | | | |
| Bumped pad size (Max.) | 1 | | 60 | 110 | |
| | 2 to 116 | | 50 | 100 | |
| | 117 | | 60 | 110 | |
| | 118 | | 110 | 60 | |
| | 119 to 143 | | 110 | 40 | |
| | 144 | | 110 | 60 | |
| | 145 | | 60 | 110 | |
| | 146 to 289 | | 40 | 110 | |
| | 290 | | 60 | 110 | |
| | 291 | | 110 | 60 | |
| | 292 to 316 | | 110 | 40 | |
| 317 | | 110 | 60 | | |
| Bumped pad height | All pad | | 14 (Typ.) | | |

* Dummy to Dummy pad pitch is 80 um . Dummy to normal pad pitch is 80 um.

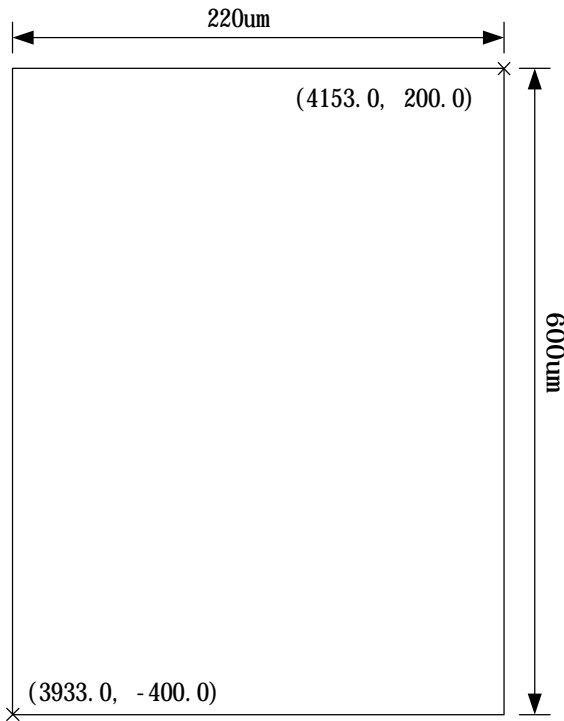
COG Align Key Coordinate

ILB Align Key Coordinate



TOM(TEG On Main chip) Coordinate

The TOM has test items for process evaluation. There are many bumped PADs in this area as like main chip. So when designing COG pattern, ITO pattern must be prohibited on this area (TOM). If ITO pattern is used for routing over this area, it can be happened pattern-short through bumped PAD on TOM.



PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

| NO. | Name | X | Y | NO. | Name | X | Y | NO. | Name | X | Y | NO. | Name | X | Y |
|-----|--------|-------|------|-----|-------|------|------|-----|-------|------|------|-----|-------|------|-----|
| 1 | DUMMY | -4070 | -925 | 51 | VSS2 | -560 | -925 | 101 | V2 | 2940 | -925 | 151 | COM1 | 3990 | 893 |
| 2 | TEST1 | -3990 | -925 | 52 | VSS2 | -490 | -925 | 102 | V2 | 3010 | -925 | 152 | COM0 | 3930 | 893 |
| 3 | TEST2 | -3920 | -925 | 53 | VSS2 | -420 | -925 | 103 | V2 | 3080 | -925 | 153 | COM5 | 3870 | 893 |
| 4 | TEST3 | -3850 | -925 | 54 | VSS2 | -350 | -925 | 104 | V2 | 3150 | -925 | 154 | SEG0 | 3810 | 893 |
| 5 | TEST4 | -3780 | -925 | 55 | VOUT | -280 | -925 | 105 | V1 | 3220 | -925 | 155 | SEG1 | 3750 | 893 |
| 6 | VSS | -3710 | -925 | 56 | VOUT | -210 | -925 | 106 | V1 | 3290 | -925 | 156 | SEG2 | 3690 | 893 |
| 7 | VDD | -3640 | -925 | 57 | VOUT | -140 | -925 | 107 | V1 | 3360 | -925 | 157 | SEG3 | 3630 | 893 |
| 8 | VDD | -3570 | -925 | 58 | VOUT | -70 | -925 | 108 | V1 | 3430 | -925 | 158 | SEG4 | 3570 | 893 |
| 9 | PS0 | -3500 | -925 | 59 | VOUT | 0 | -925 | 109 | V0 | 3500 | -925 | 159 | SEG5 | 3510 | 893 |
| 10 | VSS | -3430 | -925 | 60 | VOUT | 70 | -925 | 110 | V0 | 3570 | -925 | 160 | SEG6 | 3450 | 893 |
| 11 | VDD | -3360 | -925 | 61 | VOUT | 140 | -925 | 111 | V0 | 3640 | -925 | 161 | SEG7 | 3390 | 893 |
| 12 | PS1 | -3290 | -925 | 62 | VOUT | 210 | -925 | 112 | V0 | 3710 | -925 | 162 | SEG8 | 3330 | 893 |
| 13 | VSS | -3220 | -925 | 63 | C3+ | 280 | -925 | 113 | VR | 3780 | -925 | 163 | SEG9 | 3270 | 893 |
| 14 | CS1B | -3150 | -925 | 64 | C3+ | 350 | -925 | 114 | VR | 3850 | -925 | 164 | SEG10 | 3210 | 893 |
| 15 | VDD | -3080 | -925 | 65 | C3+ | 420 | -925 | 115 | VSS | 3920 | -925 | 165 | SEG11 | 3150 | 893 |
| 16 | VDD | -3010 | -925 | 66 | C3+ | 490 | -925 | 116 | VSS | 3990 | -925 | 166 | SEG12 | 3090 | 893 |
| 17 | RESETB | -2940 | -925 | 67 | C1- | 560 | -925 | 117 | DUMMY | 4070 | -925 | 167 | SEG13 | 3030 | 893 |
| 18 | RS | -2870 | -925 | 68 | C1- | 630 | -925 | 118 | DUMMY | 4618 | -881 | 168 | SEG14 | 2970 | 893 |
| 19 | VSS | -2800 | -925 | 69 | C1- | 700 | -925 | 119 | COM31 | 4618 | -801 | 169 | SEG15 | 2910 | 893 |
| 20 | RW_WR | -2730 | -925 | 70 | C1- | 770 | -925 | 120 | COM30 | 4618 | -741 | 170 | SEG16 | 2850 | 893 |
| 21 | E_RD | -2660 | -925 | 71 | C1+ | 840 | -925 | 121 | COM29 | 4618 | -681 | 171 | SEG17 | 2790 | 893 |
| 22 | VDD | -2590 | -925 | 72 | C1+ | 910 | -925 | 122 | COM28 | 4618 | -621 | 172 | SEG18 | 2730 | 893 |
| 23 | DB0 | -2520 | -925 | 73 | C1+ | 980 | -925 | 123 | COM27 | 4618 | -561 | 173 | SEG19 | 2670 | 893 |
| 24 | DB1 | -2450 | -925 | 74 | C1+ | 1050 | -925 | 124 | COM26 | 4618 | -501 | 174 | SEG20 | 2610 | 893 |
| 25 | DB2 | -2380 | -925 | 75 | C2+ | 1120 | -925 | 125 | COM25 | 4618 | -441 | 175 | SEG21 | 2550 | 893 |
| 26 | DB3 | -2310 | -925 | 76 | C2+ | 1190 | -925 | 126 | COM24 | 4618 | -381 | 176 | SEG22 | 2490 | 893 |
| 27 | DB4 | -2240 | -925 | 77 | C2+ | 1260 | -925 | 127 | COM23 | 4618 | -321 | 177 | SEG23 | 2430 | 893 |
| 28 | DB5 | -2170 | -925 | 78 | C2+ | 1330 | -925 | 128 | COM22 | 4618 | -261 | 178 | SEG24 | 2370 | 893 |
| 29 | DB6 | -2100 | -925 | 79 | C2- | 1400 | -925 | 129 | COM21 | 4618 | -201 | 179 | SEG25 | 2310 | 893 |
| 30 | DB7 | -2030 | -925 | 80 | C2- | 1470 | -925 | 130 | COM20 | 4618 | -141 | 180 | SEG26 | 2250 | 893 |
| 31 | VDD | -1960 | -925 | 81 | C2- | 1540 | -925 | 131 | COM19 | 4618 | -81 | 181 | SEG27 | 2190 | 893 |
| 32 | VDD | -1890 | -925 | 82 | C2- | 1610 | -925 | 132 | COM18 | 4618 | -21 | 182 | SEG28 | 2130 | 893 |
| 33 | VDD | -1820 | -925 | 83 | C4+ | 1680 | -925 | 133 | COM17 | 4618 | 39 | 183 | SEG29 | 2070 | 893 |
| 34 | VDD | -1750 | -925 | 84 | C4+ | 1750 | -925 | 134 | COM16 | 4618 | 99 | 184 | SEG30 | 2010 | 893 |
| 35 | VDD | -1680 | -925 | 85 | C4+ | 1820 | -925 | 135 | COM15 | 4618 | 159 | 185 | SEG31 | 1950 | 893 |
| 36 | VDD | -1610 | -925 | 86 | C4+ | 1890 | -925 | 136 | COM14 | 4618 | 219 | 186 | SEG32 | 1890 | 893 |
| 37 | VDD | -1540 | -925 | 87 | VSS | 1960 | -925 | 137 | COM13 | 4618 | 279 | 187 | SEG33 | 1830 | 893 |
| 38 | VCI | -1470 | -925 | 88 | REF | 2030 | -925 | 138 | COM12 | 4618 | 339 | 188 | SEG34 | 1770 | 893 |
| 39 | VCI | -1400 | -925 | 89 | VEXT | 2100 | -925 | 139 | COM11 | 4618 | 399 | 189 | SEG35 | 1710 | 893 |
| 40 | VCI | -1330 | -925 | 90 | VDD | 2170 | -925 | 140 | COM10 | 4618 | 459 | 190 | SEG36 | 1650 | 893 |
| 41 | VCI | -1260 | -925 | 91 | INTRS | 2240 | -925 | 141 | COM9 | 4618 | 519 | 191 | SEG37 | 1590 | 893 |
| 42 | VCI | -1190 | -925 | 92 | VSS | 2310 | -925 | 142 | COM8 | 4618 | 579 | 192 | SEG38 | 1530 | 893 |
| 43 | VCI | -1120 | -925 | 93 | V4 | 2380 | -925 | 143 | COM7 | 4618 | 639 | 193 | SEG39 | 1470 | 893 |
| 44 | VCI | -1050 | -925 | 94 | V4 | 2450 | -925 | 144 | DUMMY | 4618 | 719 | 194 | SEG40 | 1410 | 893 |
| 45 | VCI | -980 | -925 | 95 | V4 | 2520 | -925 | 145 | DUMMY | 4370 | 893 | 195 | SEG41 | 1350 | 893 |
| 46 | VSS1 | -910 | -925 | 96 | V4 | 2590 | -925 | 146 | COM6 | 4290 | 893 | 196 | SEG42 | 1290 | 893 |
| 47 | VSS1 | -840 | -925 | 97 | V3 | 2660 | -925 | 147 | COM5 | 4230 | 893 | 197 | SEG43 | 1230 | 893 |
| 48 | VSS1 | -770 | -925 | 98 | V3 | 2730 | -925 | 148 | COM4 | 4170 | 893 | 198 | SEG44 | 1170 | 893 |
| 49 | VSS1 | -700 | -925 | 99 | V3 | 2800 | -925 | 149 | COM3 | 4110 | 893 | 199 | SEG45 | 1110 | 893 |
| 50 | VSS2 | -630 | -925 | 100 | V3 | 2870 | -925 | 150 | COM2 | 4050 | 893 | 200 | SEG46 | 1050 | 893 |

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

| NO. | Name | X | Y | NO. | Name | X | Y | NO. | Name | X | Y |
|-----|-------|-------|-----|-----|--------|-------|-----|-----|-------|-------|------|
| 201 | SEG47 | 990 | 893 | 251 | SEG97 | -2010 | 893 | 301 | COM49 | -4618 | 99 |
| 202 | SEG48 | 930 | 893 | 252 | SEG98 | -2070 | 893 | 302 | COM50 | -4618 | 39 |
| 203 | SEG49 | 870 | 893 | 253 | SEG99 | -2130 | 893 | 303 | COM51 | -4618 | -21 |
| 204 | SEG50 | 810 | 893 | 254 | SEG100 | -2190 | 893 | 304 | COM52 | -4618 | -81 |
| 205 | SEG51 | 750 | 893 | 255 | SEG101 | -2250 | 893 | 305 | COM53 | -4618 | -141 |
| 206 | SEG52 | 690 | 893 | 256 | SEG102 | -2310 | 893 | 306 | COM54 | -4618 | -201 |
| 207 | SEG53 | 630 | 893 | 257 | SEG103 | -2370 | 893 | 307 | COM55 | -4618 | -261 |
| 208 | SEG54 | 570 | 893 | 258 | SEG104 | -2430 | 893 | 308 | COM56 | -4618 | -321 |
| 209 | SEG55 | 510 | 893 | 259 | SEG105 | -2490 | 893 | 309 | COM57 | -4618 | -381 |
| 210 | SEG56 | 450 | 893 | 260 | SEG106 | -2550 | 893 | 310 | COM58 | -4618 | -441 |
| 211 | SEG57 | 390 | 893 | 261 | SEG107 | -2610 | 893 | 311 | COM59 | -4618 | -501 |
| 212 | SEG58 | 330 | 893 | 262 | SEG108 | -2670 | 893 | 312 | COM60 | -4618 | -561 |
| 213 | SEG59 | 270 | 893 | 263 | SEG109 | -2730 | 893 | 313 | COM61 | -4618 | -621 |
| 214 | SEG60 | 210 | 893 | 264 | SEG110 | -2790 | 893 | 314 | COM62 | -4618 | -681 |
| 215 | SEG61 | 150 | 893 | 265 | SEG111 | -2850 | 893 | 315 | COM63 | -4618 | -741 |
| 216 | SEG62 | 90 | 893 | 266 | SEG112 | -2910 | 893 | 316 | COM64 | -4618 | -801 |
| 217 | SEG63 | 30 | 893 | 267 | SEG113 | -2970 | 893 | 317 | DUMMY | -4618 | -881 |
| 218 | SEG64 | -30 | 893 | 268 | SEG114 | -3030 | 893 | | | | |
| 219 | SEG65 | -90 | 893 | 269 | SEG115 | -3090 | 893 | | | | |
| 220 | SEG66 | -150 | 893 | 270 | SEG116 | -3150 | 893 | | | | |
| 221 | SEG67 | -210 | 893 | 271 | SEG117 | -3210 | 893 | | | | |
| 222 | SEG68 | -270 | 893 | 272 | SEG118 | -3270 | 893 | | | | |
| 223 | SEG69 | -330 | 893 | 273 | SEG119 | -3330 | 893 | | | | |
| 224 | SEG70 | -390 | 893 | 274 | SEG120 | -3390 | 893 | | | | |
| 225 | SEG71 | -450 | 893 | 275 | SEG121 | -3450 | 893 | | | | |
| 226 | SEG72 | -510 | 893 | 276 | SEG122 | -3510 | 893 | | | | |
| 227 | SEG73 | -570 | 893 | 277 | SEG123 | -3570 | 893 | | | | |
| 228 | SEG74 | -630 | 893 | 278 | SEG124 | -3630 | 893 | | | | |
| 229 | SEG75 | -690 | 893 | 279 | SEG125 | -3690 | 893 | | | | |
| 230 | SEG76 | -750 | 893 | 280 | SEG126 | -3750 | 893 | | | | |
| 231 | SEG77 | -810 | 893 | 281 | SEG127 | -3810 | 893 | | | | |
| 232 | SEG78 | -870 | 893 | 282 | COM32 | -3870 | 893 | | | | |
| 233 | SEG79 | -930 | 893 | 283 | COM33 | -3930 | 893 | | | | |
| 234 | SEG80 | -990 | 893 | 284 | COM34 | -3990 | 893 | | | | |
| 235 | SEG81 | -1050 | 893 | 285 | COM35 | -4050 | 893 | | | | |
| 236 | SEG82 | -1110 | 893 | 286 | COM36 | -4110 | 893 | | | | |
| 237 | SEG83 | -1170 | 893 | 287 | COM37 | -4170 | 893 | | | | |
| 238 | SEG84 | -1230 | 893 | 288 | COM38 | -4230 | 893 | | | | |
| 239 | SEG85 | -1290 | 893 | 289 | COM39 | -4290 | 893 | | | | |
| 240 | SEG86 | -1350 | 893 | 290 | DUMMY | -4370 | 893 | | | | |
| 241 | SEG87 | -1410 | 893 | 291 | DUMMY | -4618 | 719 | | | | |
| 242 | SEG88 | -1470 | 893 | 292 | COM40 | -4618 | 639 | | | | |
| 243 | SEG89 | -1530 | 893 | 293 | COM41 | -4618 | 579 | | | | |
| 244 | SEG90 | -1590 | 893 | 294 | COM42 | -4618 | 519 | | | | |
| 245 | SEG91 | -1650 | 893 | 295 | COM43 | -4618 | 459 | | | | |
| 246 | SEG92 | -1710 | 893 | 296 | COM44 | -4618 | 399 | | | | |
| 247 | SEG93 | -1770 | 893 | 297 | COM45 | -4618 | 339 | | | | |
| 248 | SEG94 | -1830 | 893 | 298 | COM46 | -4618 | 279 | | | | |
| 249 | SEG95 | -1890 | 893 | 299 | COM47 | -4618 | 219 | | | | |
| 250 | SEG96 | -1950 | 893 | 300 | COM48 | -4618 | 159 | | | | |

PIN DESCRIPTION

POWER SUPPLY

Table 1. Power Supply Pins

| Name | I/O | Description | | | | | | | | | | |
|----------------------------|-----------------------|--|-------------------|-------------------|----|----|----|----------|-----------------------|-----------------------|-------------------|-------------------|
| VDD | Supply | Power supply | | | | | | | | | | |
| VSS1 VSS2 | Supply | Ground NOTE: VSS1 and VSS2 must be shorted to external wire. | | | | | | | | | | |
| V0 V1 V2 V3 V4 | I/O | <p>LCD driver supplies voltages The voltage determined by LCD pixel is impedance converted by an operational amplifier for application. Voltages should have the following relationship; $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq Vss$ When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</p> <table border="1"> <thead> <tr> <th>LCD bias</th> <th>V1</th> <th>V2</th> <th>V3</th> <th>V4</th> </tr> </thead> <tbody> <tr> <td>1/N bias</td> <td>$(N-1) / N \times V0$</td> <td>$(N-2) / N \times V0$</td> <td>$(2/N) \times V0$</td> <td>$(1/N) \times V0$</td> </tr> </tbody> </table> <p>NOTE: N = 4 to 9</p> | LCD bias | V1 | V2 | V3 | V4 | 1/N bias | $(N-1) / N \times V0$ | $(N-2) / N \times V0$ | $(2/N) \times V0$ | $(1/N) \times V0$ |
| LCD bias | V1 | V2 | V3 | V4 | | | | | | | | |
| 1/N bias | $(N-1) / N \times V0$ | $(N-2) / N \times V0$ | $(2/N) \times V0$ | $(1/N) \times V0$ | | | | | | | | |

LCD DRIVER SUPPLY

Table 2. LCD Driver Supply Pins

| Name | I/O | Description |
|------|-----|--|
| C1- | O | Capacitor 1 negative connection pin for voltage converter |
| C1+ | O | Capacitor 1 positive connection pin for voltage converter |
| C2- | O | Capacitor 2 negative connection pin for voltage converter |
| C2+ | O | Capacitor 2 positive connection pin for voltage converter |
| C3+ | O | Capacitor 3 positive connection pin for voltage converter |
| C4+ | O | Capacitor 4 positive connection pin for voltage converter |
| VOUT | I/O | Voltage converter input / output pin |
| VCI | I | Voltage converter input voltage pin Voltages should have the following relationship: $VDD \leq VCI \leq V0$ |
| VR | I | V0 voltage adjustment pin It is valid only when on-chip resistors are not used (INTRS = "L") |
| REF | I | Selects the external VREF voltage via VEXT pin – REF = "L": using the external VREF – REF = "H": using the internal VREF |
| VEXT | I | Externally input reference voltage (VREF) for the internal voltage regulator It is valid only when REF is "L". |

SYSTEM CONTROL**Table 3. System Control Pins**

| Name | I/O | Description |
|----------------------|-----|--|
| INTRS | I | Internal resistors select pin This pin selects the resistors for adjusting V0 voltage level. – INTRS = "H": use the internal resistors – INTRS = "L": use the external resistors VR pin and external resistive divider control V0 voltage. |
| TEST1 to TEST4 | I | Test pins Don't use these pins. |

MICROPROCESSOR INTERFACE

Table 4. Microprocessor Interface Pins

| Name | I/O | Description | | | | | |
|---|-----|---|----------------|------------------|---|---------------|--------------|
| RESETB | I | Reset the input pin When RESETB is "L", initialization is executed. | | | | | |
| PS0 | I | Parallel/Serial data input select input | | | | | |
| | | PS0 | Interface Mode | Data/Instruction | Data | Read / Write | Serial Clock |
| | | H | Parallel | RS | DB0 to DB7 | E_RD RW_WR | - |
| | | L | Serial | RS or None | SID(DB7) | Write only | SCLK(DB6) |
| *NOTE: When PS is "L", DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either "H" or "L". | | | | | | | |
| PS1 | I | Microprocessor interface select input pin <ul style="list-style-type: none"> - PS0 = "H", PS1 = "H": 6800-series parallel MPU interface - PS0 = "H", PS1 = "L": 8080-series parallel MPU interface - PS0 = "L", PS1 = "H": 4 Pin-SPI serial MPU interface - PS0 = "L", PS1 = "L": 3 Pin-SPI serial MPU interface | | | | | |
| CS1B | I | Chip select input pins Data/Instruction I/O is enabled only when CS1B is "L". When chip select is non-active, DB0 to DB7 may be high impedance. | | | | | |
| RS | I | Register select input pin <ul style="list-style-type: none"> - RS = "H": DB0 to DB7 are display data - RS = "L": DB0 to DB7 are control data | | | | | |
| RW_WR | I | Read / Write execution control pin | | | | | |
| | | PS1 | MPU Type | RW_WR | Description | | |
| | | H | 6800-series | RW | Read/Write control input pin <ul style="list-style-type: none"> - RW = "H": read - RW = "L": write | | |
| | | L | 8080-series | /WR | Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the /WR signal. | | |

Table 6 (Continued)

| Name | I/O | Description | | | |
|------------|-----|---|-------------|------|---|
| E_RD | I | Read / Write execution control pin | | | |
| | | PS1 | MPU Type | E_RD | Description |
| | | H | 6800-series | E | Read/Write control input pin – RW = "H": When E is "H", DB0 to DB7 are in an output status. – RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal. |
| | | L | 8080-series | /RD | Read enable clock input pin When /RD is "L", DB0 to DB7 are in an output status. |
| DB0 to DB7 | I/O | 8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS0 = "L"); – DB0 to DB5: high impedance – DB6: serial input clock (SCLK) – DB7: serial input data (SID) When chip select is not active, DB0 to DB7 may be high impedance. | | | |

LCD DRIVER OUTPUTS

Table 5. LCD Driver Outputs Pins

| Name | I/O | Description | | | |
|----------------------|-----|--|--------------|-------------------------------|-----------------|
| SEG0 to SEG127 | O | LCD segment driver outputs The display data and the M signal control the output voltage of segment driver. | | | |
| | | Display data | M (Internal) | Segment driver output voltage | |
| | | | | Normal display | Reverse display |
| | | H | H | V0 | V2 |
| | | H | L | Vss | V3 |
| | | L | H | V2 | V0 |
| | | L | L | V3 | Vss |
| | | Power save mode | | Vss | Vss |
| COM0 to COM63 | O | LCD common driver outputs The internal scanning data and M signal control the output voltage of common driver. | | | |
| | | Scan data | M (Internal) | Common driver output voltage | |
| | | | | Vss | |
| | | H | L | V0 | |
| | | L | H | V1 | |
| | | L | L | V4 | |
| | | Power save mode | | Vss | |
| COMS (COMS1) | O | Common output for the icons The output signals of two pins are same. When not used, these pins should be left open. | | | |

NOTE: **DUMMY** – These pins should be opened (floated).

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B for chip selection. The S6B0755 can interface with an MPU only when CS1B is "L". When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

S6B0755 has four types of interface with an MPU, which are two serial and two parallel interface. This parallel or serial interface is determined by PS 0pin as shown in Table 6.

Table 6. Parallel / Serial Interface Mode

| PS0 | Type | CS1B | PS1 | Interface mode |
|-----|----------|------|-----|----------------------|
| H | Parallel | CS1B | H | 6800-series MPU mode |
| | | | L | 8080-series MPU mode |
| L | Serial | CS1B | H | 4 Pin-SPI MPU mode |
| | | | L | 3 Pin-SPI MPU mode |

Parallel Interface (PS0 = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in Table 7. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in Table 8.

Table 7. Microprocessor Selection for Parallel Interface

| PS1 | CS1B | RS | E_RD | RW_WR | DB0 to DB7 | MPU bus |
|-----|------|----|------|-------|------------|-------------|
| H | CS1B | RS | E | RW | DB0 to DB7 | 6800-series |
| L | CS1B | RS | /RD | /WR | DB0 to DB7 | 8080-series |

Table 8. Parallel Data Transfer

| Common | 6800-series | | 8080-series | | Description |
|--------|-------------|------------|-------------|-------------|---|
| | E_RD (E) | RW_WR (RW) | E_RD (/RD) | RW_WR (/WR) | |
| RS | | | | | |
| H | H | H | L | H | Display data read out |
| H | H | L | H | L | Display data write |
| L | H | H | L | H | Register status read |
| L | H | L | H | L | Writes to internal register (instruction) |

NOTE: When E_RD pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at RS, RW_WR as in case of 6800-series mode.

Serial Interface (PS0 = "L")

When the S6B0755 is active(CS1B="L"), serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select(RS) Pin, based on the setting of PS1. When the RS pin is used (PS1 = "H"), data is display data when RS is high, and command data when RS is low. When RS is not used (PS1 = "L"), the LCD Driver will receive command from MPU by default. If messages on the data pin are data rather than command, MPU should send Data Direction command(11101000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are send, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

| Serial Mode | PS0 | PS1 | CS1B | RS |
|-----------------------------------|-----|-----|------|----------|
| Serial-mode with RS pin | L | H | CS1B | Used |
| Serial-mode with software command | L | L | CS1B | Not used |

4 Pin-SPI Interface (PS0 = "L" , PS1 = "H")

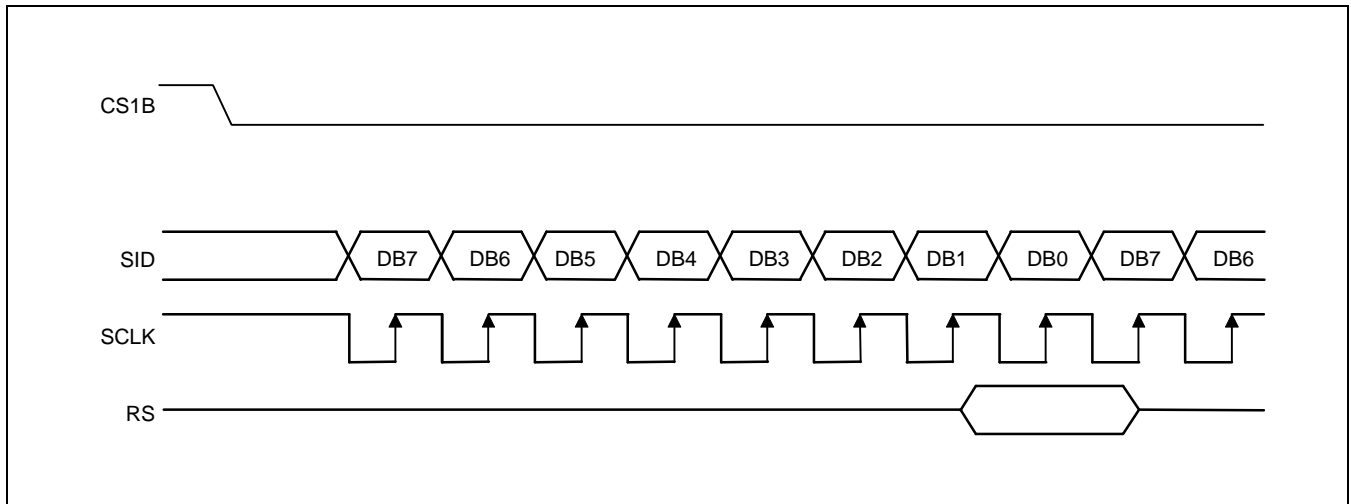


Figure 3. 4 Pin SPI Timing (RS is used)

3 Pin-SPI Interface (PS0 = "L" , PS1 = "L")

To write data to the DDRAM, send Data Direction Command in 3-Pin SPI mode. Data is latched at the rising edge of SCLK. And the DDRAM column address pointer will be increased by one automatically.

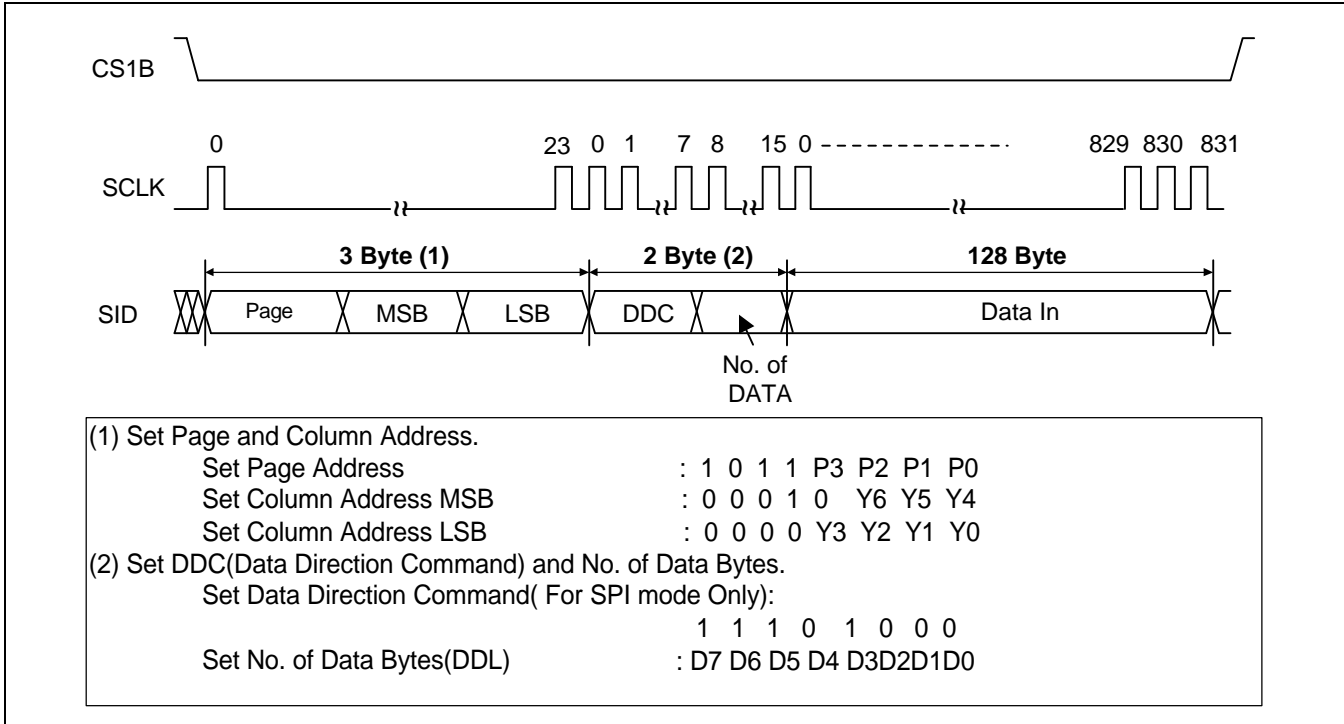


Figure 4. 3 Pin SPI Timing (RS is not used)

This command is used in 3-Pin SPI mode only. It will be two continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data. New data will be transferred serially with most significant bit first.

Notes:

- In spite of transmission of data, if CS1B will be disable, state terminates abnormally. Next state is initialized.
- DDL Register value "0" → "1" , "127" → "128". (decimal value)

Busy Flag

The Busy Flag indicates whether the S6B0755 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B0755 uses bus holder and internal data bus for Data Transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 5. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 6. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

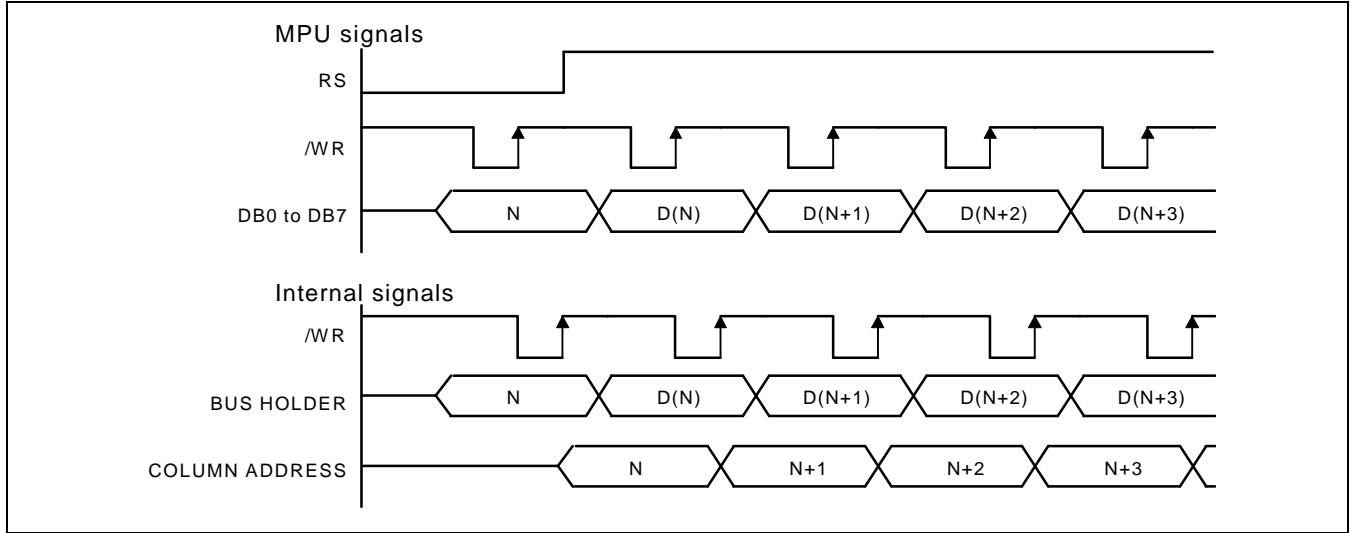


Figure 5. Write Timing

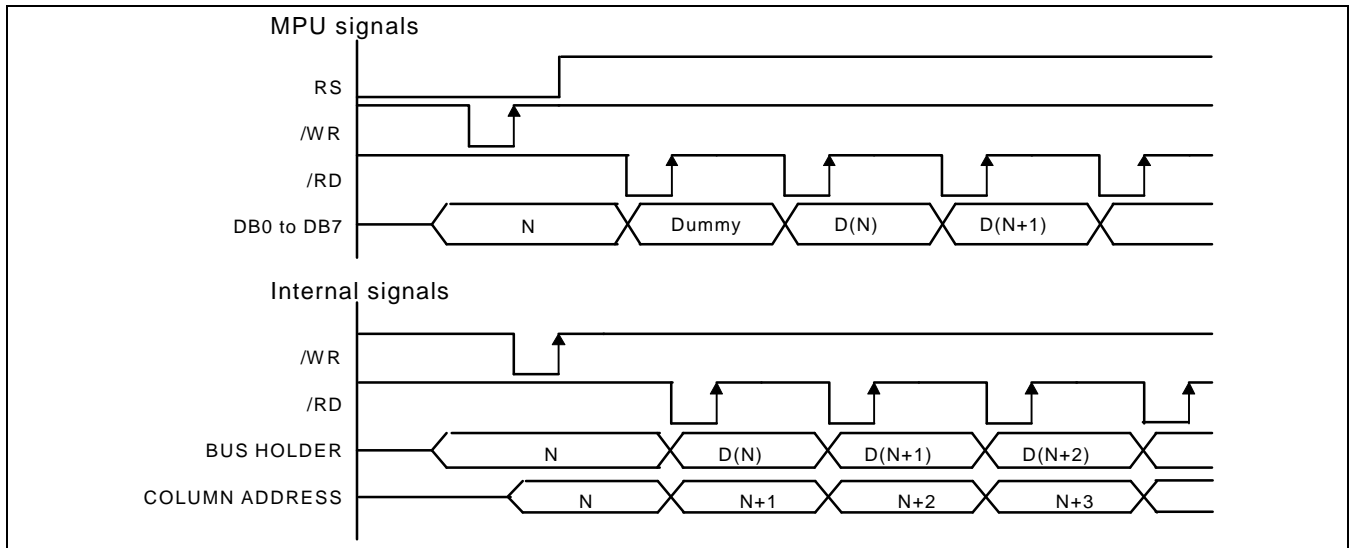


Figure 6. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in Figure 7. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

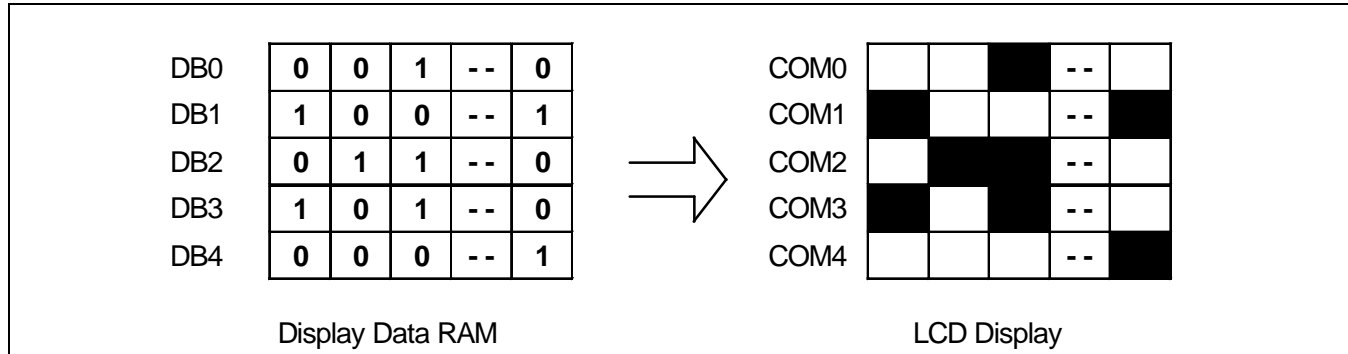


Figure 7. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in Figure 9. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 8 (DB3 is "H", DB2, DB1 and DB0 is "L") is a special RAM area for the icons and display data DB0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in Figure 9 & Figure 10. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 128-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column address circuit has a 7-bit preset counter that provides column address to the Display Data RAM as shown in Figure 9. When set Column Address MSB / LSB instruction is issued, 7-bit [Y6:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. And the Column Address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following Figure 8.

| SEG output | SEG 0 | SEG 1 | SEG 2 | SEG 3 | | SEG 124 | SEG 125 | SEG 126 | SEG 127 |
|----------------------------------|-------|-------|-------|-------|--------|---------|---------|---------|---------|
| Column address [Y6:Y0] | 00H | 01H | 02H | 03H | | 7CH | 7DH | 7EH | 7FH |
| Display data | 1 | 0 | 1 | 0 | | 1 | 1 | 0 | 0 |
| LCD panel display (ADC = 0) | | | | | | | | | |
| | | | | | | | | | |
| LCD panel display (ADC = 1) | | | | | | | | | |

Figure 8. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the Display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

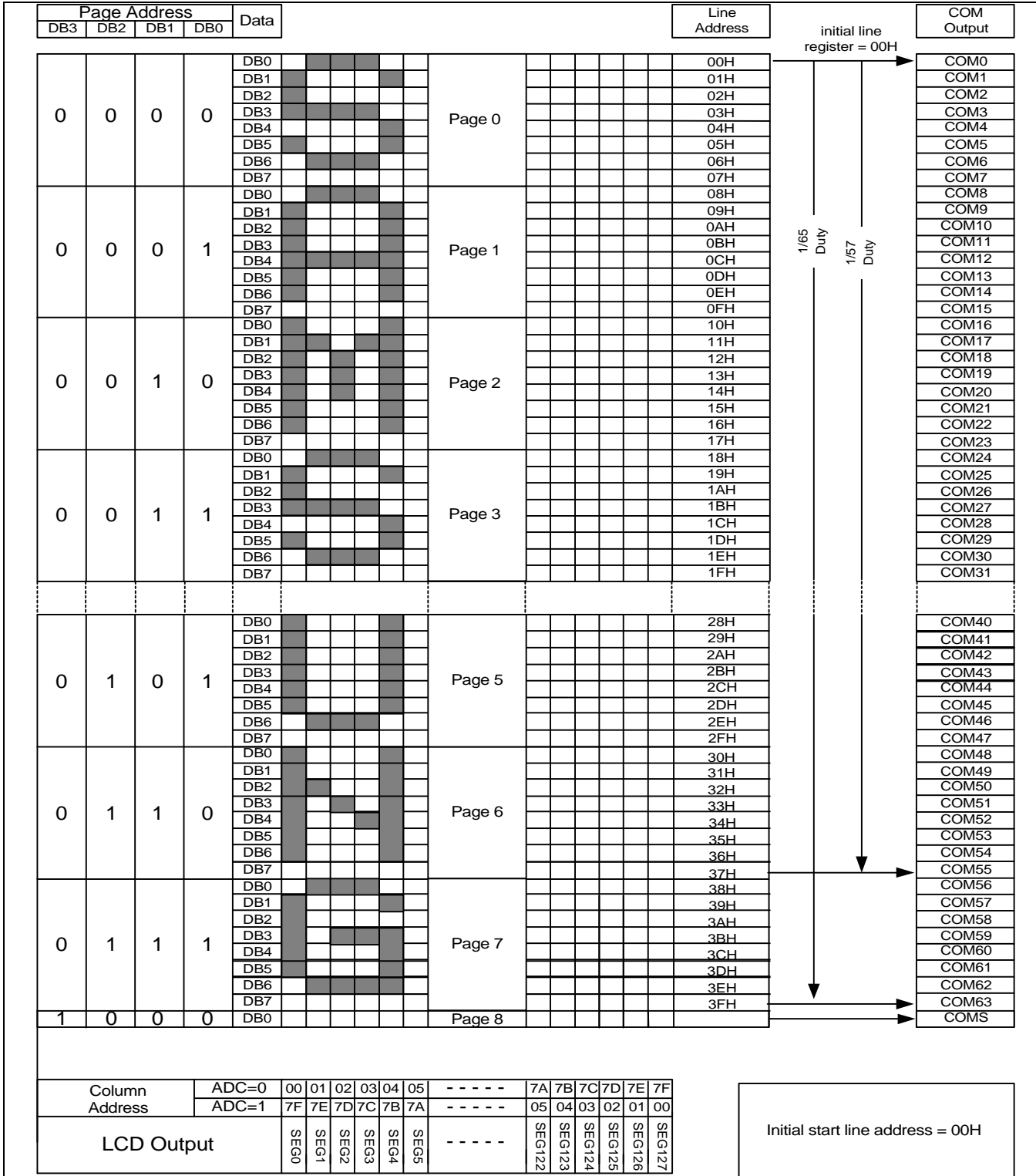


Figure 9. Display Data RAM Map (Initial Line Address = 00H)

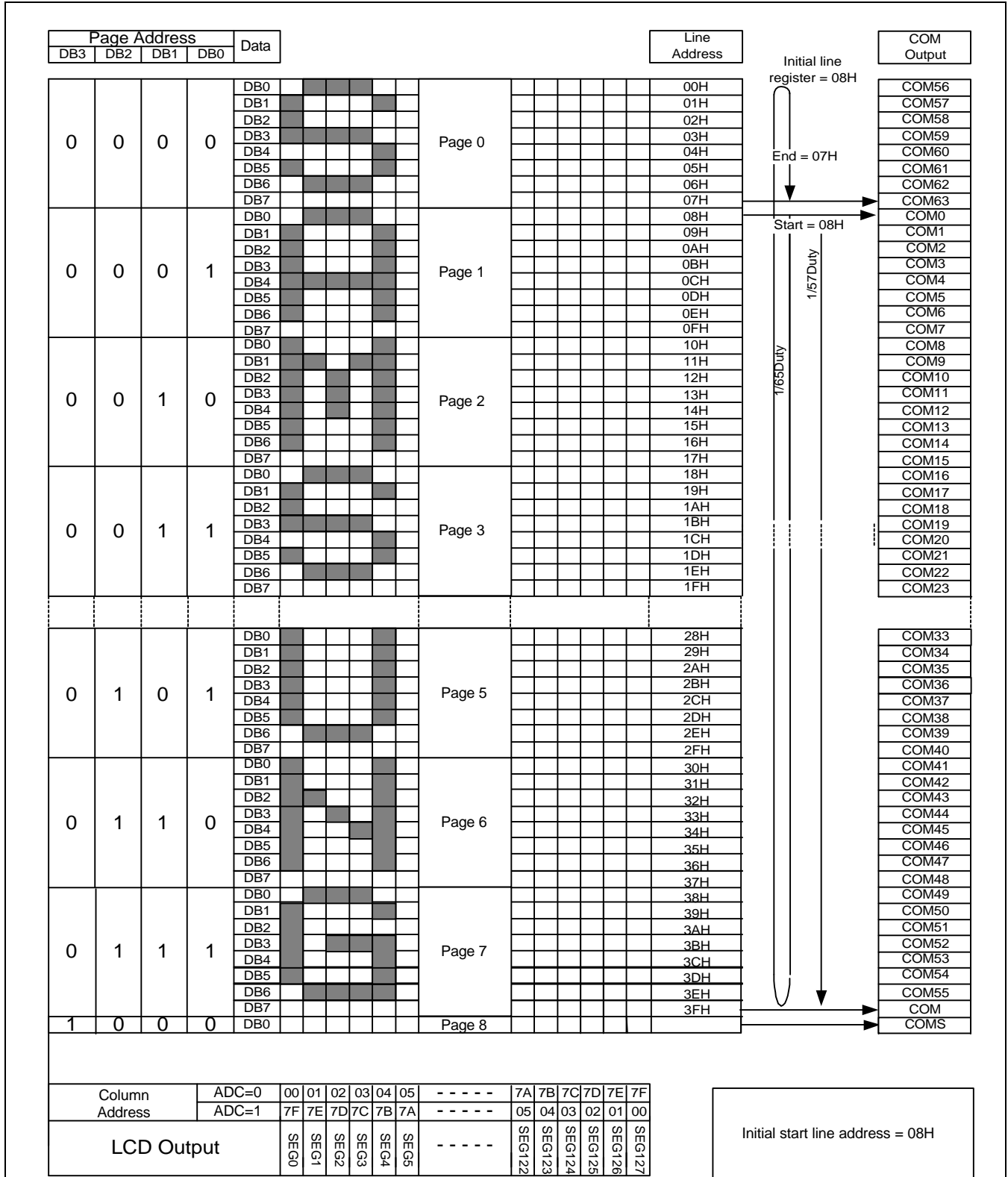


Figure 10. Display Data RAM Map (Initial Line Address = 08H)

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip Oscillator and its frequency is nearly independent of VDD. This Oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL(internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 11.

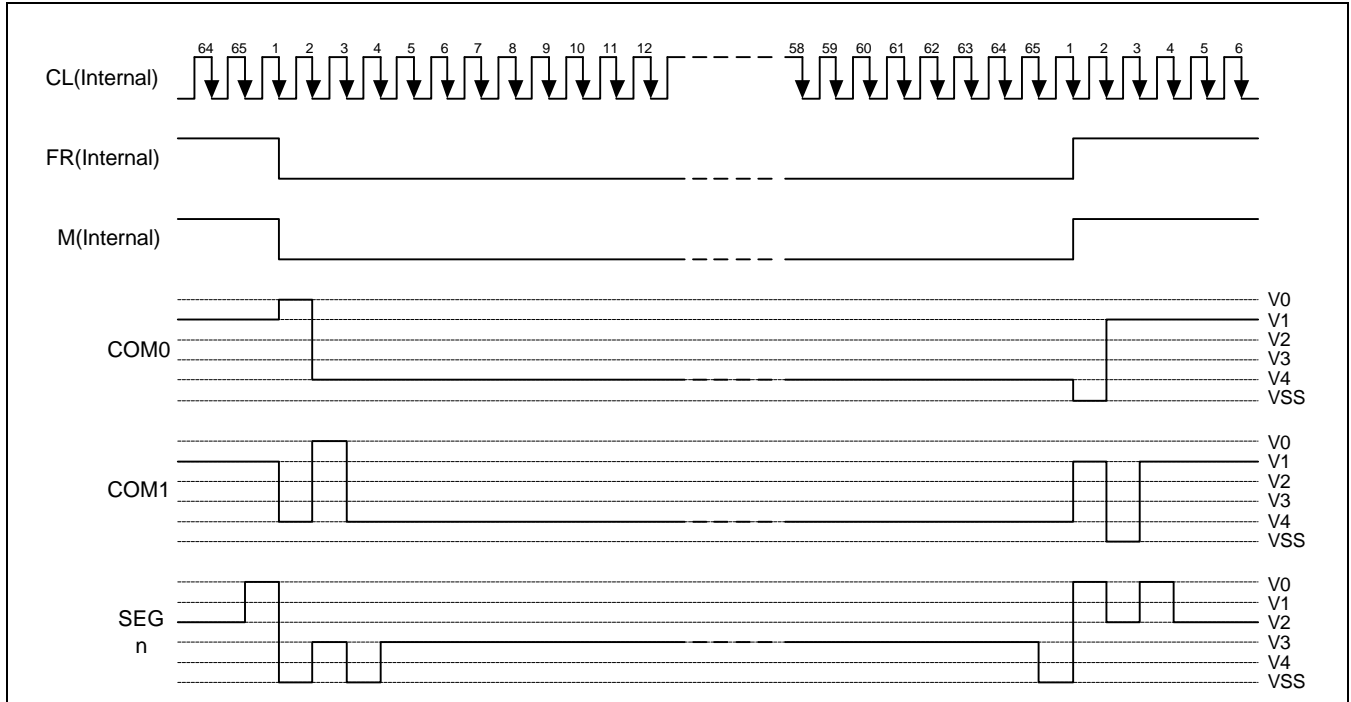


Figure 11. 2-frame AC Driving Waveform (Duty Ratio = 1/65)

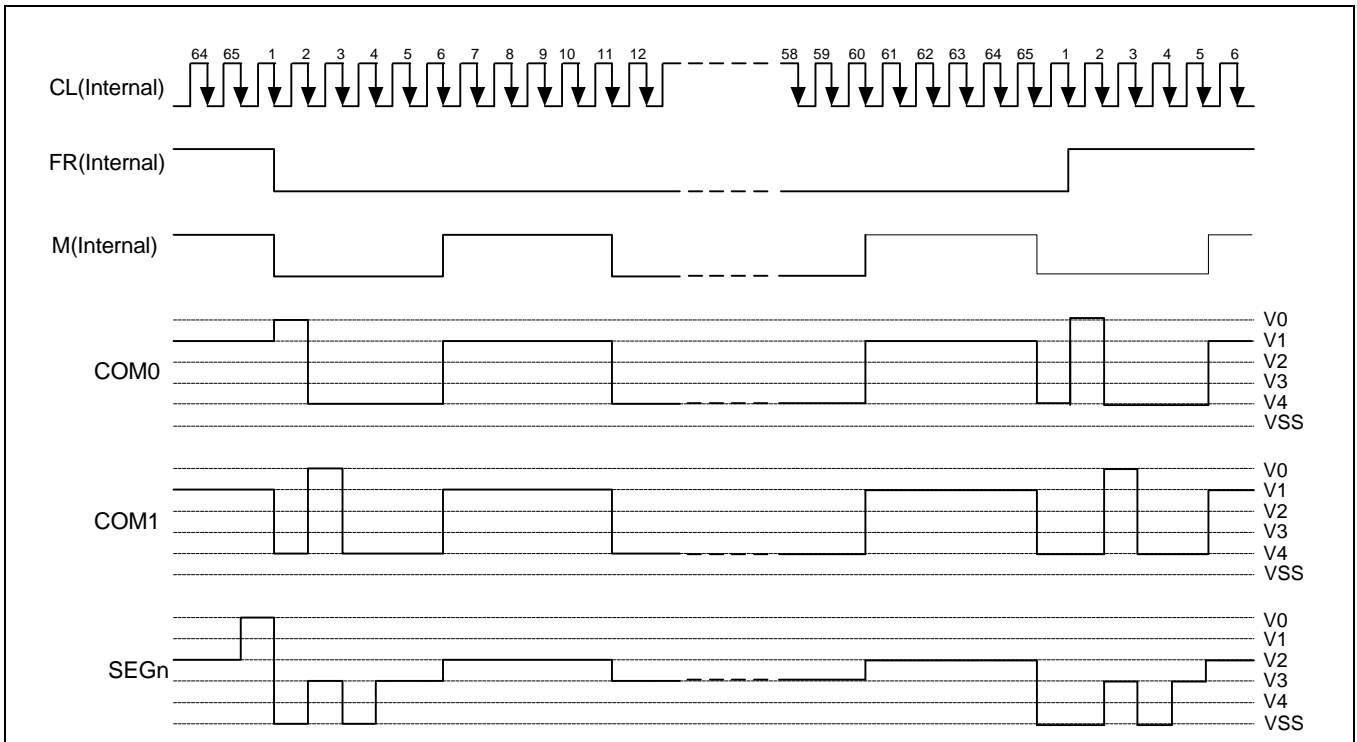


Figure 12. N-line Inversion Driving Waveform (N = 5 , Duty Ratio = 1/65)

LCD DRIVER CIRCUIT

65-channel common driver and 128-channel segment driver configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and M(internal) signal.

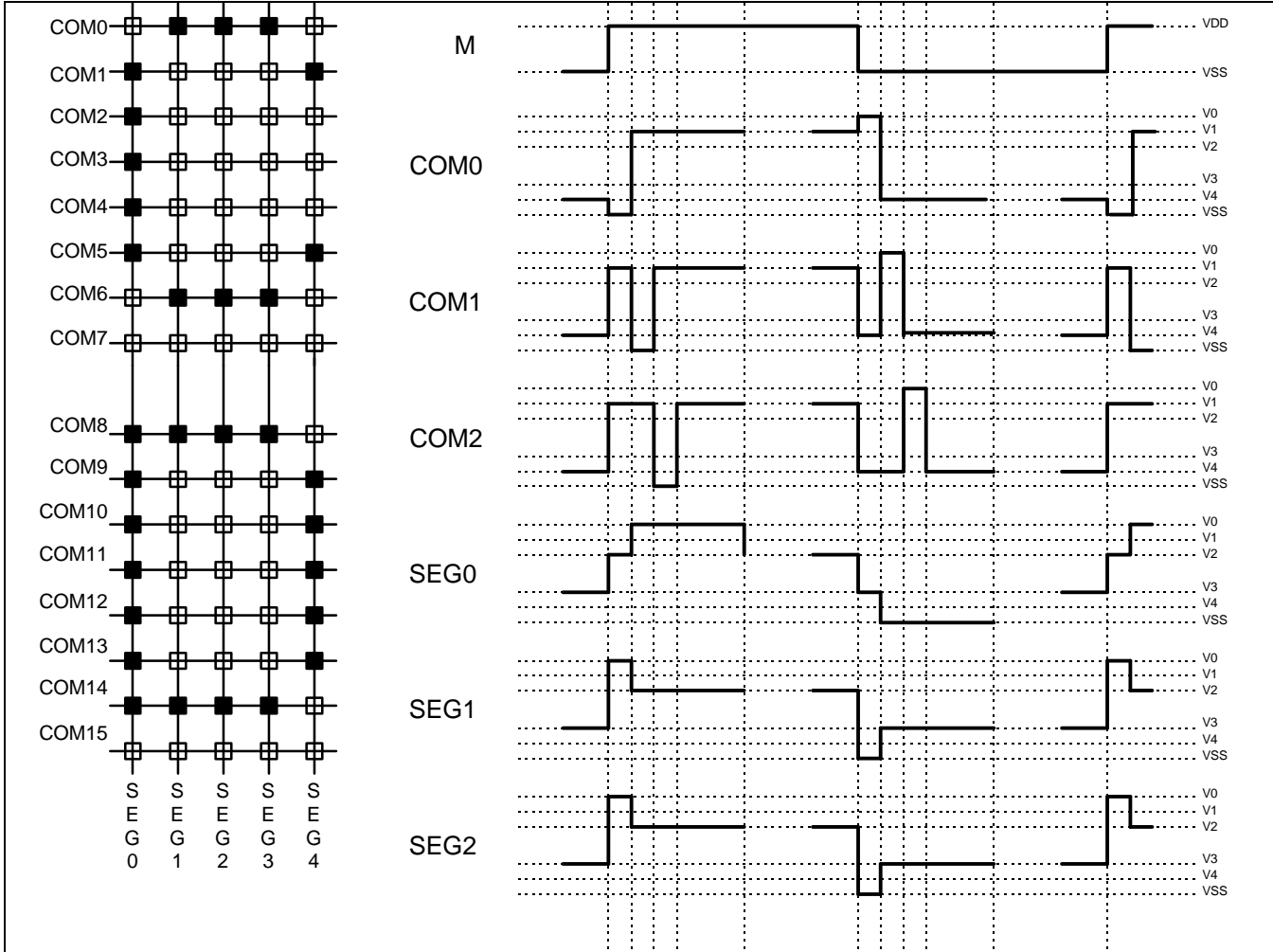


Figure 13. Segment and Common Timing

Partial Display on LCD

The S6B0755 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages

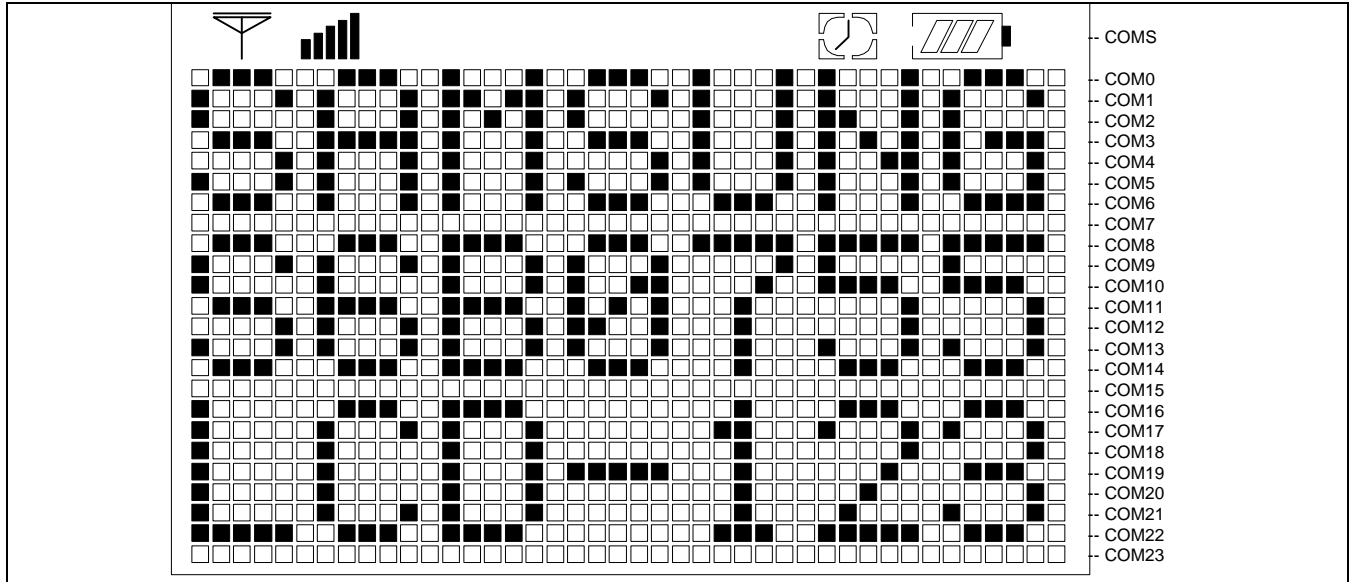


Figure 14. Reference Example for Partial Display (Display Duty = 25)

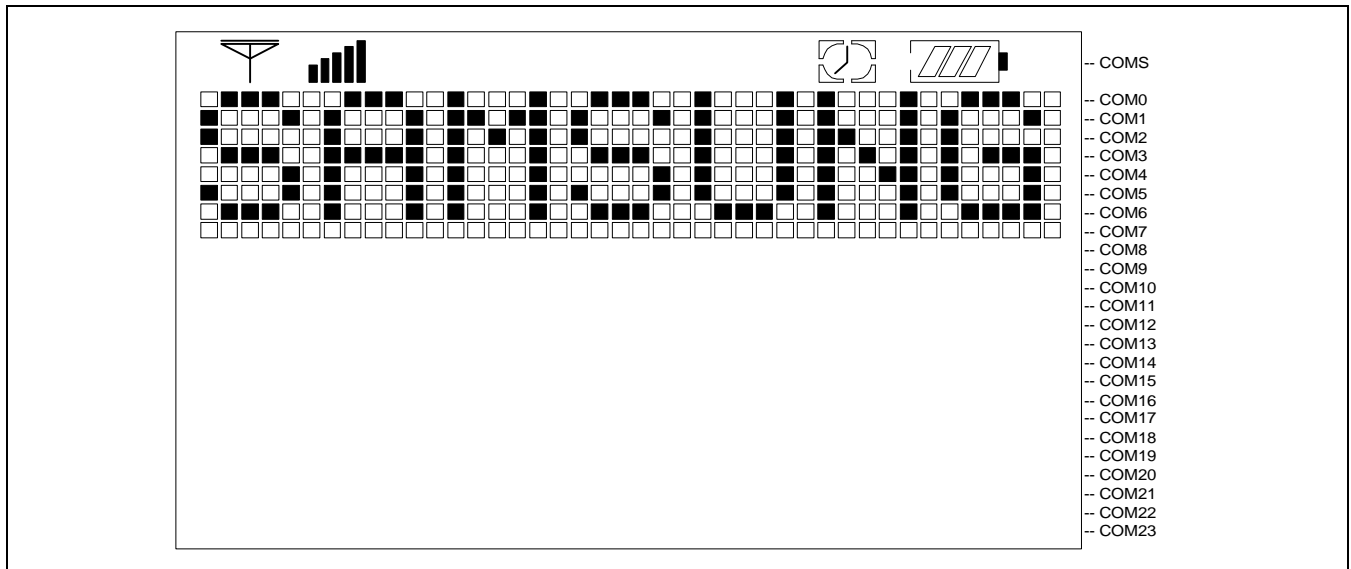


Figure 15. Partial Display (Partial Display Duty = 9, Initial COM0 = 0)

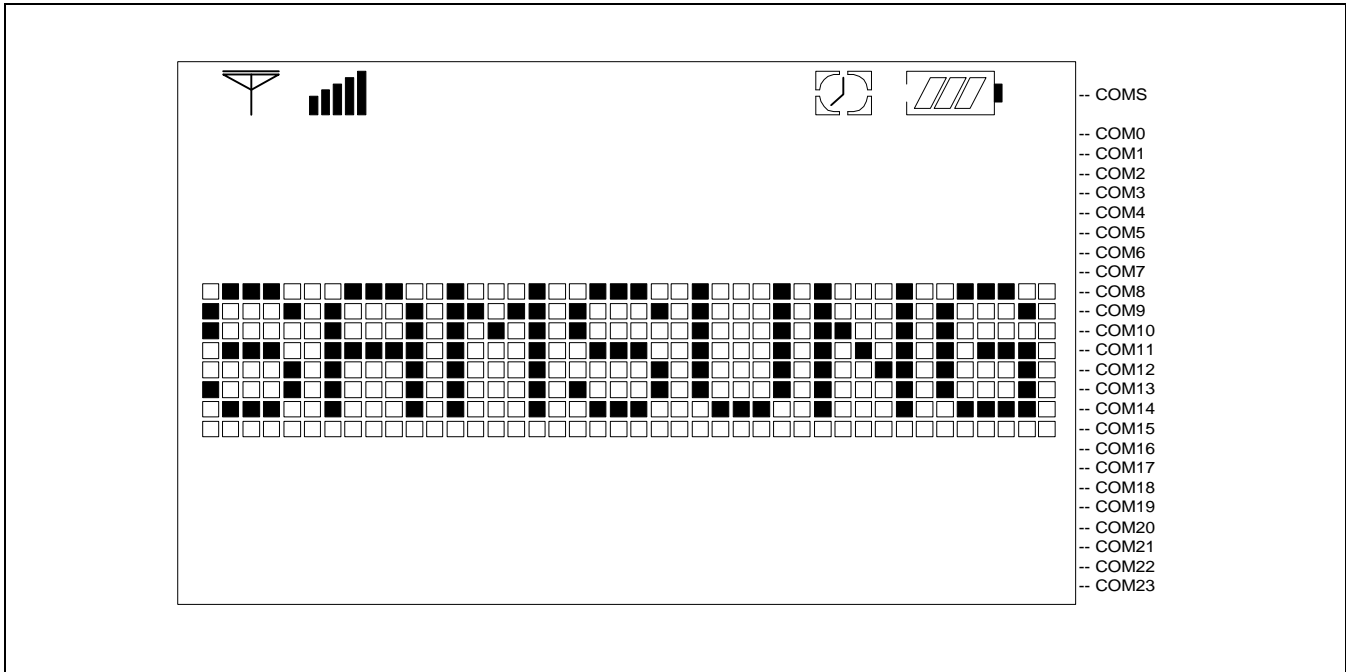


Figure 16. Moving Display (Partial Display Duty = 9, Initial COM0 = 8)

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 9 shows the referenced combinations in using Power Supply circuits.

Table 9. Recommended Power Supply Combinations

| User setup | Power control (VC VR VF) | V/C circuits | V/R circuits | V/F circuits | VOUT | V0 | V1 to V4 |
|--|-----------------------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|
| Only the internal power supply circuits are used | 1 1 1 | ON | ON | ON | Open | Open | Open |
| Only the voltage regulator circuits and voltage follower circuits are used | 0 1 1 | OFF | ON | ON | External input | Open | Open |
| Only the voltage follower circuits are used | 0 0 1 | OFF | OFF | ON | Open | External input | Open |
| Only the external power supply circuits are used | 0 0 0 | OFF | OFF | OFF | Open | External input | External input |

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by "Set DC-DC Step-up" instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

[C1 = 1.0 to 4.7 nF]

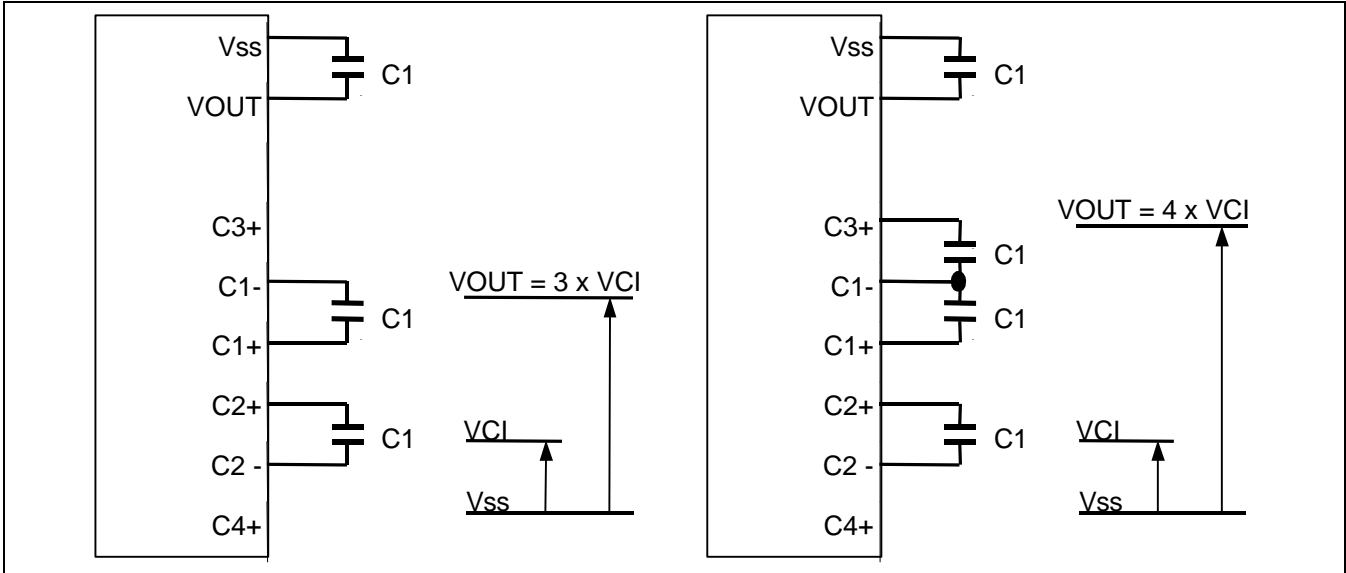


Figure 17. Three Times Boosting Circuit

Figure 18. Four Times Boosting Circuit

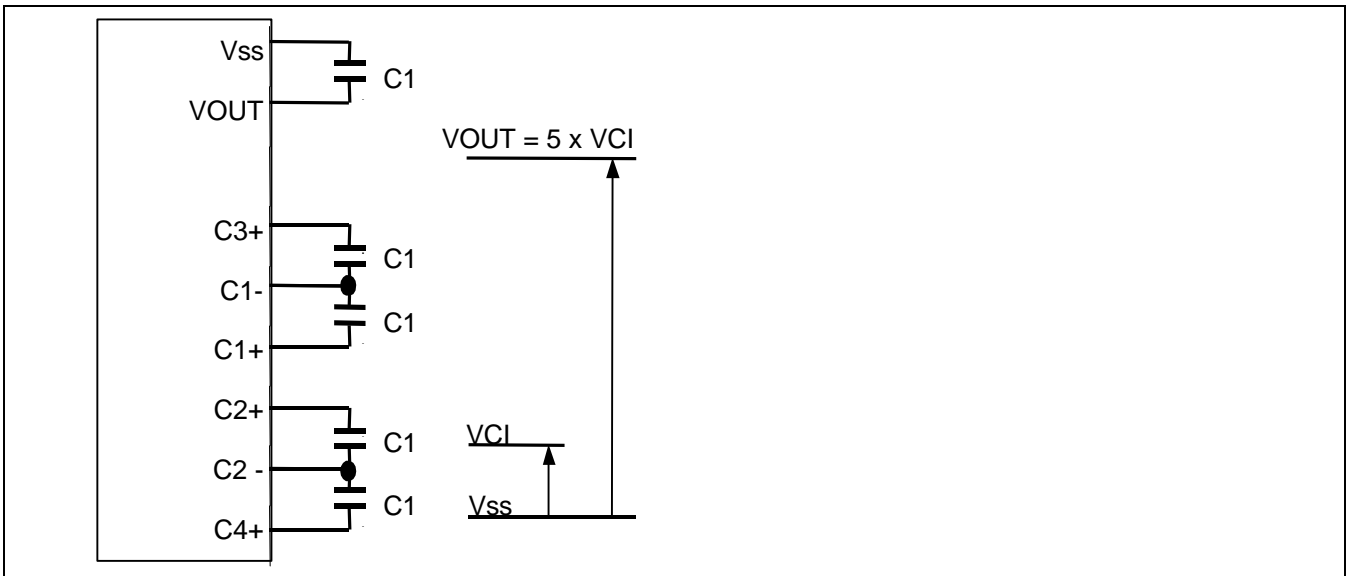


Figure 19. Five Times Boosting Circuit

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V_0 , by adjusting resistors, R_a and R_b , within the range of $|V_0| < |V_{OUT}|$. Because V_{OUT} is the operating voltage of operational-amplifier circuits shown in Figure 20, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V_0 by R_a , R_b and V_{EV} . The R_a and R_b are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at $T_a = 25^\circ\text{C}$ is shown in Table 10.

$$V_0 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV} \quad [\text{V}] \quad \text{----- (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{210}\right) \times V_{REF} \quad [\text{V}] \quad \text{----- (Eq. 2)}$$

Table 10. . V_{REF} Voltage at $T_a = 25^\circ\text{C}$

| REF | Temp. coefficient | V_{REF} [V] |
|-----|-------------------|-----------------|
| 1 | -0.05% / °C | 2.1 |
| 0 | External input | V_{EXT} |

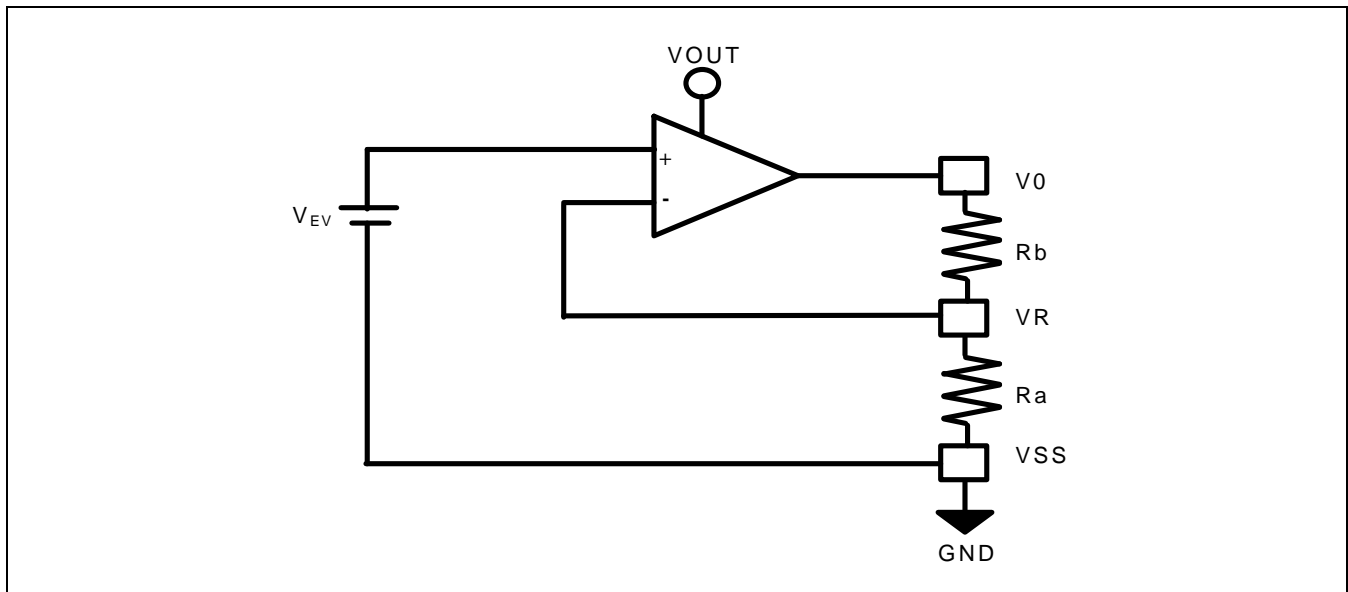


Figure 20. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 11. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

| | 3-bit data settings (R2 R1 R0) | | | | | | | |
|---------------|--------------------------------|-------|-------|-------|-------|-------|-------|-------|
| | 0 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1 0 0 | 1 0 1 | 1 1 0 | 1 1 1 |
| 1 + (Rb / Ra) | 2.3 | 3.0 | 3.7 | 4.4 | 5.1 | 5.8 | 6.5 | 7.2 |

Figure 21 Shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

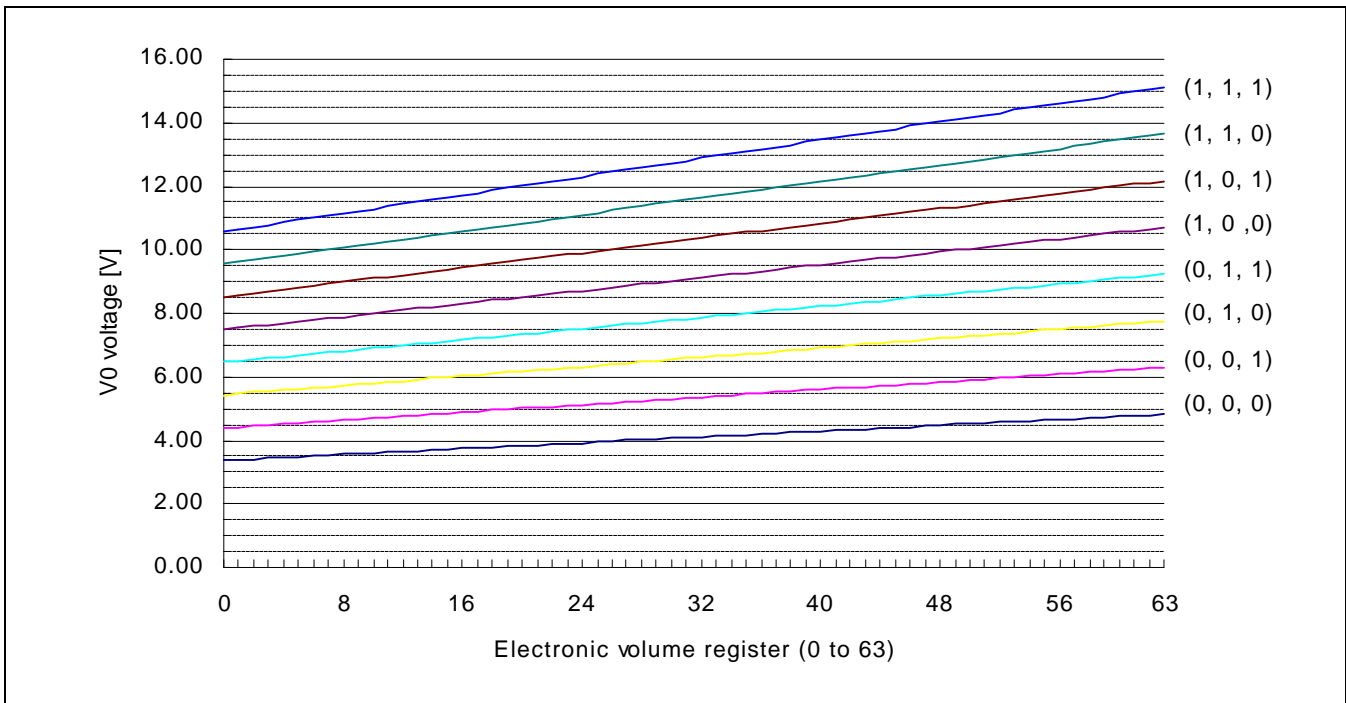


Figure 21. Electronic Volume Level (Temp. Coefficient = -0.05% / °C)

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV} \quad [V] \text{ ----- (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(63 - 32)}{210}\right) \times 2.1 = 1.79 \quad [V] \text{ ----- (Eq. 4)}$$

From requirement 3.

$$\frac{10}{R_a + R_b} = 1 \quad [\mu A] \text{ ----- (Eq. 5)}$$

From equations Eq. 3, 4 and 5

$$R_a = 1.79 \quad [M\Omega]$$

$$R_b = 8.21 \quad [M\Omega]$$

Table 12 Shows the Range of V0 depending on the above Requirements.

Table 12. The Range of V0

| | Electronic volume level | | | | |
|----|-------------------------|-------|-------|-------|-------|
| | 0 | | 32 | | 63 |
| V0 | 8.21 | | 10.00 | | 11.73 |

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 13 shows the relationship between V1 to V4 level and each duty ratio.

Table 13

| LCD bias | V1 | V2 | V3 | V4 | Remarks |
|----------|--------------|--------------|----------|----------|------------|
| 1/N | (N-1)/N x V0 | (N-1)/N x V0 | 2/N x V0 | 1/N x V0 | N = 4 to 9 |

REFERECE CIRCUIT EXAMPLES

[C1 = 1.0 to 4.7 [μF], C2 = 0.47 to 2.0 [μF]]

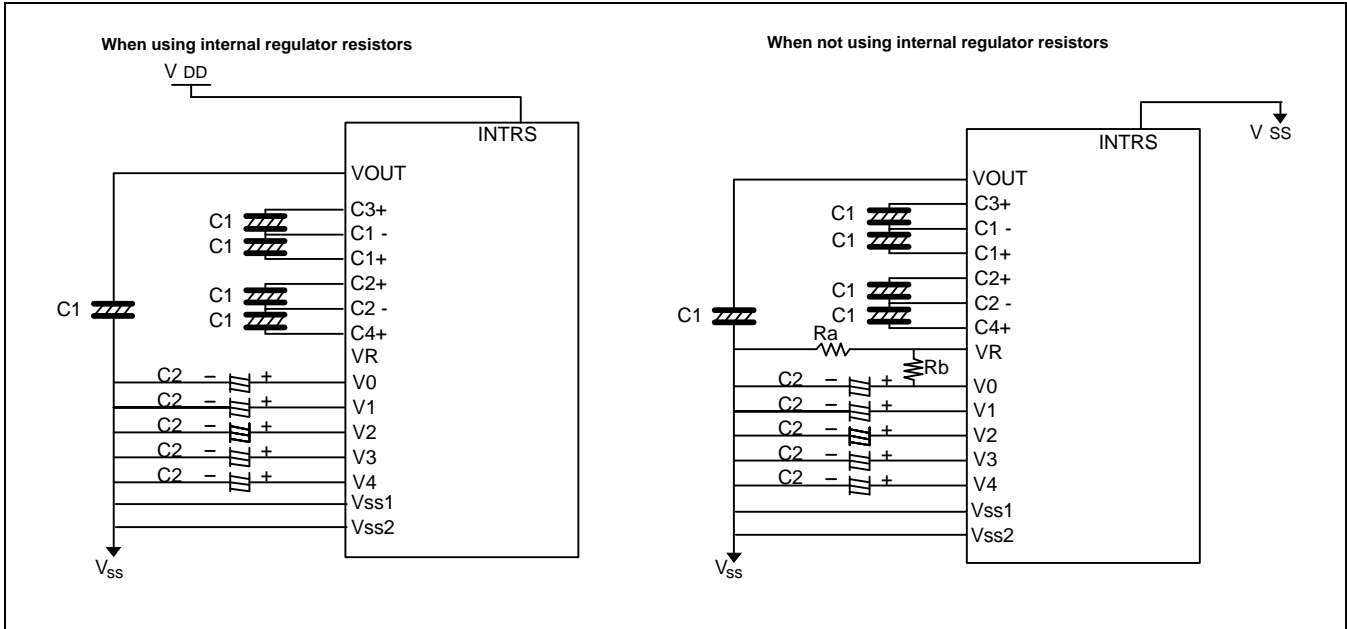


Figure 22. When Using all LCD Power Circuits (6-Time V/C: ON, V/R: ON, V/F: ON)

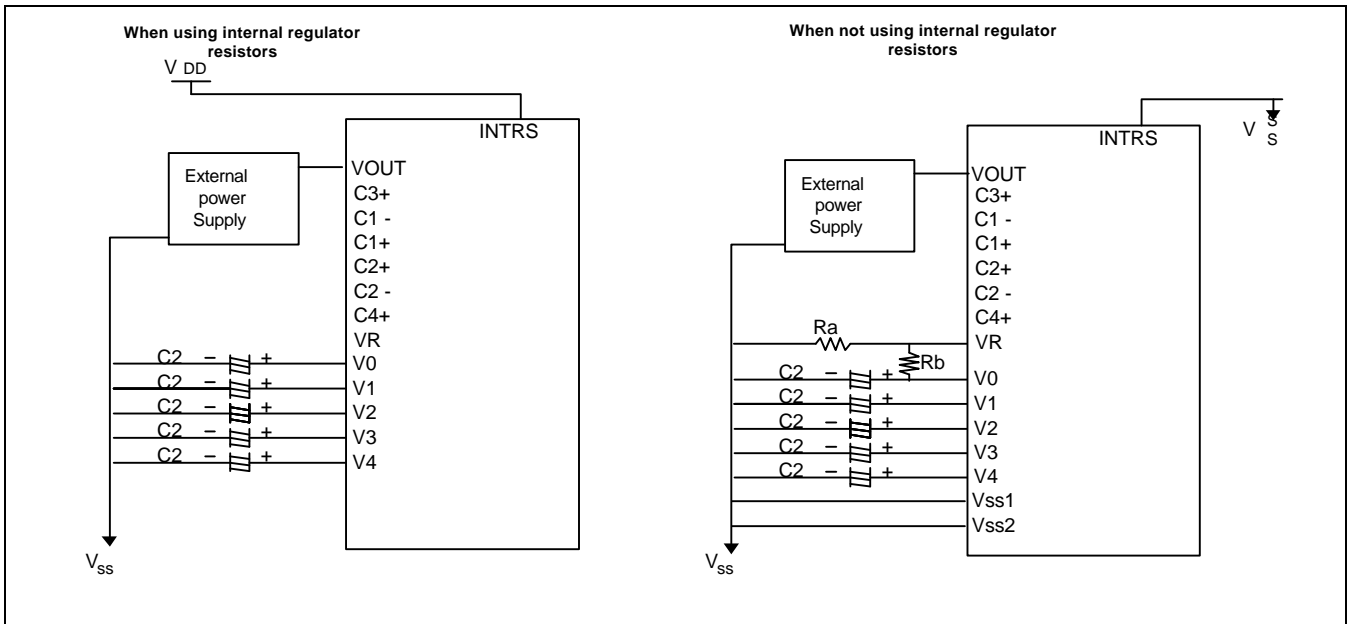


Figure 23. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

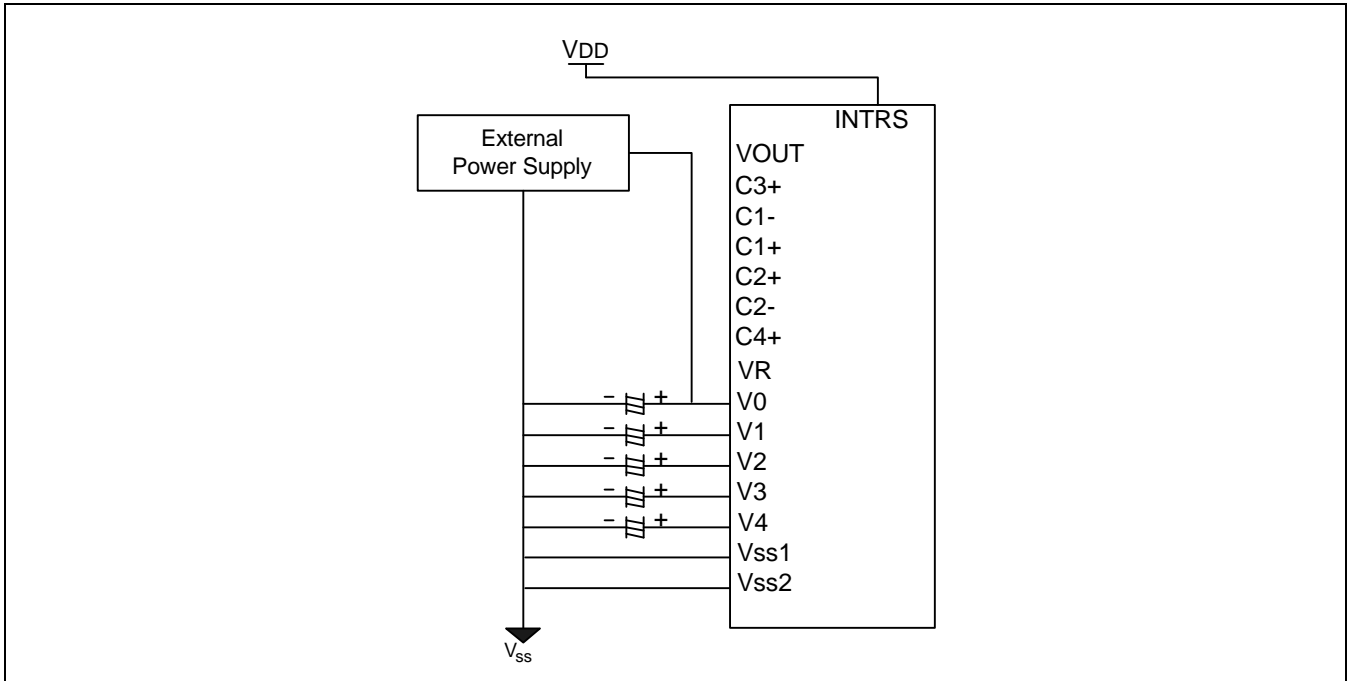


Figure 24. When Using only Voltage Follower Circuit (V/C: OFF, V/R: OFF, V/F: ON)

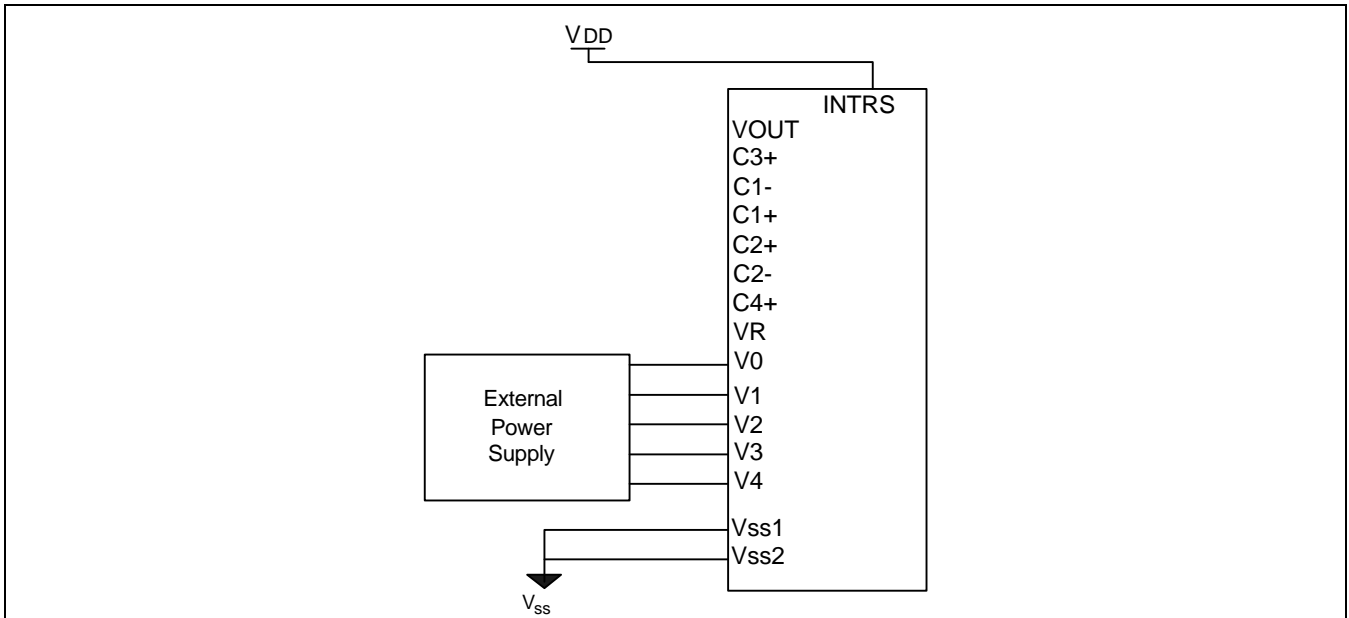


Figure 25. When Not Using all LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.
When RESETB becomes "L", following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: OFF
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Partial display duty ratio: 1/64
Icon enable/disable : 0 (disable)
Reverse display ON / OFF: OFF (normal)
n-line inversion register: 0 (disable)
Entire display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
DC-DC step up: 3 times converter circuit = (0, 0)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register: (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)
LCD bias ratio: 1/9
SHL select: OFF (normal)
ADC select: OFF (normal)
Oscillator status: OFF
Power save mode: release

When RESET instruction is issued, following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: OFF
Initial display line: 0 (First)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)
Other instruction registers : Not Changed

While RESETB is "L" or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 14. Instruction Table

×: Don't care

| Instruction | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Description |
|-----------------------------------|----|----|------------|-----|-----|-----|-----|-----|-----|-----|--|
| Read display data | 1 | 1 | Read data | | | | | | | | Read data from DDRAM |
| Write display data | 1 | 0 | Write data | | | | | | | | Write data into DDRAM |
| Read status | 0 | 1 | BUSY | ON | RES | 0 | 0 | 0 | 0 | 0 | Read the internal status |
| Set page address | 0 | 0 | 1 | 0 | 1 | 1 | P3 | P2 | P1 | P0 | Set page address |
| Set column address MSB | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Y6 | Y5 | Y4 | Set column address MSB |
| Set column address LSB | 0 | 0 | 0 | 0 | 0 | 0 | Y3 | Y2 | Y1 | Y0 | Set column address LSB |
| Set modify-read | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Set modify-read mode |
| Reset modify-read | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Release modify-read mode |
| Display ON / OFF | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D | D = 0: display OFF D = 1: display ON |
| Set initial display line register | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | × | × | 2-byte instruction to specify the initial display line to realize vertical scrolling |
| | 0 | 0 | × | S6 | S5 | S4 | S3 | S2 | S1 | S0 | |
| Set initial COM0 register | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | × | × | 2-byte instruction to specify the initial COM0 to realize window scrolling |
| | 0 | 0 | × | × | C5 | C4 | C3 | C2 | C1 | C0 | |
| Set partial display duty ratio | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | × | × | 2-byte instruction to set partial display duty ratio |
| | 0 | 0 | × | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Set n-line inversion | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | × | × | 2-byte instruction to set n-line inversion register |
| | 0 | 0 | × | × | × | N4 | N3 | N2 | N1 | N0 | |
| Release n-line inversion | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | Release n-line inversion mode |
| Reverse display ON / OFF | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | REV | REV = 0: normal display REV = 1: reverse display |
| Icon enable/disable | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | I | I = 0: Icon disable I = 1: Icon enable |
| Entire display ON / OFF | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | EON | EON = 0: normal display EON = 1: entire display ON |

Table 16. Instruction Table (Continued)

| Instruction | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Description |
|---|----|----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Power control | 0 | 0 | 0 | 0 | 1 | 0 | 1 | VC | VR | VF | Control power circuit operation |
| Select DC-DC step-up | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | DC1 | DC0 | Select the step-up of the internal voltage converter |
| Select regulator resistor | 0 | 0 | 0 | 0 | 1 | 0 | 0 | R2 | R1 | R0 | Select internal resistance ratio of the regulator resistor |
| Set electronic volume register | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2-byte instruction to specify the electronic volume register |
| | 0 | 0 | × | × | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 | |
| Select LCD bias | 0 | 0 | 0 | 1 | 0 | 1 | 0 | B2 | B1 | B0 | Select LCD bias |
| SHL select | 0 | 0 | 1 | 1 | 0 | 0 | SHL | × | × | × | COM bi-directional selection SHL = 0: normal direction SHL = 1: reverse direction |
| ADC select | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | ADC | SEG bi-directional selection ADC = 0: normal direction ADC = 1: reverse direction |
| Set Data Direction & Display Data Length(DDL) | × | × | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 2-byte Instruction to specify the number of data bytes(SPI Mode). |
| | × | × | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Oscillator ON start | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Start the built-in oscillator |
| Set power save mode | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | P | P = 0: standby mode P = 1: sleep mode |
| Release power save mode | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | Release power save mode |
| Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Initialize the internal functions |
| NOP | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | <u>No operation</u> |
| Test instruction | 0 | 0 | 1 | 1 | 1 | 1 | × | × | × | × | <u>Don't use this instruction.</u> |

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is incremented by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----------|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | Read data | | | | | | | |

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is incremented by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|------------|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | Write data | | | | | | | |

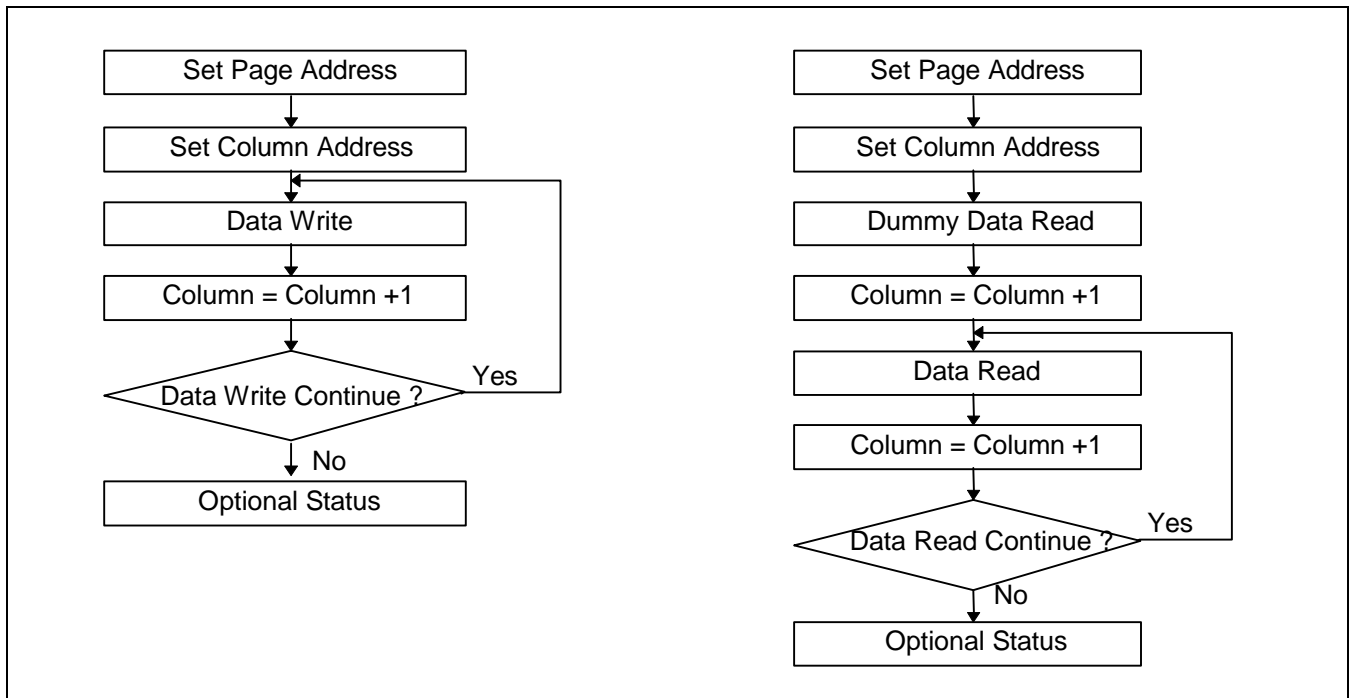


Figure 26. Sequence for Writing Display Data

Figure 27. Sequence for Reading Display Data

Read Status

Indicates the internal status of the S6B0755

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|------|-----|-----|-----|-----|-----|-----|-----|
| 0 | 1 | BUSY | ON | RES | 0 | 0 | 0 | 0 | 0 |

| Flag | Description |
|------|---|
| BUSY | The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy. |
| ON | Indicates display ON / OFF status. 0: display ON, 1: display OFF |
| RES | Indicates the initialization is in progress by RESETB signal. 0: chip is active, 1: chip is being reset. |

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 1 | P3 | P2 | P1 | P0 |

| P3 | P2 | P1 | P0 | Selected page | Description |
|----|----|----|----|---------------|---|
| 0 | 0 | 0 | 0 | 0 | Accessible pages for displaying dot-matrix display data |
| 0 | 0 | 0 | 1 | 1 | |
| 0 | 0 | 1 | 0 | 2 | |
| : | : | : | : | : | |
| 0 | 1 | 1 | 1 | 7 | Accessible page for displaying icons |
| 1 | 0 | 0 | 0 | 8 | |
| : | : | : | : | : | Not accessible page. Do not use these pages. |
| 1 | 1 | 0 | 0 | 12 | |
| 1 | 1 | 0 | 1 | 13 | |
| 1 | 1 | 1 | 0 | 14 | |
| 1 | 1 | 1 | 1 | 15 | |

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically incremented.

Set Column Address MSB

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | Y6 | Y5 | Y4 |

Set Column Address LSB

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | Y3 | Y2 | Y1 | Y0 |

| Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 | Selected column address |
|----|----|----|----|----|----|----|-------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 125 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 126 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the Write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

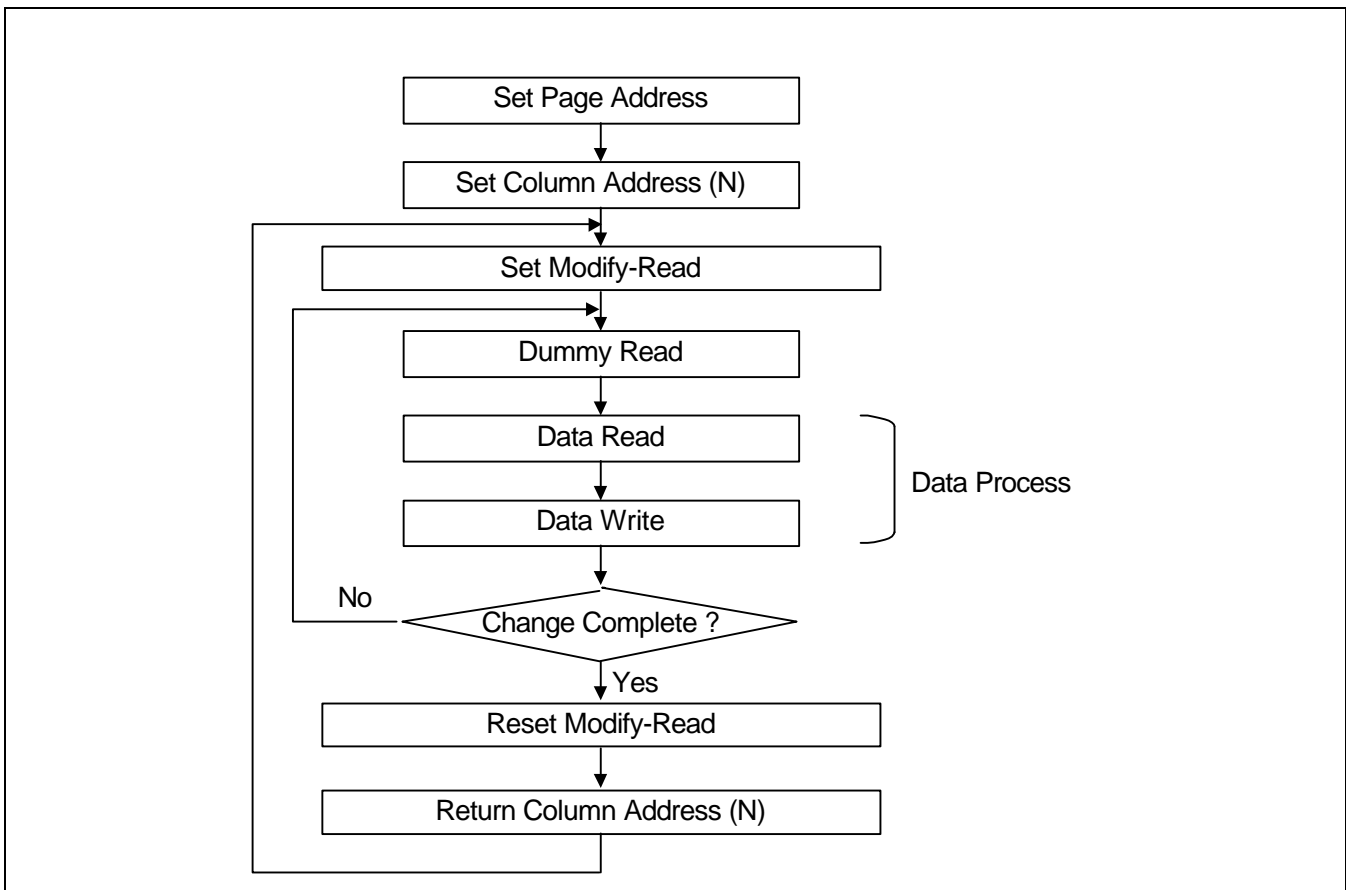


Figure 28. Sequence for Cursor Display

Display ON / OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D |

D = 1: display ON

D = 0: display OFF

Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top row (COM0) of LCD panel.

The 1st Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | × | × |

The 2nd Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | × | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

| S6 | S5 | S4 | S3 | S2 | S1 | S0 | Selected line address |
|----|----|----|----|----|----|----|-----------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 63 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | No operation |
| : | : | : | : | : | : | : | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

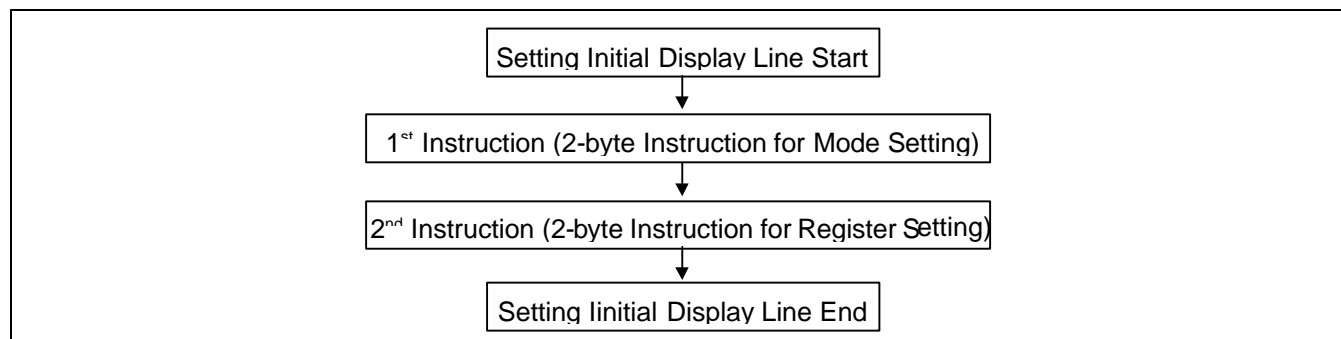


Figure 29. The Sequence for Setting the Initial Display Line

Set Initial COM0 Register

Sets the initial row (COM0) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | × | × |

The 2nd Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | × | × | C5 | C4 | C3 | C2 | C1 | C0 |

| C5 | C4 | C3 | C2 | C1 | C0 | Initial COM0 |
|----|----|----|----|----|----|--------------|
| 0 | 0 | 0 | 0 | 0 | 0 | COM0 |
| 0 | 0 | 0 | 0 | 0 | 1 | COM1 |
| 0 | 0 | 0 | 0 | 1 | 0 | COM2 |
| 0 | 0 | 0 | 0 | 1 | 1 | COM3 |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 0 | 0 | COM60 |
| 1 | 1 | 1 | 1 | 0 | 1 | COM61 |
| 1 | 1 | 1 | 1 | 1 | 0 | COM62 |
| 1 | 1 | 1 | 1 | 1 | 1 | COM63 |

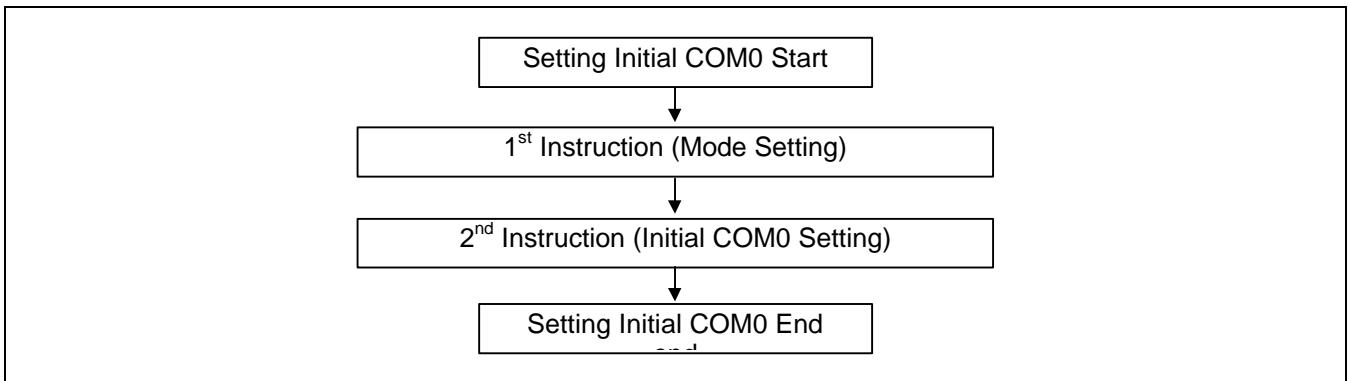


Figure 30. Sequence for Setting the Initial COM0

Set Partial Display Duty Ratio

When the icon mode is disable, Sets the duty ratio within range of 16 to 64 to realize partial display by using the 2-byte instruction. When the icon mode is enable, Sets the duty ratio within range of 17 to 65 to realize partial display by using the 2-byte instruction. This table is icon disable case.

The 1st Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | × | × |

The 2nd Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | × | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Icon Enable/Disable Bit = 0

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | Selected partial duty ratio |
|----|----|----|----|----|----|----|-----------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | No operation |
| : | : | : | : | : | : | : | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1/16 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1/17 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1/18 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1/19 |
| : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1/61 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1/62 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1/63 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1/64 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | No operation |
| : | : | : | : | : | : | : | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

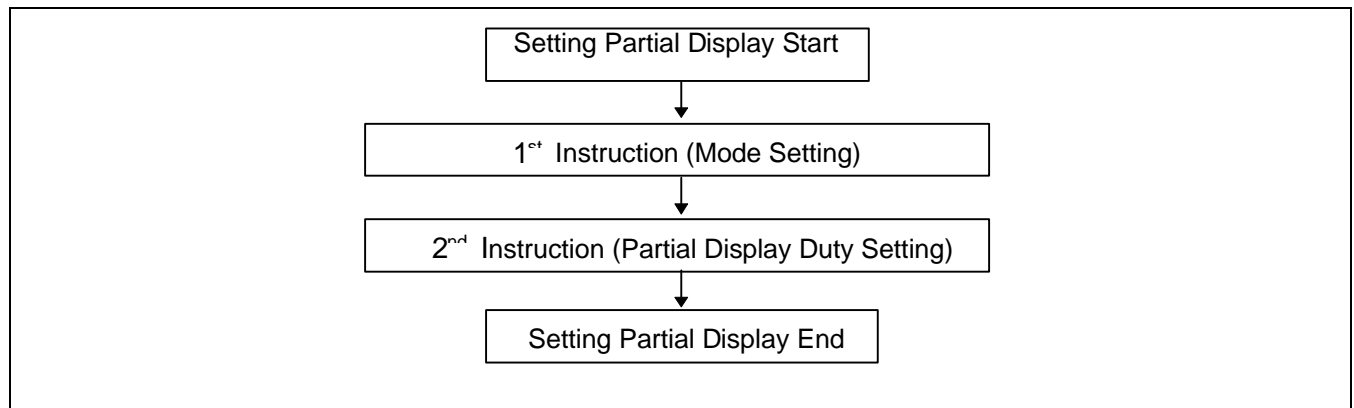


Figure 31. Sequence for Setting Partial Display

Icon Enable/Disable Bit = 1

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | Selected partial duty ratio |
|----|----|----|----|----|----|----|-----------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | No operation |
| : | : | : | : | : | : | : | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1/17 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1/18 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1/19 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1/20 |
| : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1/62 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1/63 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1/64 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1/65 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | No operation |
| : | : | : | : | : | : | : | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

Set N-line Inversion Register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (Internal M) by using the 2-byte instruction.

The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K : D/N

D : The number of display duty ratio (D is selectable by customers)

N : N for N-line inversion (N is selectable by customers).

The 1st Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | × | × |

The 2nd Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | × | × | × | N4 | N3 | N2 | N1 | N0 |

| N4 | N3 | N2 | N1 | N0 | Selected n-line inversion |
|----|----|----|----|----|------------------------------------|
| 0 | 0 | 0 | 0 | 0 | 0-line inversion (frame inversion) |
| 0 | 0 | 0 | 0 | 1 | 3-line inversion |
| 0 | 0 | 0 | 1 | 0 | 4-line inversion |
| : | : | : | : | : | : |
| 1 | 1 | 1 | 0 | 1 | 31-line inversion |
| 1 | 1 | 1 | 1 | 0 | 32-line inversion |
| 1 | 1 | 1 | 1 | 1 | 33-line inversion |

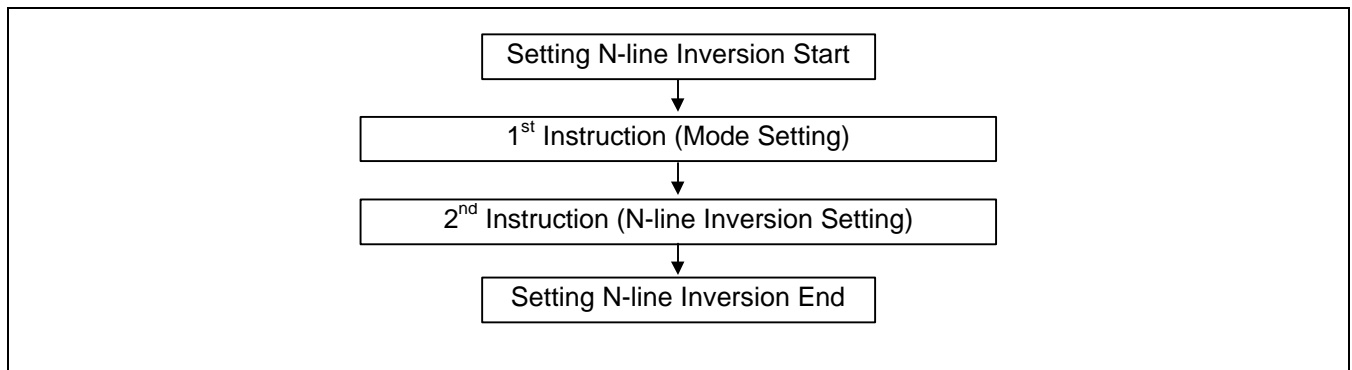


Figure 32. Sequence for Setting Partial Display

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | REV |

| REV | RAM bit data = "1" | RAM bit data = "0" |
|-------------|------------------------------|------------------------------|
| 0 (normal) | LCD pixel is illuminated | LCD pixel is not illuminated |
| 1 (reverse) | LCD pixel is not illuminated | LCD pixel is illuminated |

Icon enable / Disable

Allows the icon driver circuit to be enabled or disabled, thus changing the duty ratio setting.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | I |

| I | Duty Range |
|-------------|-------------|
| 0 (disable) | 1/16 ~ 1/64 |
| 1 (enable) | 1/17 ~ 1/65 |

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | EON |

| EON | RAM bit data = "1" | RAM bit data = "0" |
|------------|--------------------------|------------------------------|
| 0 (normal) | LCD pixel is illuminated | LCD pixel is not illuminated |
| 1 (entire) | LCD pixel is illuminated | LCD pixel is illuminated |

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | VC | VR | VF |

| VC | VR | VF | Status of internal power supply circuits |
|----|----|----|---|
| 0 | | | Internal voltage converter circuit is OFF |
| 1 | | | Internal voltage converter circuit is ON |
| | 0 | | Internal voltage regulator circuit is OFF |
| | 1 | | Internal voltage regulator circuit is ON |
| | | 0 | Internal voltage follower circuit is OFF |
| | | 1 | Internal voltage follower circuit is ON |

Select DC-DC Step-up

Selects one of 3 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | DC1 | DC0 |

| DC1 | DC0 | Selected DC-DC converter circuit |
|-----|-----|----------------------------------|
| 0 | 0 | 3 times boosting circuit |
| 0 | 1 | 4 times boosting circuit |
| 1 | 0 | 5 times boosting circuit |
| 1 | 1 | 5 times boosting circuit |

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to Table 12.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | R2 | R1 | R0 |

| R2 | R1 | R0 | [Rb / Ra] ratio |
|----|----|----|-----------------|
| 0 | 0 | 0 | Small |
| 0 | 0 | 1 | : |
| : | : | : | : |
| 1 | 1 | 0 | : |
| 1 | 1 | 1 | Large |

Set Electronic Volume Register

Consists of 2-byte instruction

The 1st instruction sets electronic volume mode, the 2nd one updates the contents of electronic volume register. After second instruction, electronic volume mode is released.

The 1st Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

The 2nd Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | × | × | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |

| EV5 | EV4 | EV3 | EV2 | EV1 | EV0 | Reference voltage (α) |
|-----|-----|-----|-----|-----|-----|--------------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : | : | : |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

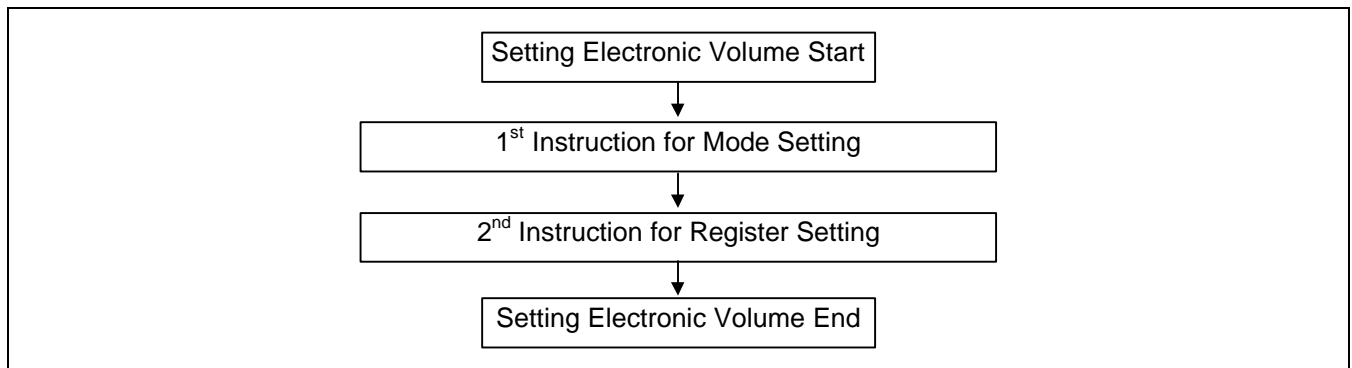


Figure 33. Sequence for Setting the Electronic Volume

Select LCD Bias

Selects LCD Bias ratio of the voltage required for driving the LCD.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | B2 | B1 | B0 |

| B2 | B1 | B0 | Selected LCD bias |
|----|----|----|-------------------|
| 0 | 0 | 0 | 1/4 |
| 0 | 0 | 1 | 1/5 |
| 0 | 1 | 0 | 1/6 |
| 0 | 1 | 1 | 1/7 |
| 1 | 0 | 0 | 1/8 |
| 1 | 0 | 1 | 1/9 |
| 1 | 1 | 0 | 1/9 |
| 1 | 1 | 1 | 1/9 |

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 0 | 0 | SHL | × | × | × |

SHL = 0: normal direction (COM0 → COM63)

SHL = 1: reverse direction (COM63 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | ADC |

ADC = 0: normal direction (SEG0 → SEG127)

ADC = 1: reverse direction (SEG127 → SEG0)

Set Data Direction & Display Data Length (3-Pin SPI Mode)

Consists of two bytes instruction.

This command is used in 3-Pin SPI mode only(PS0 = "L" and PS1 = "L"). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When RS is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| x | x | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

The 2nd Instruction: Set Display Data Length (DDL) Register

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| x | x | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Display Data Length |
|----|----|----|----|----|----|----|----|---------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3 |
| : | : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 254 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 255 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 256 |

Oscillator ON Start

This instruction enables the built-in oscillator circuit.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

Power Save

The S6B0755 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | P |

P = 0: standby mode

P = 1: sleep mode

Release Power Save Mode

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

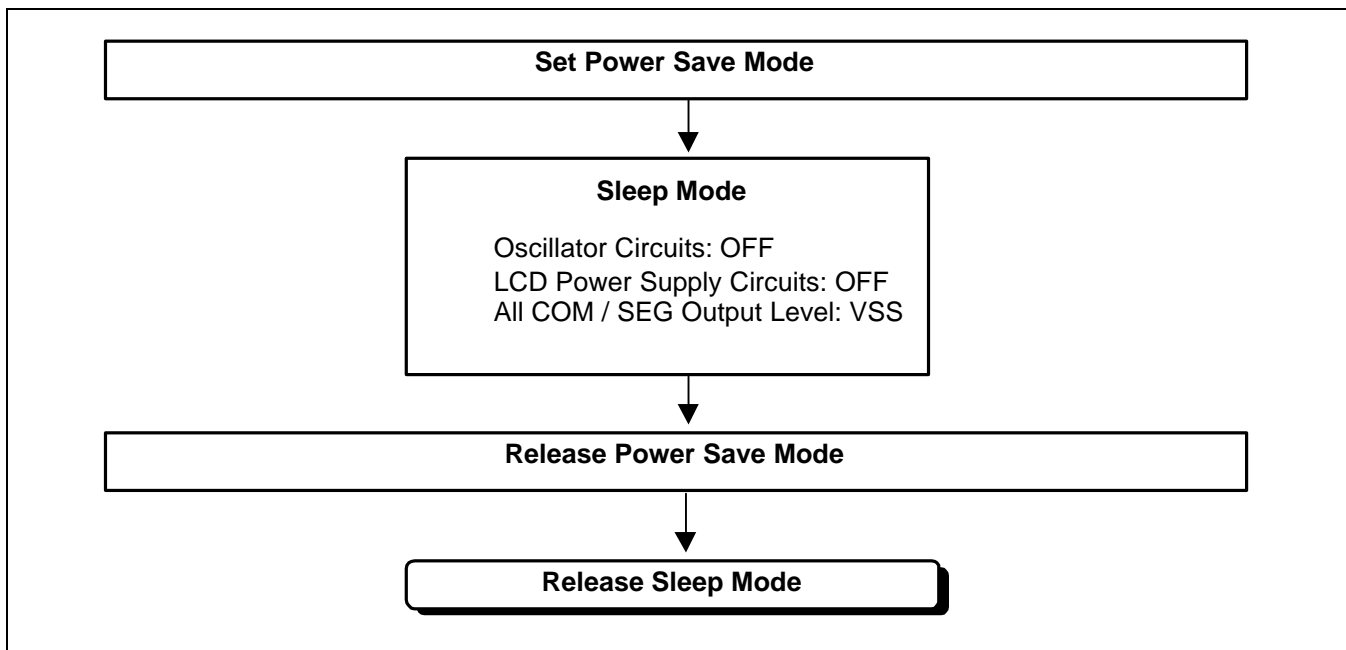


Figure 34. Power Save Routine

NOP

Non Operation Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

Test Instruction

This instruction is for testing IC. Please do not use it.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 1 | × | × | × | × |

Referential Instruction Setup Flow: Initializing with the Built-in Power Supply Circuits

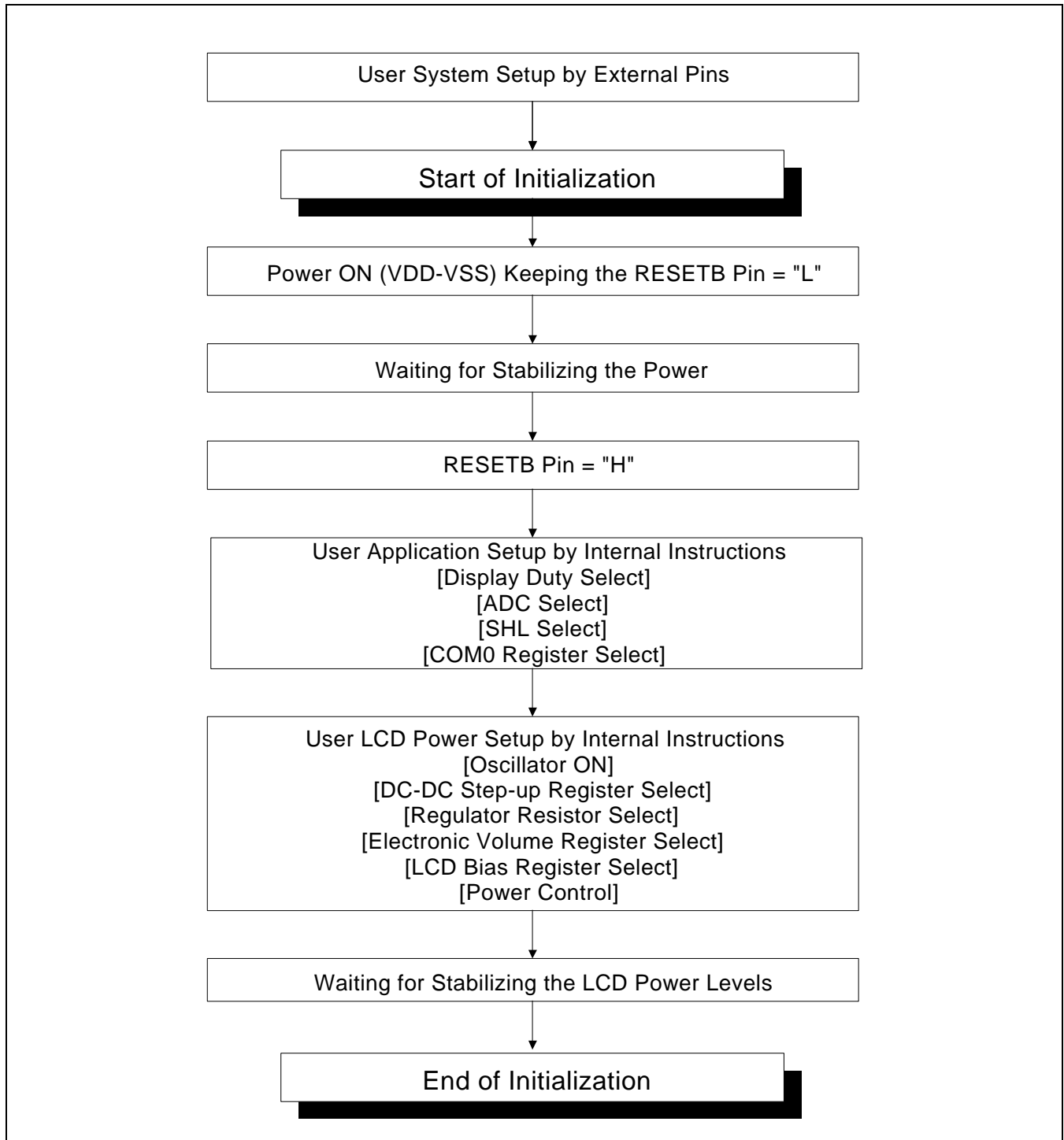


Figure 35. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the Built-in Power Supply Circuits

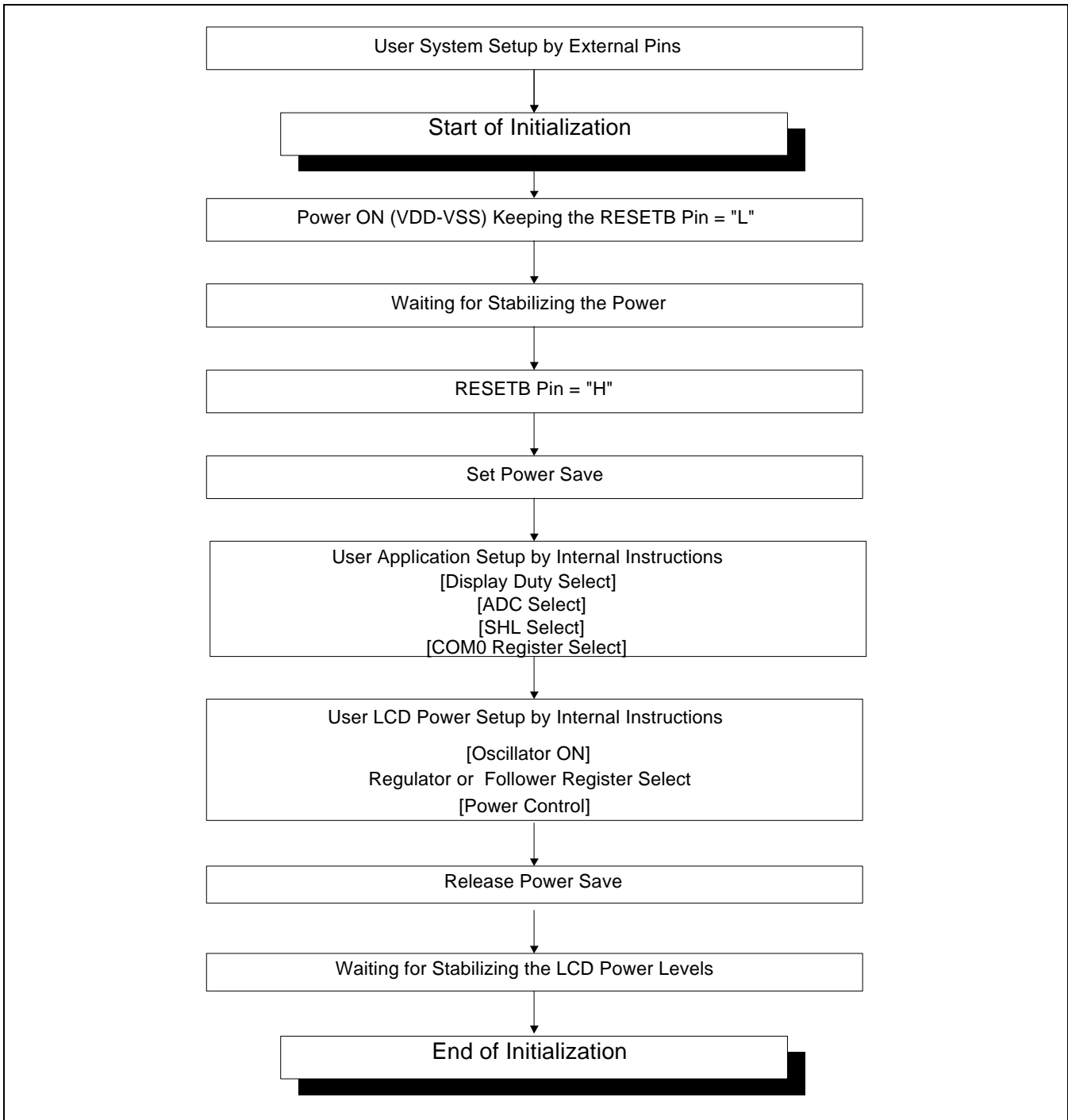
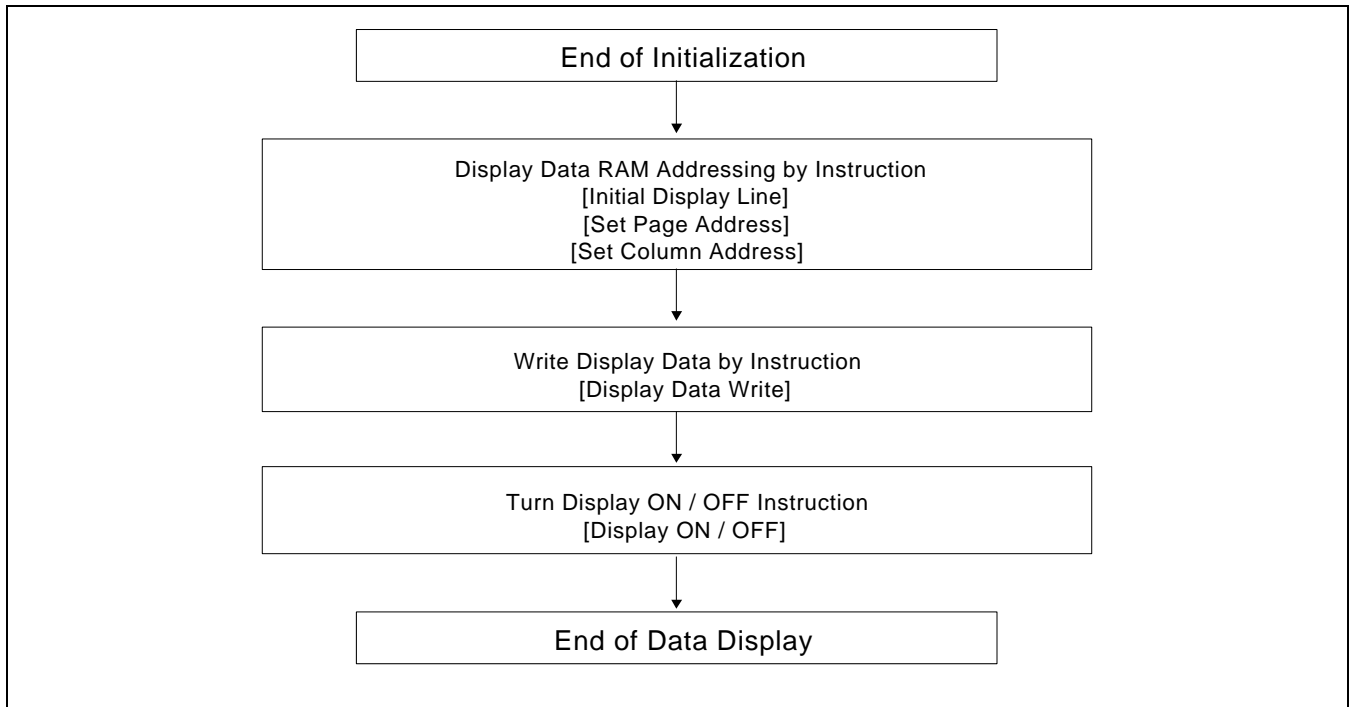
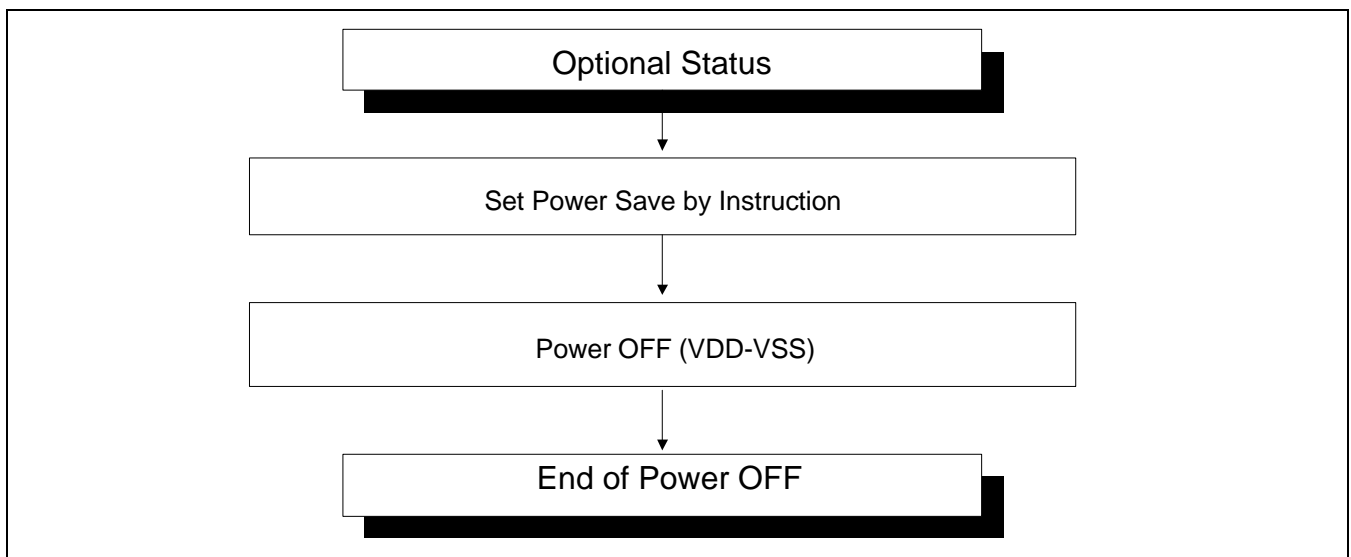


Figure 36. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying**Figure 37. Data Displaying****Referential Instruction Setup Flow: Power OFF****Figure 38. Power OFF**

Referential Instruction Setup Flow: Partial Duty Changing

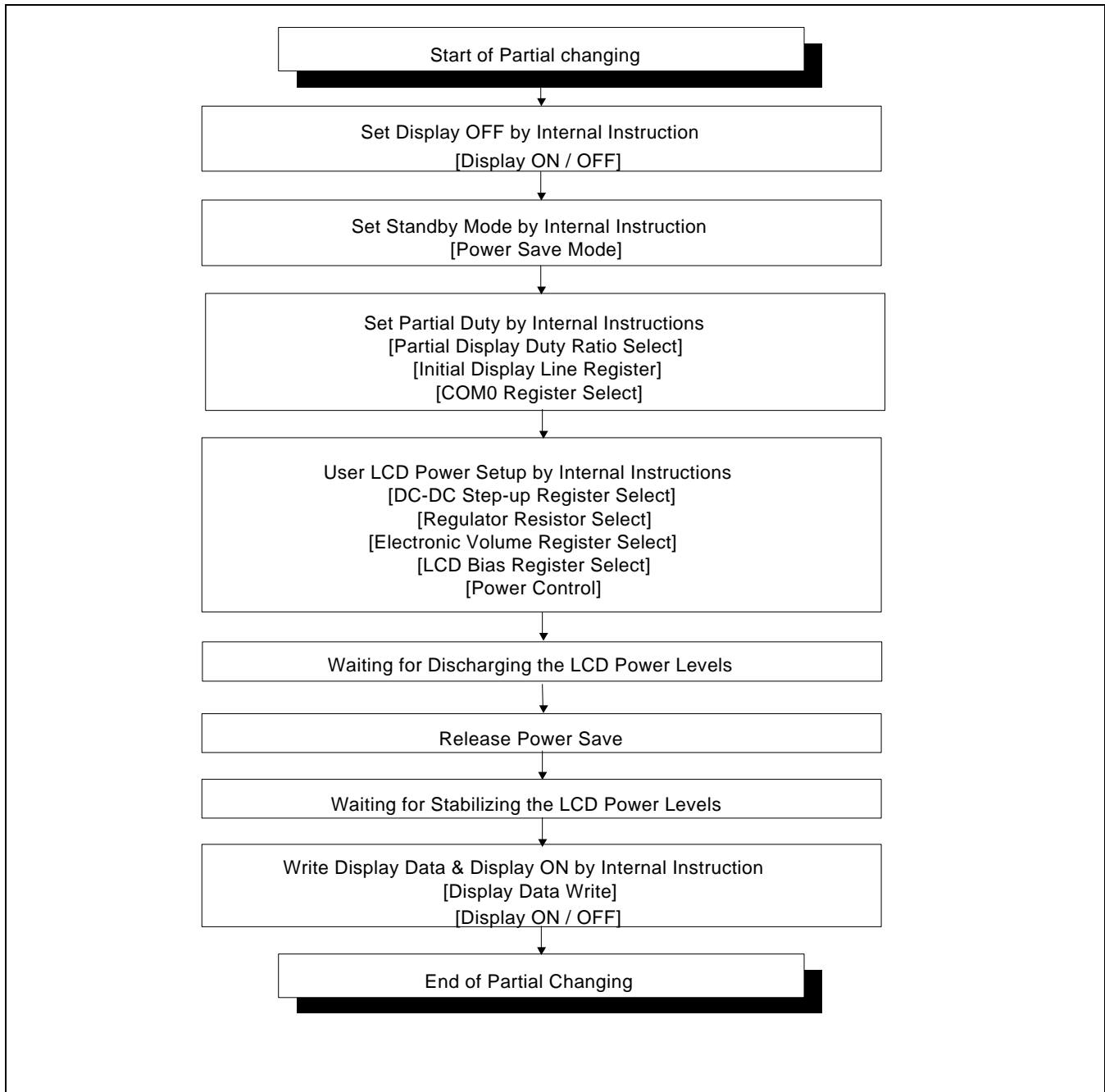


Figure 39. Partial Duty Changing

NOTE:1. Partial COM0 register setting for COM H/W half: $[64 - (\text{user duty})] / 2$

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 15. Absolute Maximum Ratings

(V_{SS} = 0V)

| Parameter | Symbol | Rating | Unit |
|-----------------------------|---|-------------------------------|------|
| Supply voltage range | V _{DD} | - 0.3 ~ + 7.0 | V |
| | V ₀ , V _{OUT} | - 0.3 ~ + 17.0 | V |
| | V ₁ , V ₂ , V ₃ , V ₄ | - 0.3 ~ V ₀ + 0.3 | V |
| External reference voltage | V _{EXT} | +0.3 ~ V _{DD} | V |
| Input voltage range | V _{IN} | - 0.3 ~ V _{DD} + 0.3 | V |
| Operating temperature range | T _{OPR} | - 40 ~ + 85 | °C |
| Storage temperature range | T _{STR} | - 65 ~ + 150 | °C |

NOTES:

1. V_{DD}, V₀, V_{OUT}, V₁ to V₄, V_{EXT} and V_{CI} are based on V_{SS} = 0V.
2. Voltage V_{OUT} ≥ V₀ ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V_{SS} must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 16. DC Characteristics

(V_{SS} = 0V, V_{DD} = 1.8~3.3V, T_a = -40~85°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin used |
|--------------------------|-----------------|--|--------------------------|--------------------|--------------------|--------------------|-----------------|
| Operating voltage (1) | V _{DD} | | 1.8 | - | 3.3 | V | VDD *1 |
| Operating voltage (2) | V ₀ | | 4.0 | - | 15.0 | V | V0, *2 |
| Input voltage | High | V _{IH} | 0.8V _{DD} | - | V _{DD} | V | *3 |
| | Low | V _{IL} | V _{SS} | - | 0.2V _{DD} | | |
| Output voltage | High | V _{OH} | I _{OH} = -0.5mA | 0.8V _{DD} | - | V _{DD} | *4 |
| | Low | V _{OL} | I _{OL} = 0.5mA | V _{SS} | - | 0.2V _{DD} | |
| Input leakage current | I _{IL} | V _{IN} = V _{DD} or V _{SS} | - 1.0 | - | + 1.0 | μA | *3 |
| Output leakage current | I _{OZ} | V _{IN} = V _{DD} or V _{SS} | - 3.0 | - | + 3.0 | μA | *5 |
| LCD driver ON resistance | R _{ON} | T _a = 25°C, V ₀ = 8V | - | 2.0 | 3.0 | kΩ | SEGN COMn *6 |
| Frame frequency | f _{FR} | T _a = 25°C | 70 | 85 | 100 | Hz | *7 |

Table 17. DC Characteristics

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin used |
|---|------------------|--|------|------|------|------|----------|
| Voltage converter circuit output voltage | V _{OUT} | ×3 / ×4 / ×5 voltage conversion (no-load) | 95 | 99 | - | % | VOUT |
| Voltage regulator circuit operating voltage | V _{OUT} | | 5.4 | - | 15.0 | V | VOUT |
| Voltage follower circuit operating voltage | V ₀ | | 4.0 | - | 15.0 | V | V0 *8 |
| Reference voltage | V _{REF} | T _a = 25°C | 2.04 | 2.10 | 2.16 | V | *9 |

Dynamic Current Consumption (1) when An External Power Supply is used.**Table 18. Dynamic Current 1 (External Power)** $(V_{DD} = 2.4V, T_a = 25^{\circ}C)$

| Item | Symbol | Condition | Min | Typ | Max | Unit | Pin used |
|---------------------------------|-----------|---|-----|-----|-----|---------|----------|
| Dynamic current consumption (1) | I_{DD1} | $V_0 - V_{SS} = 9.0V$, duty = 1/65 (Display Off) | - | - | 10 | μA | *10 |
| | | $V_0 - V_{SS} = 9.0V$, duty = 1/65 (Display On , Checker Pattern) | - | - | 15 | μA | *10 |

Dynamic Current Consumption (2) when The Internal Power Supply is ON**Table 19. . Dynamic Current 2 (Internal Power)** $(V_{DD} = 2.4V, T_a = 25^{\circ}C)$

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin used |
|---------------------------------|-----------|--|------|------|------|---------|----------|
| Dynamic current consumption (2) | I_{DD2} | $V_0 - V_{SS} = 9.0V$, x4 boosting, duty = 1/65, normal mode (Display Off) | - | - | 190 | μA | *10 |
| | | $V_0 - V_{SS} = 9.0V$, x4 boosting, duty = 1/65, normal mode (Display On , Checker Pattern) | - | - | 300 | μA | *10 |

Current Consumption during Power Save Mode**Table 20. Power Save Mode Current** $(V_{DD} = 2.4V, T_a = 25^{\circ}C)$

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin used |
|--------------------|------------|--------------|------|------|------|---------|----------|
| Sleep mode current | I_{DDs1} | During sleep | - | - | 3 | μA | *10 |

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

| Duty ratio | Item | FCL | F _{osc} |
|------------|------------------------------------|-------------------|----------------------------|
| 1/N | On-chip oscillator circuit is used | $F_{FR} \times N$ | $f_{FR} \times 4 \times N$ |

(f_{osc}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: frame frequency, N = 17 to 65)

[* Remark Solves]

- *1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
- *2. In case of external power supply is applied.
- *3. CS1B, RS, DB0 to DB7, E_RD, RW_WR, RESETB, PS1, PS0, INTR, and REF
- *4. DB0 to DB7
- *5. Applies when the DB0 to DB7 pins are in high impedance.
- *6. Resistance value when -0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON [kΩ] = ΔV[V] / 0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
- *7. See Table 21 for the relationship between oscillation frequency and frame frequency.
- *8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
- *9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
- *10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors(Rb and Ra) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MP)

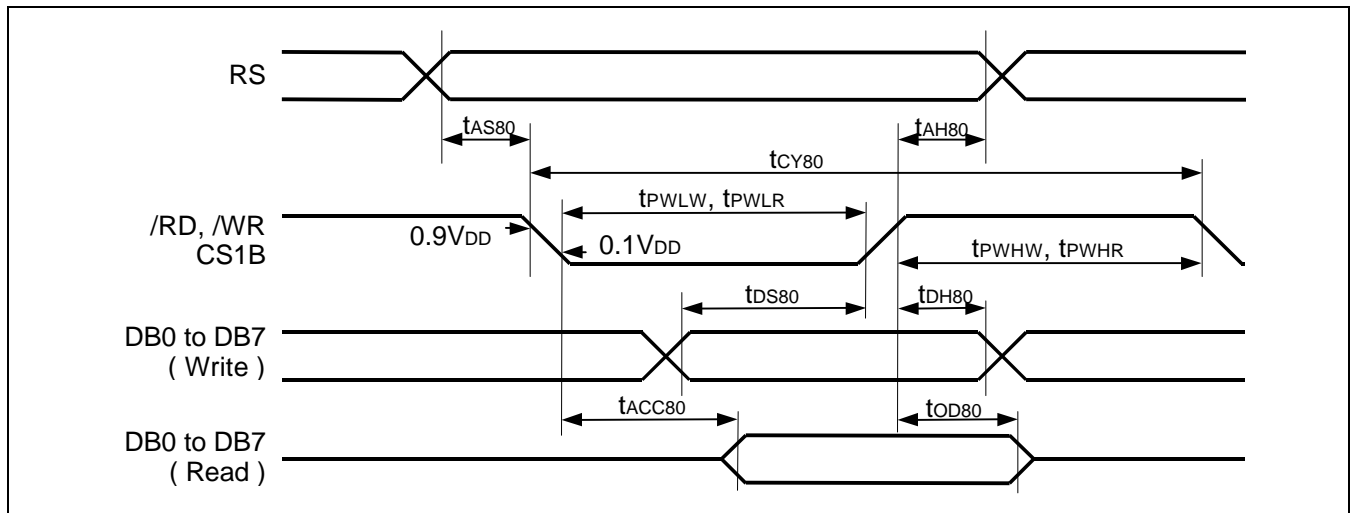


Figure 40. Read / Write Characteristics (8080-series MPU)

Table 22

($V_{DD} = 1.8 \sim 3.3V$, $T_a = -40 \sim +85^{\circ}C$)

| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|----------------------------|------------------|-------------|-------------|------|------|------|
| Address setup time | RS | t_{AS80} | | 0 | - | ns |
| Address hold time | | t_{AH80} | | 0 | - | ns |
| System cycle time | | t_{CY80} | | 500 | - | ns |
| Pulse width low for write | RW_WR (/WR) | t_{PWLW} | | 120 | - | ns |
| Pulse width high for write | | t_{PWHW} | | 120 | - | ns |
| Pulse width low for read | E_RD (/RD) | t_{PWLR} | | 240 | - | ns |
| Pulse width high for read | | t_{PWHR} | | 120 | - | ns |
| Data setup time | DB0 to DB7 | t_{DS80} | | 80 | - | ns |
| Data hold time | | t_{DH80} | | 30 | - | ns |
| Read access time | DB0 to DB7 | t_{ACC80} | CL = 100 pF | - | 280 | ns |
| Output disable time | | t_{OD80} | | 10 | 200 | |

NOTE: *1. The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less.

($t_r + t_f$) < ($t_{CY80} - t_{PWLW} - t_{PWHW}$) for write, ($t_r + t_f$) < ($t_{CY80} - t_{PWLR} - t_{PWHR}$) for read

Read / Write Characteristics (6800-series Microprocessor)

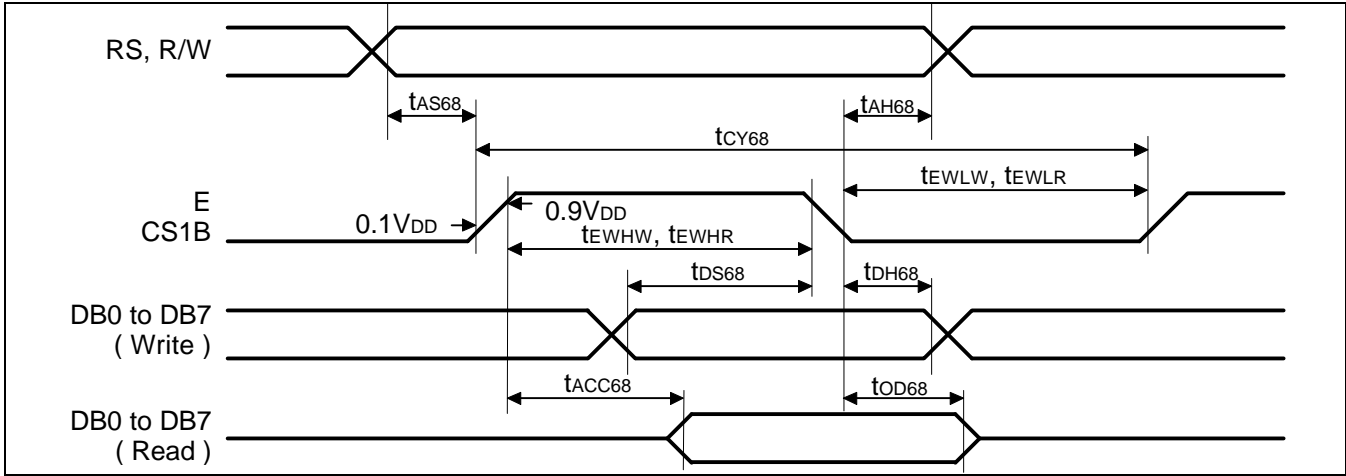


Figure 41. Read / Write Characteristics (6800-series Microprocessor)

Table 23

(V_{DD} = 1.8 ~ 3.3V, T_a = -40 ~ +85°C)

| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|-----------------------------|------------|--------------------|-------------------------|------|------|------|
| Address setup time | RS | t _{AS68} | | 0 | - | ns |
| Address hold time | RW | t _{AH68} | | 0 | - | ns |
| System cycle time | | t _{CY68} | | 500 | - | ns |
| Enable width high for write | E_RD | t _{EHLW} | | 120 | - | ns |
| Enable width low for write | (E) | t _{EHLR} | | 120 | - | ns |
| Enable width high for read | E_RD | t _{EHLH} | | 240 | - | ns |
| Enable width low for read | (E) | t _{EHLR} | | 120 | - | ns |
| Data setup time | DB0 to DB7 | t _{DS68} | | 30 | - | ns |
| Data hold time | | t _{DH68} | | 5 | - | ns |
| Read access time | DB0 to DB7 | t _{ACC68} | C _L = 100 pF | - | 60 | ns |
| Output disable time | | t _{OD68} | | 10 | 50 | ns |

NOTE: *1. The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less.
 (t_r + t_f) < (t_{CY68} - t_{EHLW} - t_{EHLR}) for write, (t_r + t_f) < (t_{CY68} - t_{EHLH} - t_{EHLR}) for read

Serial Interface Characteristics

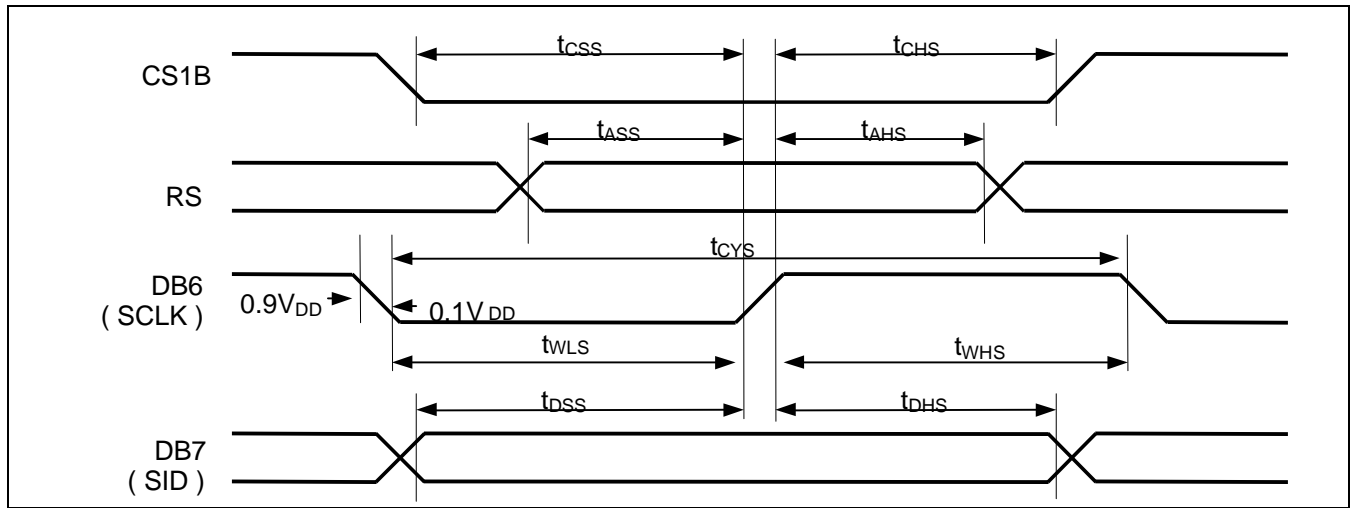


Figure 42

Table 24

(V_{DD} = 1.8 ~ 2.6V, T_a = -40 ~ +85°C)

| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|-----------------------|---------------|------------------|-----------|------|------|------|
| Serial clock cycle | DB6 (SCLK) | t _{SCY} | | 111 | - | ns |
| SCLK high pulse width | | t _{SHW} | | 60 | - | |
| SCLK low pulse width | | t _{SLW} | | 60 | - | |
| Address setup time | RS | t _{ASS} | | 60 | - | ns |
| Address hold time | | t _{AHS} | | 60 | - | |
| Data setup time | DB7 (SID) | T _{DSS} | | 60 | - | ns |
| Data hold time | | t _{DHS} | | 60 | - | |
| CS1B setup time | CS1B | T _{CSS} | | 60 | - | ns |
| CS1B hold time | | t _{CHS} | | 60 | - | |

(V_{DD} = 2.6V~ 3.3V, T_a = -40 ~ +85°C)

| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|-----------------------|---------------|------------------|-----------|------|------|------|
| Serial clock cycle | DB6 (SCLK) | t _{SCY} | | 58.8 | - | ns |
| SCLK high pulse width | | t _{SHW} | | 30 | - | |
| SCLK low pulse width | | t _{SLW} | | 30 | - | |
| Address setup time | RS | t _{ASS} | | 30 | - | ns |
| Address hold time | | t _{AHS} | | 30 | - | |
| Data setup time | DB7 (SID) | T _{DSS} | | 30 | - | ns |
| Data hold time | | t _{DHS} | | 30 | - | |
| CS1B setup time | CS1B | T _{CSS} | | 30 | - | ns |
| CS1B hold time | | t _{CHS} | | 30 | - | |

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Reset Input Timing

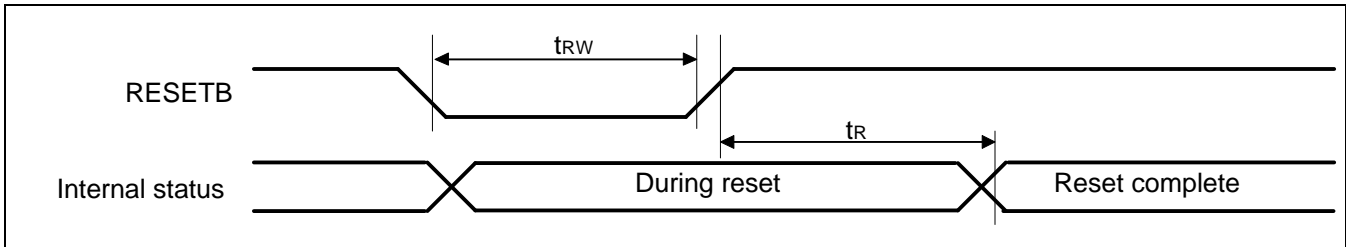


Figure 43

Table 25

(V_{DD} = 1.8 ~ 3.3V, T_a = -40 ~ +85°C)

| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|-----------------------|--------|-----------------|-----------|------|------|------|
| Reset low pulse width | RESETB | t _{rw} | | 1000 | - | ns |
| Reset time | - | t _r | | - | 1000 | ns |

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS0 = "H", PS1 = "H")

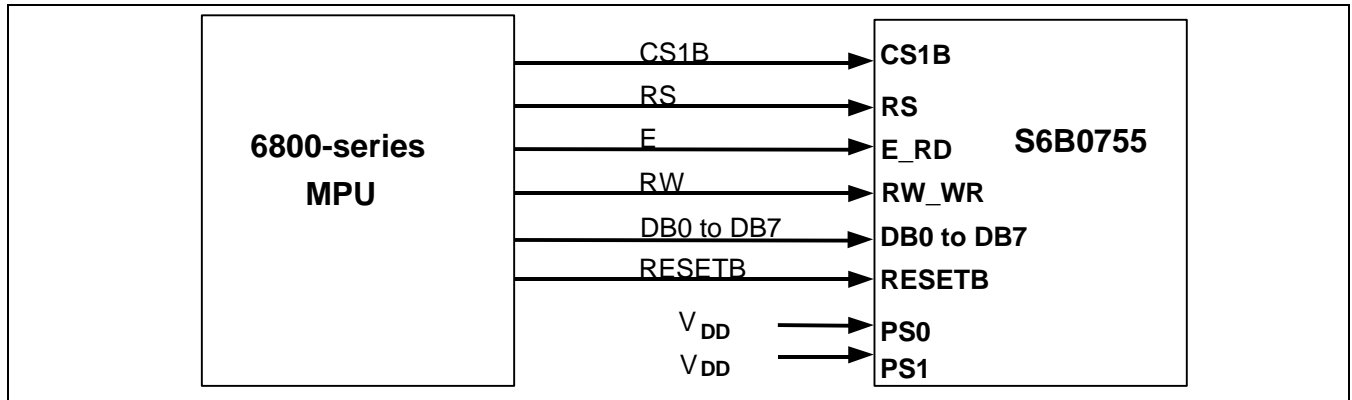


Figure 44. Interfacing with 6800-series

In Case of Interfacing with 8080-series (PS0 = "H" , PS1 = "L")

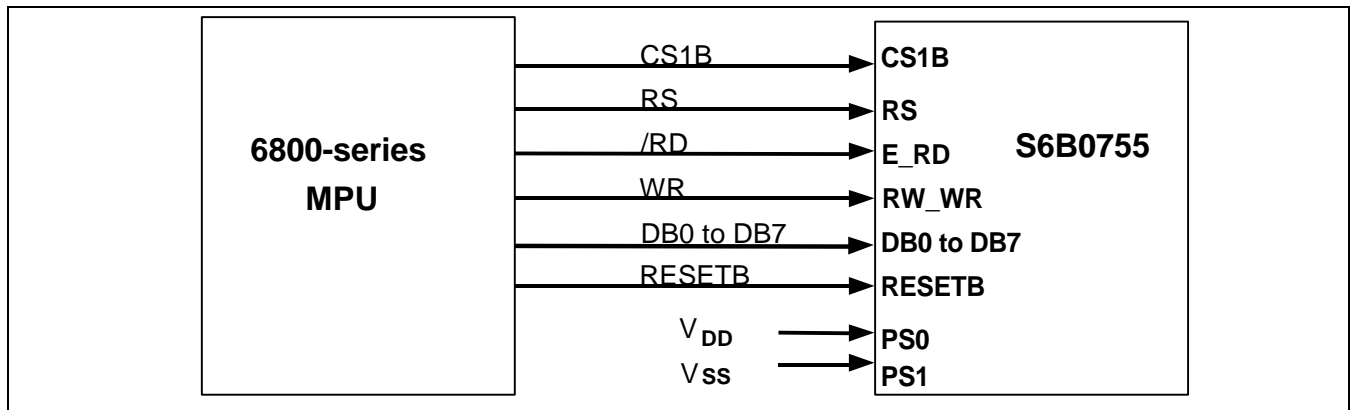


Figure 45. Interfacing with 8080-series

In Case of Serial Peripheral Interface with RS Pin (PS0 = "L" , PS1 = "H")

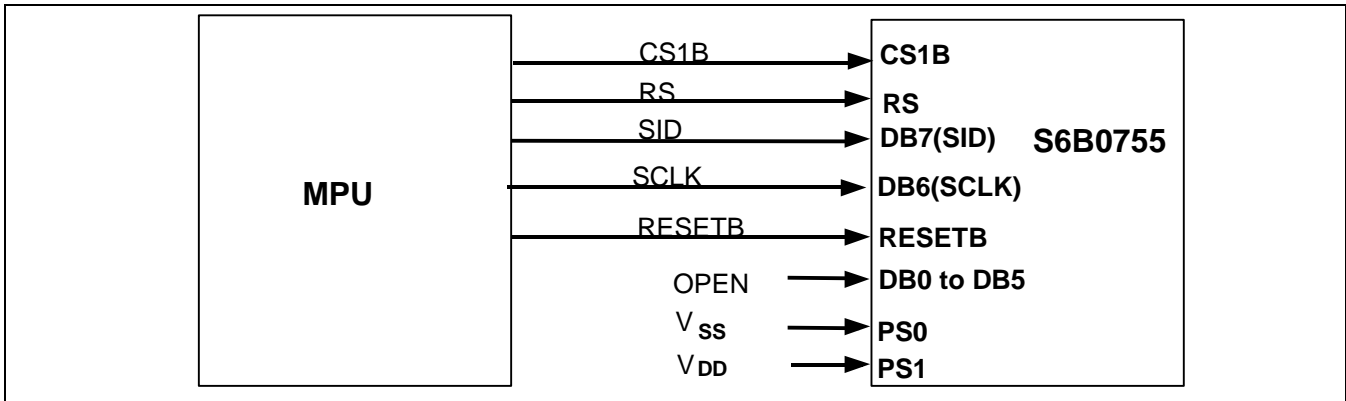


Figure 46. Serial Interface

In Case of Serial Peripheral Interface with software command (PS0 = "L" , PS1 = "L")

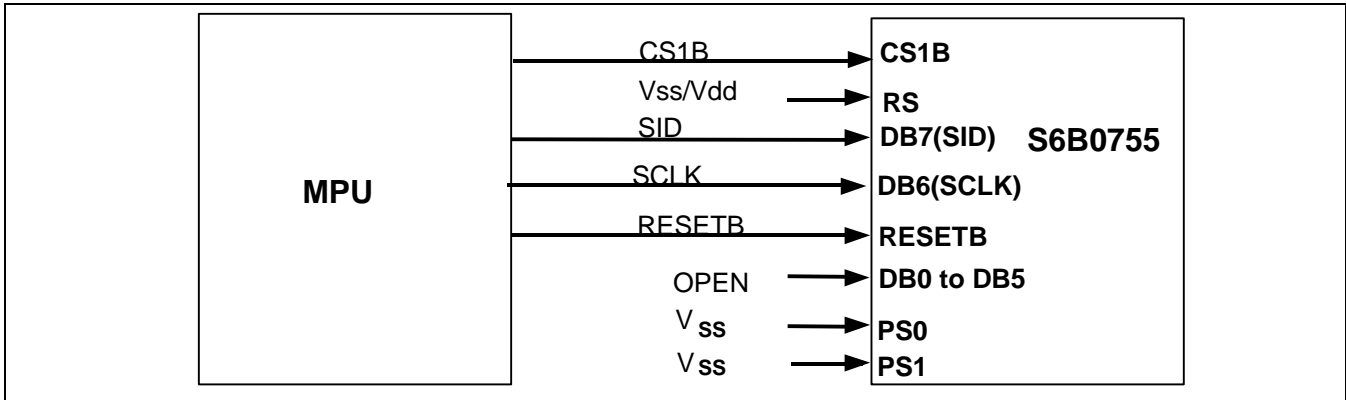


Figure 47. Serial Interface

CONNECTIONS BETWEEN S6B0755 AND LCD PANEL

Single Chip Configurations (1/65 Duty)

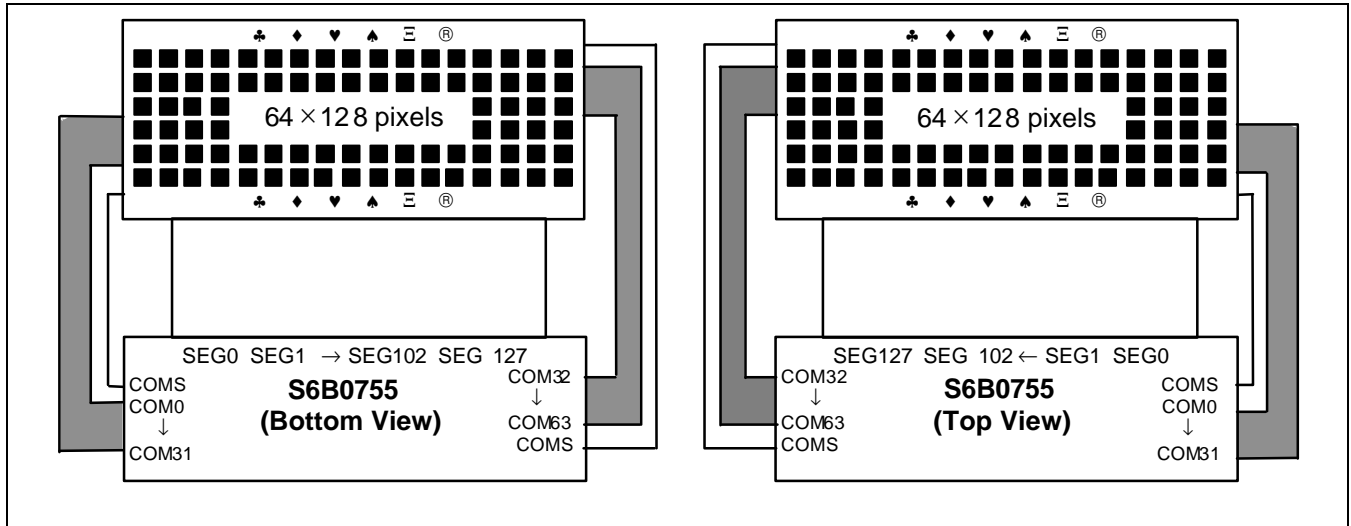


Figure 48. SHL = 0, ADC = 1

Figure 49. SHL = 0, ADC = 0

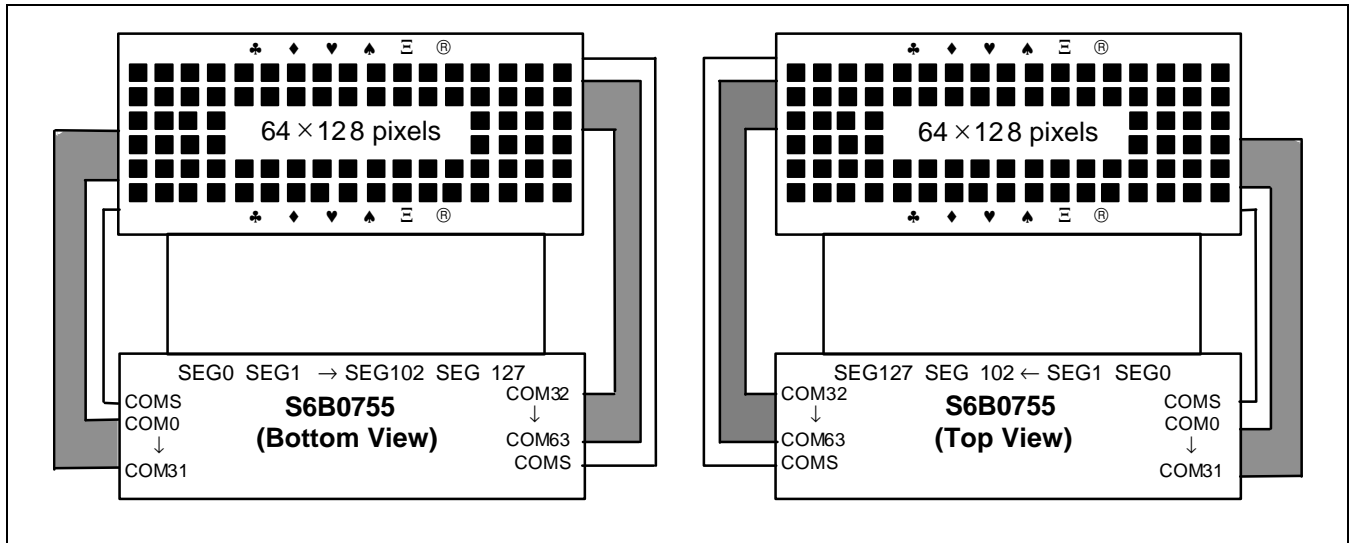


Figure 50. SHL = 1, ADC = 0

Figure 51. SHL = 1, ADC = 1