Am27S185/27S185A

8,192-Bit (2048x4) Bipolar PROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

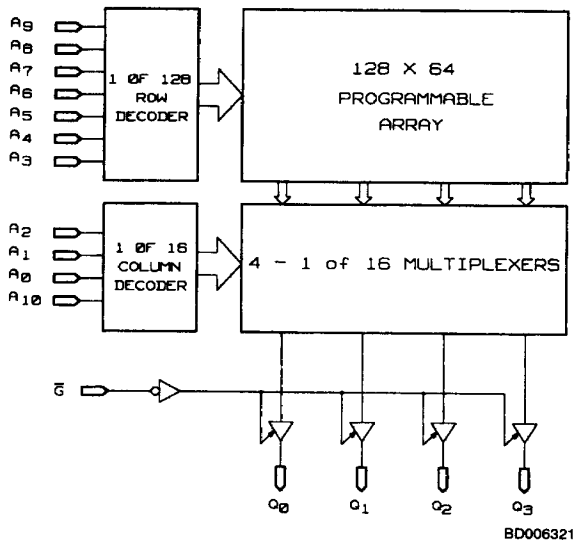
- Ultra-fast access time "A" version (35 ns Max.) — Fast access time Standard version (50 ns Max.) — allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

GENERAL DESCRIPTION

The Am27S185 (2048 words by 4 bits) is a Schottky TTL Programable Read-Only Memory (PROM).

This device has three-state outputs, compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy-word depth expansion is facilitated by an active LOW ($\overline{G}$) output enable.

BLOCK DIAGRAM



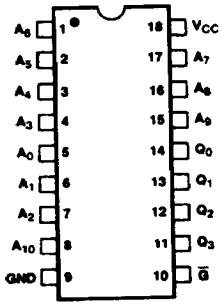
PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S185A		Am27S185	
Address Access Time	35 ns	45 ns	50 ns	55 ns
Operating Range	C	M	C	M

Publication # 03192 Rev. D Amendment /0
Issue Date: January 1989

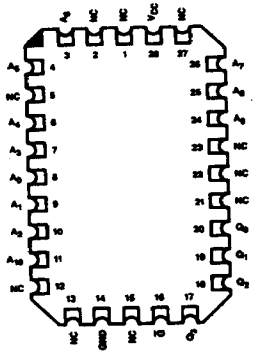
CONNECTION DIAGRAMS
Top View

DIPs*



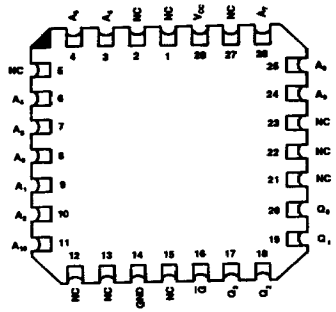
CD000373

LCC



CD000383

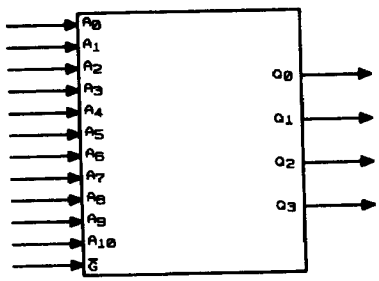
LCC**



CD009501

Note: Pin 1 is marked for orientation.
*Also available in an 18-pin Flatpack. Pinout identical to DIPs.
**Also available in a 28-pin square PLCC. Pinout identical to LCC.

LOGIC SYMBOL



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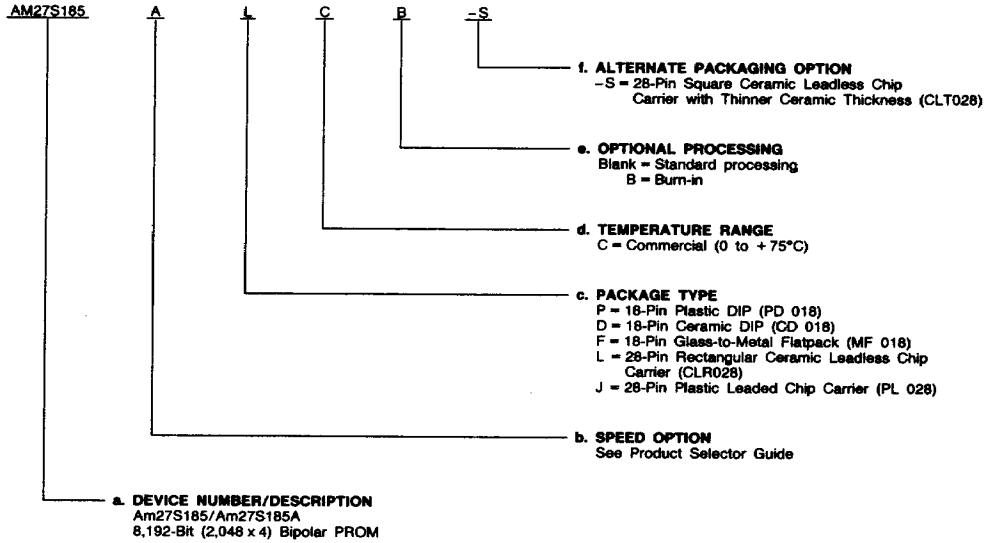
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing
f. Alternate Packaging Option



Valid Combinations	
AM27S185	PC, PCB, DC DCB, FC, FCB, LC, LCB, LC-S, LCB-S, JC, JCB
AM27S185A	

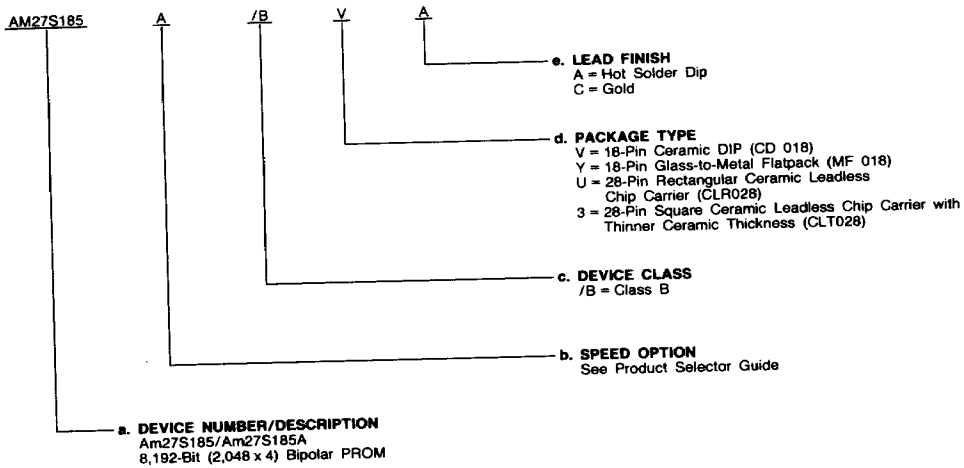
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27S185	/BVA, /BYC, /BUA, /B3A,
AM27S185A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

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MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

$A_0 - A_{10}$ Address Inputs
The 11-bit field presented at the address inputs selects one of 2,048 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G}$ Output Enable
Provides direct control of the Q-output buffers. Outputs disabled forces all three-state outputs to a floating or high-impedance state.

Enable = $\overline{G}$
Disable = G

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 V to +5.25 V

Military (M) Devices
Case Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military products 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC} (Note 1)	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0.0 V (Note 3)		−20		−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.				150	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	V
I_{CEX}	Output Leakage Current	V_{CC} = Max. $\overline{V_S}$ = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 4) V_{CC} = 5 V., T_A = 25°C			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 4) V_{CC} = 5 V., T_A = 25°C			8.0		

Notes: 1. This applies to three-state devices only.
2. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

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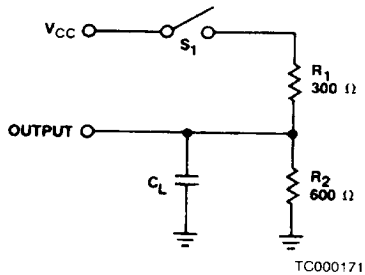
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*)

No.	Parameter Symbol	Parameter Description	Version	COM'L		MIL		Unit
				Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time	A		35		45	ns
			STD		50		55	
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	A		25		30	ns
			STD		25		30	
3	TGVQV	Delay from Output Enable Valid to Output Valid	A		25		30	ns
			STD		25		30	

See also Switching Test Circuit.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.

SWITCHING TEST CIRCUIT



Notes: 1. TAVQV is tested with switch S_1 closed and C_L = 50 pF.
2. For three-state outputs, TGVQV is tested with C_L = 50 pF to the 1.5 V level: S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGVQZ is tested with C_L = 5 pF. HIGH to high-impedance tests are made to an output steady state HIGH voltage – 0.5 V with S_1 open; LOW to high-impedance tests are made to the steady state LOW + 0.5 V level with S_1 closed.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
⟋⟋⟋	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
⟋⟋⟋	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
⟋⟋⟋	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⟋⟋⟋	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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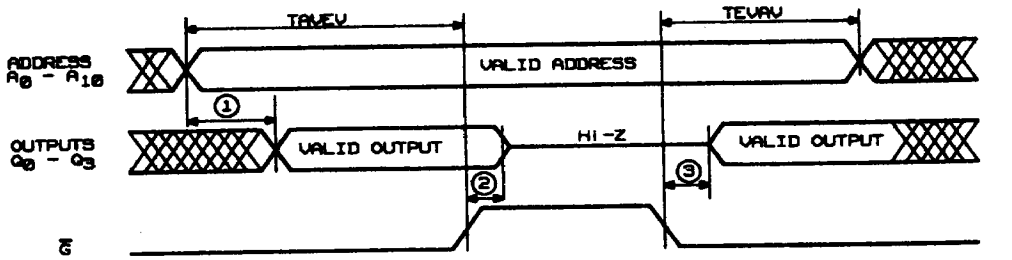

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