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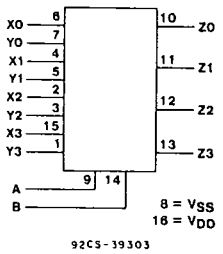
NOT RECOMMENDED FOR NEW DESIGNS

CD4519B Types

CMOS 4-Bit AND/OR Selector, Quad 2-Channel Data Selector, or Quad Exclusive NOR Gate

High-Voltage Types (20-Volt Rating)



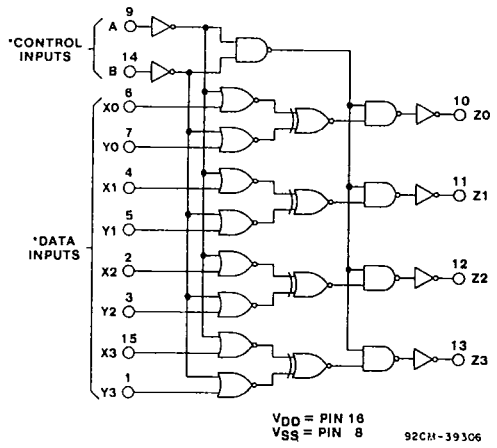
FUNCTIONAL DIAGRAM

Features:

- *Standardized, symmetrical output characteristics*
- *100% tested for quiescent current at 20V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25° C*
- *Noise margin (over full package-temperature range) = 1V at V_{DD} = 5V, 2V at V_{DD} = 10V, 2.5V at V_{DD} = 15V*
- *Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*

■ CD4519B CMOS types can be configured as 4-bit AND/OR selectors, as quad 2-channel data selectors, or as quad exclusive-NOR gates. This is achieved by setting the control inputs (A and B) to produce the particular function desired.

The CD4519B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).



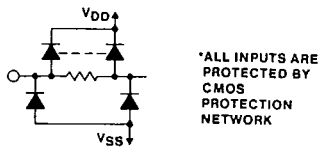


Fig. 1 - Logic diagram.

TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \odot Y_n$

Note:
$X_n \odot Y_n$ means X_n (Exclusive-NOR) Y_n

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

CD4519B Types

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
- Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA

POWER DISSIPATION PER PACKAGE (P_D):
- For T_A = -55°C to +100°C 500mW
- For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C

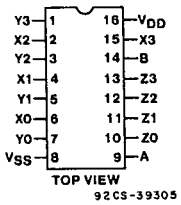
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

RECOMMENDED OPERATING CONDITIONS at 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V



CD4519B
TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	—	0, 5	5	1	1	30	30	—	0.02	1	μA
	—	0, 10	10	2	2	60	60	—	0.02	2	
	—	0, 15	15	4	4	120	120	—	0.02	4	
	—	0, 20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0, 5	5	3.84	3.66	2.52	2.16	3.06	6	—	mA
	0.5	0, 10	10	9.6	9	6.6	5.4	7.8	15.6	—	
	1.5	0, 15	15	25.2	24	16.8	14.4	20.4	40.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0, 5	5	0.05				—	0	0.05	V
	—	0, 10	10	0.05				—	0	0.05	
	—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0, 5	5	4.95				4.95	5	—	
	—	0, 10	10	9.95				9.95	10	—	
	—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	4.5	—	5	3.5				3.5	—	—	
	9	—	10	7				7	—	—	
	13.5	—	15	11				11	—	—	
Input Current I_{IN} Max	—	0, 18	18	±0.1	±0.1	±1	±1	—	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	V_{DD} (V)	Min.	Typ.	Max.	
Propagation Delay Time (t_{PHL}, t_{PLH})	5	—	180	360	ns
	10	—	75	150	
	15	—	60	120	
Transition Time (t_{THL}, t_{TLH})	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Input Capacitance (C_{IN})	Any Input	—	5	7.5	pF

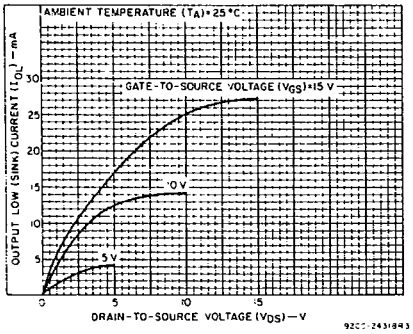


Fig. 2 — Typical output low (sink) current characteristics.

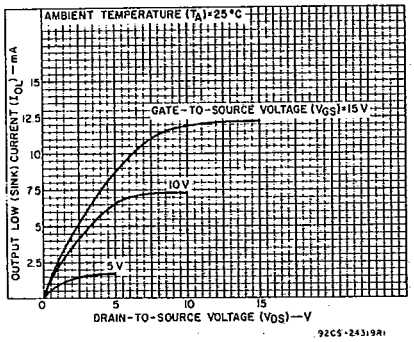


Fig. 3 — Minimum output low (sink) current characteristics.

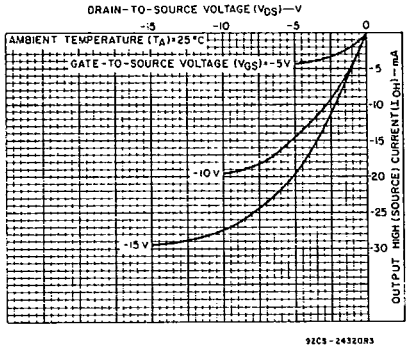


Fig. 4 — Typical output high (source) current characteristics.

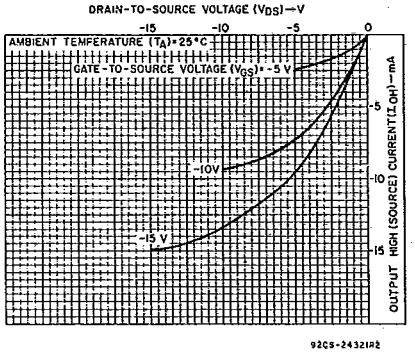


Fig. 5 — Minimum output high (source) current characteristics.

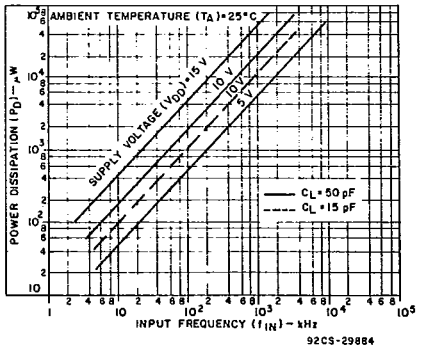


Fig. 6 — Typical dynamic power dissipation as a function of input frequency.

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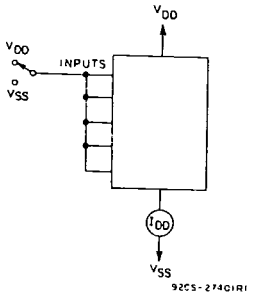


Fig. 7 — Quiescent device current test circuit.

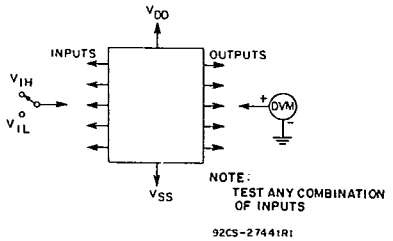


Fig. 8 — Input voltage test circuit.

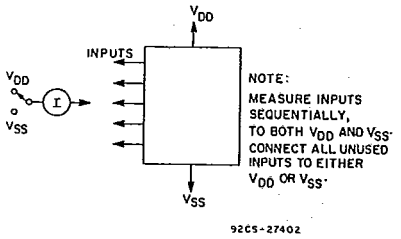
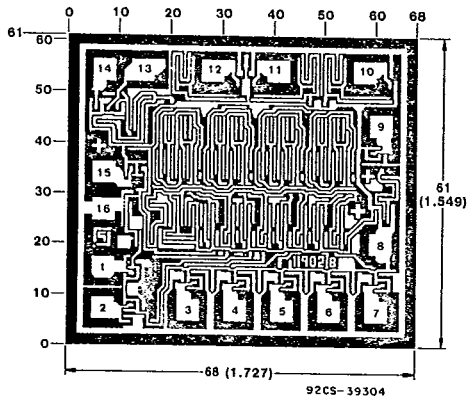


Fig. 9 — Input current test circuit.



Chip dimensions and pad layout for CD4519B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).