1M x 64/72 DRAM Module

Features

- 168 Pin JEDEC Standard, Unbuffered 8 Byte Dual In-line Memory Module
- 1Mx64, 1Mx72 Extended Data Out Page Mode DIMMs
- Performance:

		-60	-6R	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	17ns	20ns
t_{AA}	Access Time From Address	30ns	30ns	35ns
t_{RC}	Cycle Time	104ns	104ns	124ns
t_{HPC}	EDO Mode Cycle Time	25ns	25ns	30ns

- All inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V ± 0.3V Power Supply
- Au contacts
- Optimized for byte-write, non-parity, or ECC applications.
- System Performance Benefits:
  -Non buffered for increased performance
  -Reduced noise (35 V_{SS}/V_{CC} pins)
  -Byte write, byte read accesses
  -Serial PDs
- Extended Data Out (EDO) Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only, CBR and Hidden Refresh
- 1024 refresh cycles distributed across 16ms
- 10/10 addressing (Row/Column)
- Card Sizes:
  -5.25" x 1.0" x 0.102" (TSOP)
  -5.25" x 1.25" x 0.202" (SOJ)
- DRAMS in TSOP OR SOJ Packages

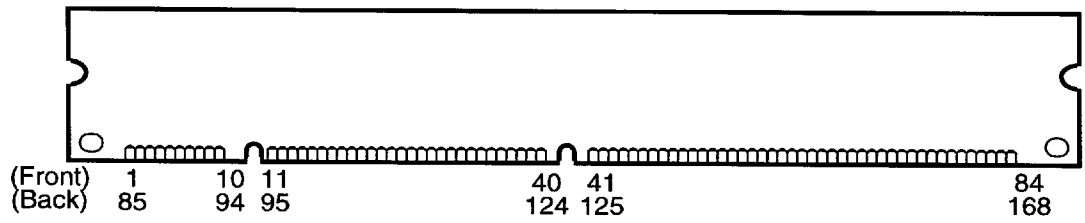
Description

IBM11N1645L/IBM11N1735Q industry standard 168-pin 8-byte Dual In-line Memory Modules (DIMMs) which are organized as 1Mx64 and 1Mx72 high speed memory arrays designed with EDO DRAMs for non-parity or ECC applications. The x64 DIMM uses 4 1Mx16 EDO DRAMs (TSOP or SOJ) and the x72 DIMM uses 4 1Mx16 plus 2 1Mx4 EDO DRAMs (all in SOJ packages). The use of EDO DRAMs allows for a reduction in Page Mode Cycle time from 40ns (Fast Page) to 25ns for 60ns DRAM modules.

The DIMMs use serial presence detects implemented via a serial EEPROM using the two pin I^2C protocol. This communication protocol uses Clock (SCL) and Data I/O (SDA) lines to synchronously clock data between the master (system logic) and the slave EEPROM device (DIMM). The EEPROM device address pins (SA0-2) are brought out to the DIMM tabs to allow 8 unique DIMM/EEPROM addresses. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes of serial PD data are available to the customer.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products include the unbuffered X72 ECC DIMMs and the buffered DIMMs (x64, x72 parity and x72 ECC Optmized) for applications which can benefit from the on-card buffers.

Card Outline (TSOP version shown)



50H8035
SA14-4630-03
Revised 8/96

Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe	V_{CC}	Power (3.3V)
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE0}$, $\overline{WE2}$	Read/write Input	NC	No Connect
$\overline{OE0}$, $\overline{OE2}$	Output Enable	DU	Don't Use
A0 - A9	Address Inputs	SCL	Serial Presence Detect Clock Input
DQx	Data Input/Output	SDA	Serial Presence Detect Data Input
CBx	Check Bit Data Input/Output	SA0-2	Serial Presence Detect Address Inputs

Pinout

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	22	CB1	106	CB5	43	V_{SS}	127	V_{SS}	64	V_{SS}	148	V_{SS}
2	DQ0	86	DQ32	23	V_{SS}	107	V_{SS}	44	$\overline{OE2}$	128	DU	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	$\overline{RAS2}$	129	NC	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	$\overline{CAS2}$	130	$\overline{CAS6}$	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V_{CC}	110	V_{CC}	47	$\overline{CAS3}$	131	$\overline{CAS7}$	68	V_{SS}	152	V_{SS}
6	V_{CC}	90	V_{CC}	27	$\overline{WE0}$	111	DU	48	$\overline{WE2}$	132	DU	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	$\overline{CAS0}$	112	$\overline{CAS4}$	49	V_{CC}	133	V_{CC}	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	$\overline{CAS1}$	113	$\overline{CAS5}$	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	$\overline{RAS0}$	114	NC	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	$\overline{OE0}$	115	DU	52	CB2	136	CB6	73	V_{CC}	157	V_{CC}
11	DQ8	95	DQ40	32	V_{SS}	116	V_{SS}	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V_{SS}	96	V_{SS}	33	A0	117	A1	54	V_{SS}	138	V_{SS}	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V_{SS}	162	V_{SS}
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	NC	163	NC
17	DQ13	101	DQ45	38	NC	122	NC	59	V_{CC}	143	V_{CC}	80	NC	164	NC
18	V_{CC}	102	V_{CC}	39	NC	123	NC	60	DQ20	144	DQ52	81	NC	165	SA0
19	DQ14	103	DQ46	40	V_{CC}	124	V_{CC}	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V_{CC}	125	DU	62	DU	146	DU	83	SCL	167	SA2
21	CB0	105	CB4	42	DU	126	DU	63	NC	147	NC	84	V_{CC}	168	V_{CC}

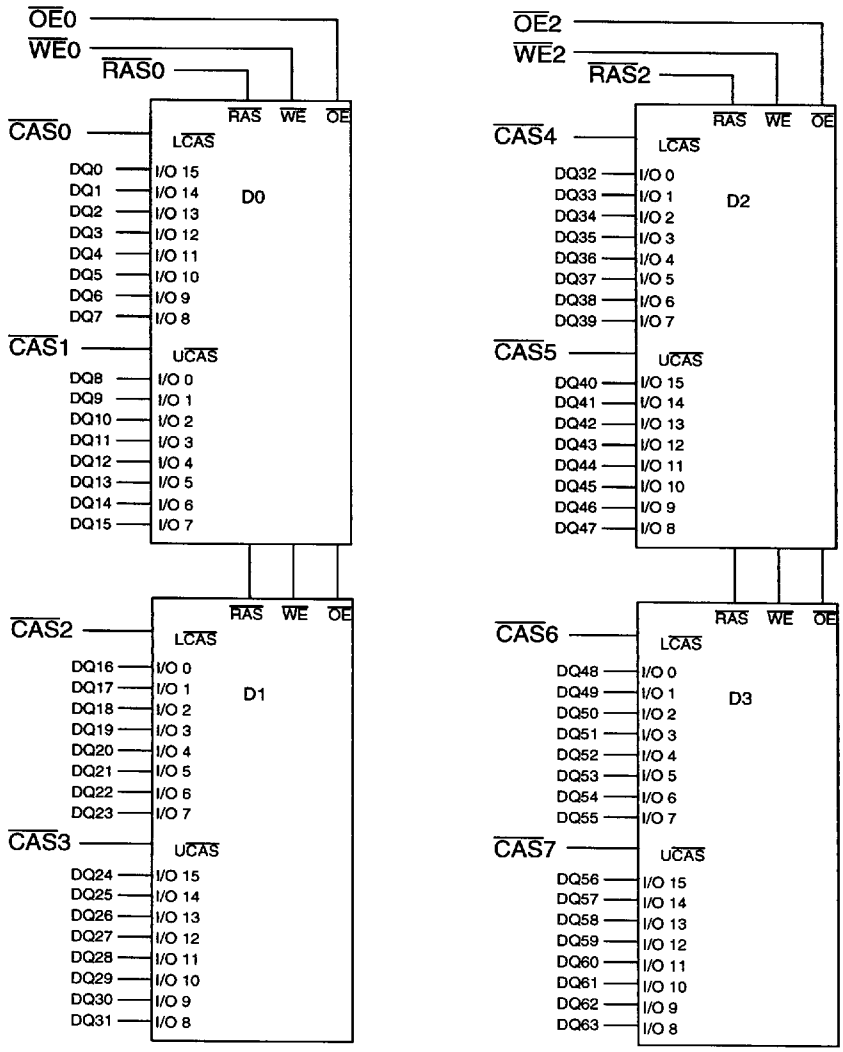
Note: All pin assignments are consistent for all 8 Byte versions.

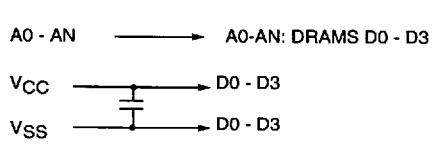
Ordering Information

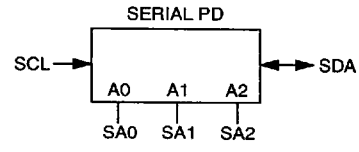
Part Number	Organization	Speed	Addr.	Leads	Dimension	Power	Notes
IBM11N1645LB-60	1Mx64	60ns	10/10	Au	5.25"x1.0"x 0.102"	3.3V	
IBM11N1645LB-6R		6Rns					1
IBM11N1645LB-70		70ns					
IBM11N1645LB-60J		60ns			5.25"x1.25"x 0.202"		2
IBM11N1645LB-6RJ		6Rns					1, 2
IBM11N1645LB-70J		70ns					2
IBM11N1735QB-60J	1Mx72	60ns					2
IBM11N1735QB-6RJ		6Rns					1, 2
IBM11N1735QB-70J		70ns					2

1. 6Rns speed sort has t_{CAC} of 17ns.
2. DRAM package designator appended to speed portion of part number on assemblies beginning with DRAM die rev E.

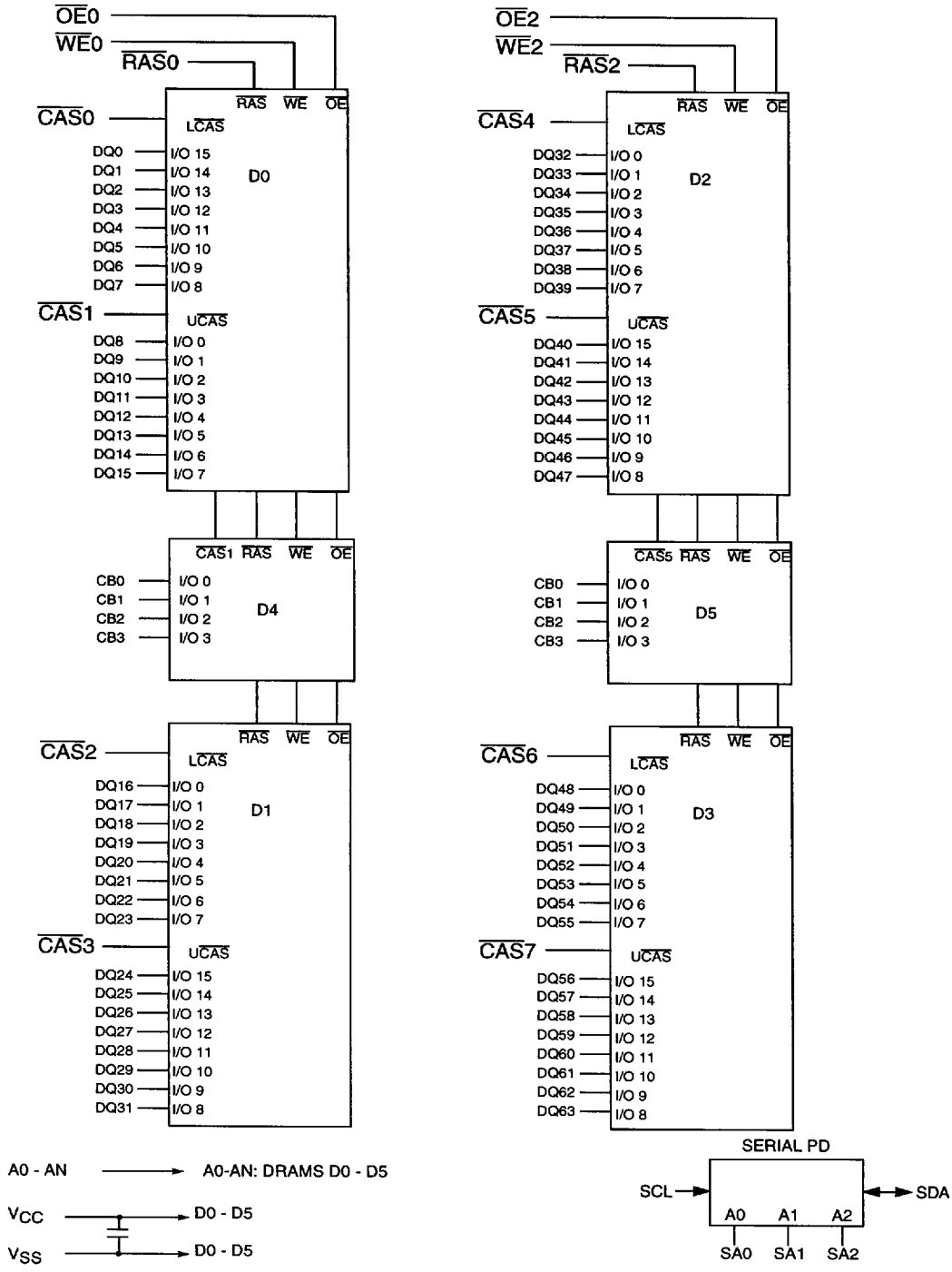
x64 DIMM Block Diagram (1 Bank, x16 DRAMs)







x64 DIMM Block Diagram (1 Bank, x16/x4)



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	DQx
Standby		H	H→X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col	Valid Data Out
Early-Write		L	L	L	X	Row	Col	Valid Data In
Late-Write		L	L	H→L	H	Row	Col	Valid Data In
RMW		L	L	H→L	L→H	Row	Col	Valid Data In/Out
EDO Page Mode - Read 1st Cycle		L	H→L	H	L	Row	Col	Valid Data Out
Subsequent Cycles		L	H→L	H	L	N/A	Col	Valid Data Out
EDO Page Mode - Write 1st Cycle		L	H→L	L	X	Row	Col	Valid Data In
Subsequent Cycles		L	H→L	L	X	N/A	Col	Valid Data In
EDO Page Mode - RMW 1st Cycle		L	H→L	H→L	L→H	Row	Col	Valid Data In/Out
Subsequent Cycles		L	H→L	H→L	L→H	N/A	Col	Valid Data In/Out
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	X	High Impedance
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col	Data Out
	Write	L→H→L	L	H	X	Row	Col	Data In
Self Refresh		H→L	L	H	X	X	X	High Impedance

Serial Presence Detect

Byte #	Description		SPD Entry Value	SPD Entry								
				Binary								Hex
				Bit 7	Bit 6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
0	Number of SPD Bytes		128	1	0	0	0	0	0	0	0	80
1	Total # Bytes in Serial PD		256	0	0	0	0	1	0	0	0	08
2	Memory Type		EDO	0	0	0	0	0	0	1	0	02
3	# of Row Addresses		10	0	0	0	0	1	0	1	0	0A
4	# of Column Addresses		10	0	0	0	0	1	0	1	0	0A
5	# of DIMM Banks		1	0	0	0	0	0	0	0	1	01
6	Module Data Width		x64	0	1	0	0	0	0	0	0	40
			x72	0	1	0	0	1	0	0	0	48
7	Module Data Width (Cont.)		0	0	0	0	0	0	0	0	0	00
8	Module Interface Levels		LVTTL	0	0	0	0	0	0	0	1	01
9	$\overline{RAS}$ Access	60ns	60	0	0	1	1	1	1	0	0	3C
		70ns	70	0	1	0	0	0	1	1	0	46
10	$\overline{CAS}$ Access	15ns	15	0	0	0	0	1	1	1	1	0F
		17ns	17	0	0	0	1	0	0	0	1	11
		20ns	20	0	0	0	1	0	1	0	0	14
11	Dimm Config(Error Det/Corr.)	x64	None	0	0	0	0	0	0	0	0	00
		x72	ECC	0	0	0	0	0	0	1	0	02
12	Refresh Rate/Type		Normal 15.6 µs	0	0	0	0	0	0	0	0	00
13	Primary DRAM Organization		x16	0	0	0	1	0	0	0	0	10
14	Secondary DRAM Organization	x64	Undefined	0	0	0	0	0	0	0	0	00
		x72	x4	0	0	0	0	0	1	0	0	04

Absolute Maximum Ratings

Symbol	Parameter		Rating (3.3V)	Units	Notes
V_{CC}	Power Supply Voltage		-0.5 to +4.6	V	1
V_{IN}	Input Voltage		-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
$V_{IN/OUT}$ (SPD)	Input Voltage (Serial PD Device)		-0.3 to +6.5	V	1
V_{OUT}	Output Voltage		-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature		0 to +70	°C	1
T_{STG}	Storage Temperature		-55 to +125	°C	1
P_D	Power Dissipation	x64	2.4	W	1
		x72	3.1	W	1
I_{OUT}	Short Circuit Output Current		50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3V			Units	Notes
		Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 1.2V for pulse widths of ≤ 4.0ns (or V_{CC} + 1.0V for ≤ 8.0ns). Additionally, V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Max x64	Max x72	Units
C_{I1}	Input Capacitance (A0-A9)	45	55	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{WE}$, $\overline{OE}$)	40	45	pF
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	20	pF
C_{I4}	Input Capacitance ($\overline{SCL}$, SA0-3)	8	8	pF
C_{IO1}	Input/Output Capacitance (DQx, CBx)	11	11	pF
C_{IO2}	Input/Output Capacitance (SDA)	10	10	pF

DC Electrical Characteristics (T_A= 0 to +70°C, V_{CC}= 3.3V ± 0.3V)

Symbol	Parameter		x64		x72		Units	Notes
			Min.	Max.	Min.	Max.		
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min.)	-60/6R	—	660	—	850	mA	1, 2, 3
		-70	—	560	—	720		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		—	8	—	10	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	-60/6R	—	660	—	850	mA	1, 3
		-70	—	560	—	720		
I_{CC4}	EDO Page Mode Current Average Power Supply Current, EDO Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{HPC} = t_{HPC} min)	-60/6R	—	360	—	490	mA	1, 2, 3
		-70	—	320	—	450		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	4	—	6	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60/6R	—	660	—	850	mA	1, 3
		-70	—	560	—	720		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 0.3V)), All Other Pins Not Under Test = 0V	$\overline{RAS}$, $\overline{WE}$, $\overline{OE}$	-20	+20	-30	+30	µA	
		$\overline{CAS}$	-10	+10	-20	+20		
		Address	-40	+40	-60	+60		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output Level (TTL) Output "H" Level Voltage (I_{OUT} = -2.5mA)		2.4	V_{CC}	2.4	V_{CC}	V	
V_{OL}	Output Level (TTL) Output "L" Level Voltage (I_{OUT} = +2.1mA)		0.0	0.4	0.0	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ =V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ =V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3V ± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required..
3. AC measurements assume t_T = 2ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-6R		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	—	104	—	124	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	10	10K	10	10K	12	10K	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	10	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	14	45	14	43	14	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	12	30	12	30	12	35	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	10	—	10	—	12	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	50	—	50	—	55	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	15	—	15	—	15	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	0	—	0	—	ns	4
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	0	—	ns	4
t_T	Transition Time (Rise and Fall)	2	30	2	30	2	30	ns	

1. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
3. Either t_{CDD} or t_{ODD} must be satisfied.
4. Either t_{DZC} or t_{DZO} must be satisfied.

Write Cycle

Symbol	Parameter	-60		-6R		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	10	—	10	—	12	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	12	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	—	10	—	12	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	—	10	—	12	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	0	—	ns	2
t_{DH}	D_{IN} Hold Time	10	—	10	—	12	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-6R		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	17	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	30	—	35	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	15	—	17	—	20	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	ns	
t_{OES}	$\overline{OE}$ setup time prior to $\overline{CAS}$	5	—	5	—	5	—	ns	
t_{ORD}	$\overline{OE}$ setup time prior to $\overline{RAS}$ (Hidden Refresh)	0	—	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	15	—	15	—	ns	5
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	—	15	—	15	—	15	ns	4
t_{OFF}	Output Buffer Turn-off Delay	—	15	—	15	—	15	ns	4, 6

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
5. Either t_{CDD} or t_{ODD} must be satisfied.
6. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever is last.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-6R		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	135	—	135	—	162	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	79	—	79	—	94	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	34	—	36	—	44	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	49	—	49	—	59	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	10	—	10	—	12	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

EDO Mode Cycle

Symbol	Parameter	-60		-6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{HCAS}	$\overline{CAS}$ Pulse Width (EDO Page Mode)	10	10K	10	10K	12	10K	ns	
t_{HPC}	EDO Page Mode Cycle Time (Read/Write)	25	—	25	—	30	—	ns	
t_{HPRWC}	EDO Page Mode Read Modify Write Cycle Time	60	—	60	—	72	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	5	—	5	—	5	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	0	10	0	15	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	10	—	10	—	10	—	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	35	35	—	40	ns	1
t_{RASP}	EDO Page Mode $\overline{RAS}$ Pulse Width	60	125K	60	125K	70	125K	ns	
t_{OEP}	$\overline{OE}$ High Pulse Width	10	—	10	—	10	—	ns	
t_{OEHC}	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	10	—	10	—	10	—	ns	

1. Measured with the specified current load and 100pF at V_{OL} = 0.8V and V_{OH} = 2.0V.

Refresh Cycle

Symbol	Parameter	-60		-6R		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	5	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	5	—	ns	
t_{REF}	Refresh Period	—	16	—	16	—	16	ms	1

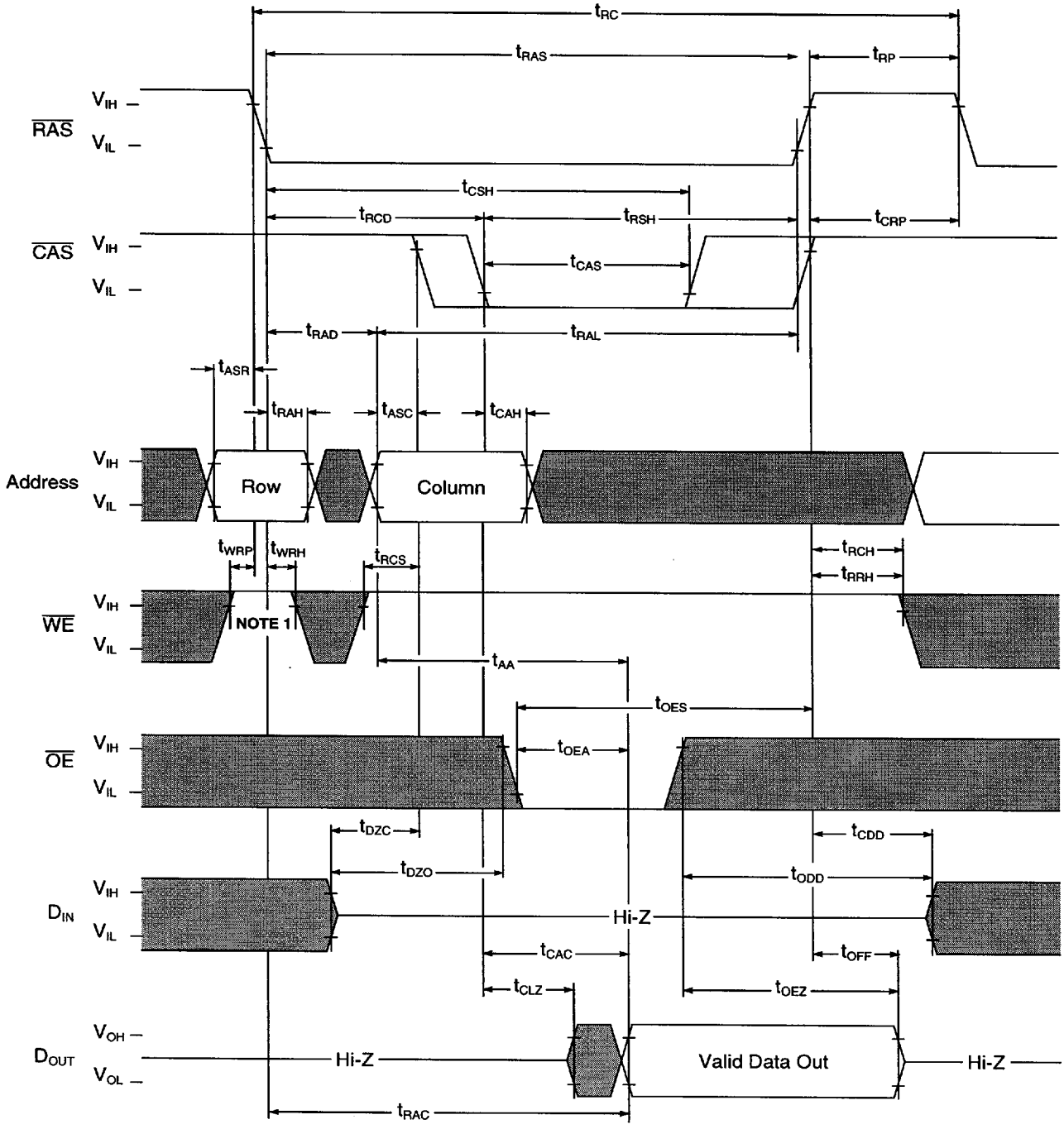
1. 1024 refreshes are required every 16ms.

Presence Detect Read and Write Cycle

Symbol	Parameter	Min	Max	Unit	Notes
f_{SCL}	SCL Clock Frequency		100	kHZ	
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns	
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs	
t_{LOW}	Clock Low Period	4.7		µs	
t_{HIGH}	Clock High Period	4.0		µs	
$t_{SU:STA}$	Start Condition Setup Time(for a Repeated Start Condition)	4.7		µs	
$t_{HD:DAT}$	Data in Hold Time	0		µs	
$t_{SU:DAT}$	Data in Setup Time	250		ns	
t_r	SDA and SCL Rise Time		1	µs	
t_f	SDA and SCL Fall Time		300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs	
t_{DH}	Data Out Hold Time	300		ns	
t_{WR}	Write Cycle Time		15	ms	1

1. The write cycle time(tWR) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

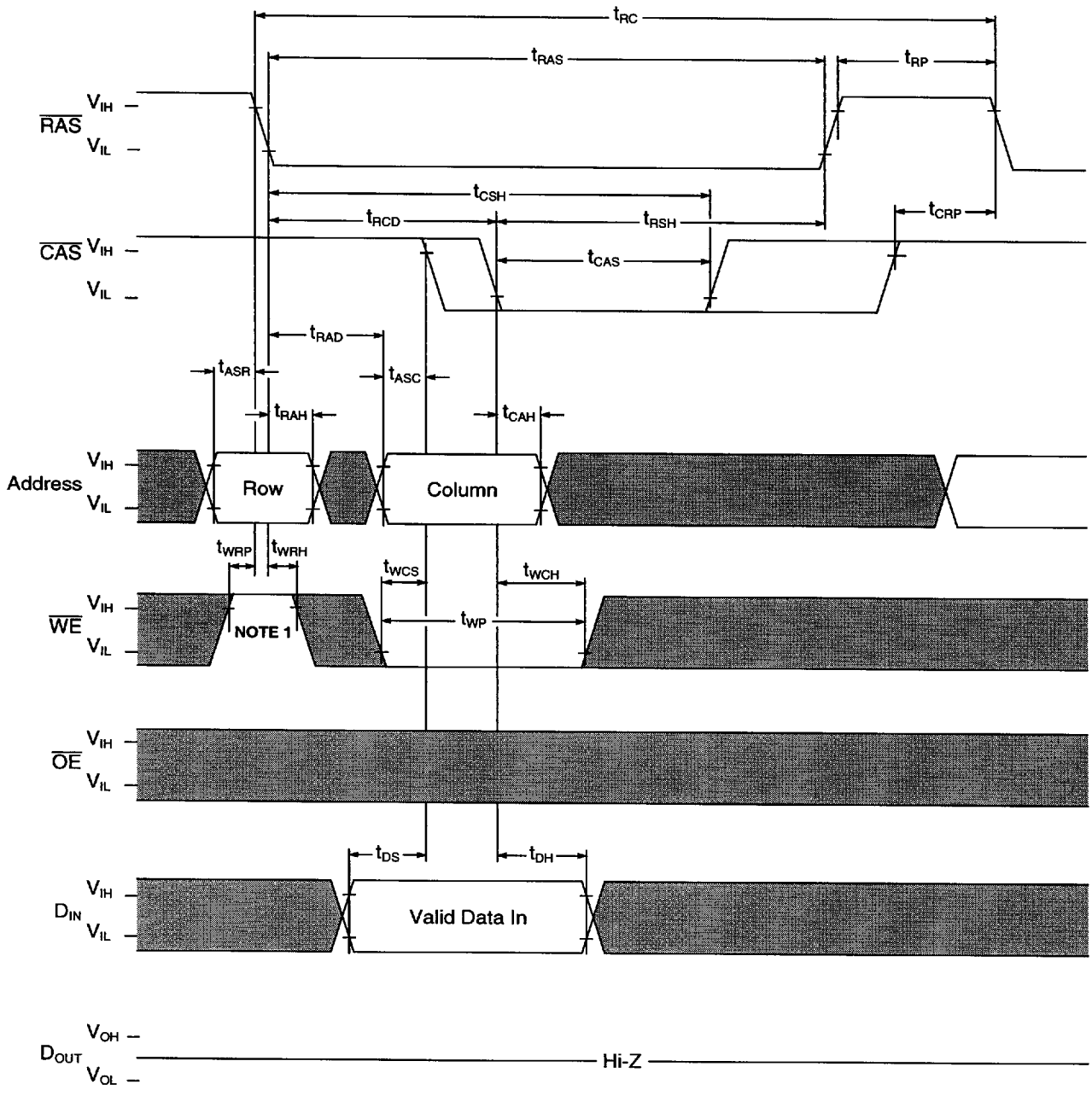
Read Cycle



: "H": or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

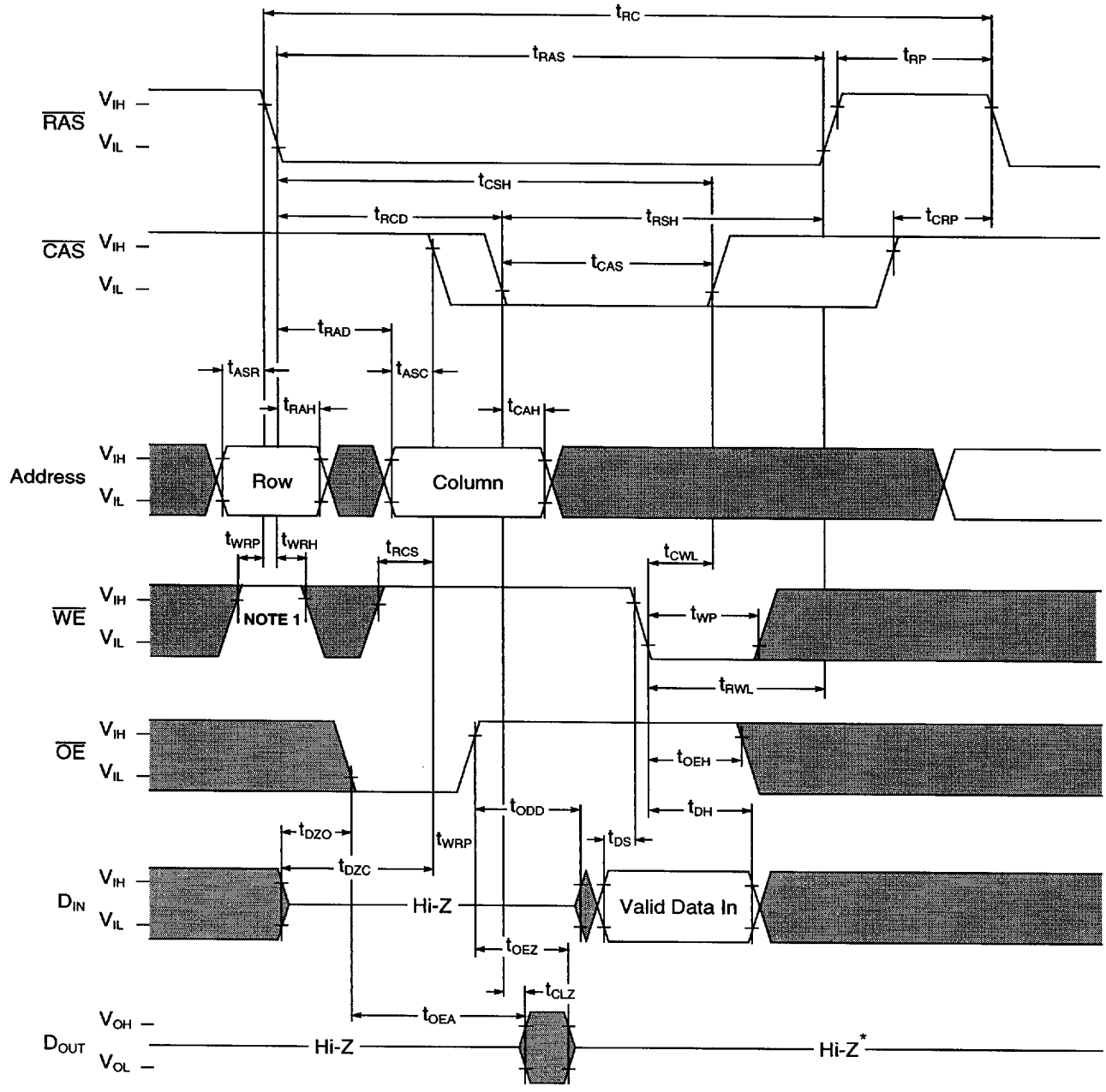
Write Cycle (Early Write)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Write Cycle (Late Write)

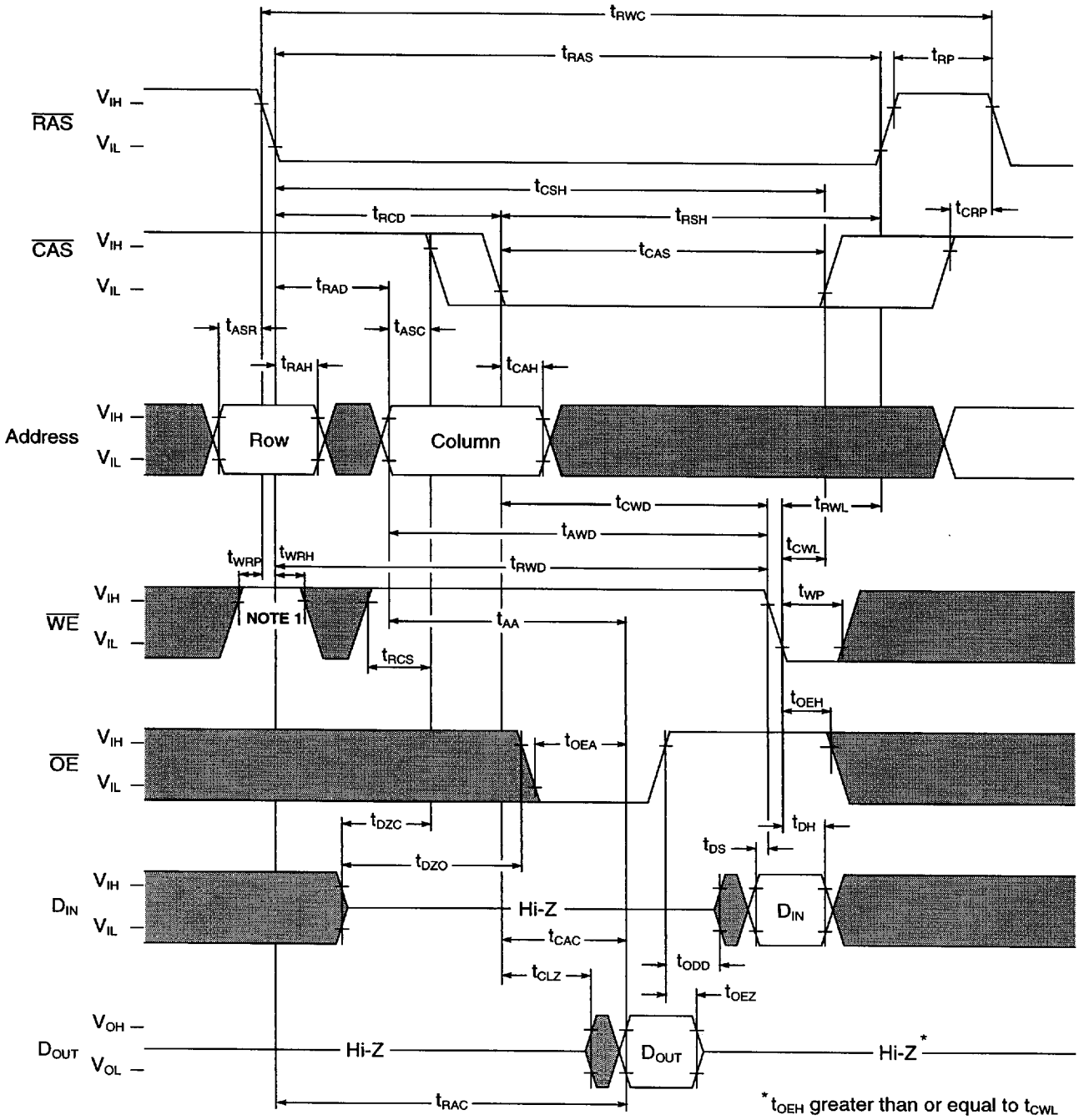


: "H" or "L"

* t_{OEH} greater than or equal to t_{CWL}

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

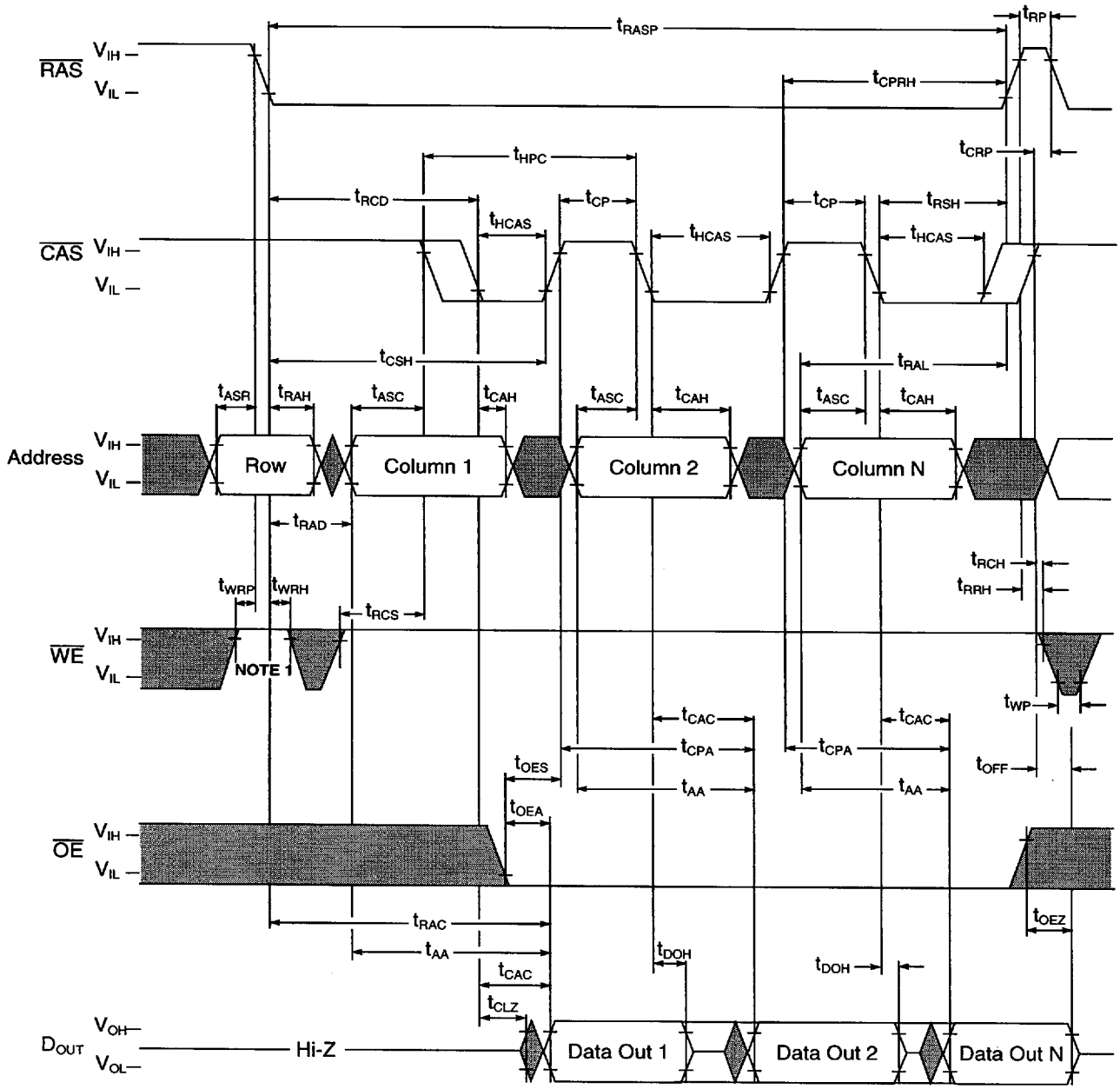
Read-Modify-Write-Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

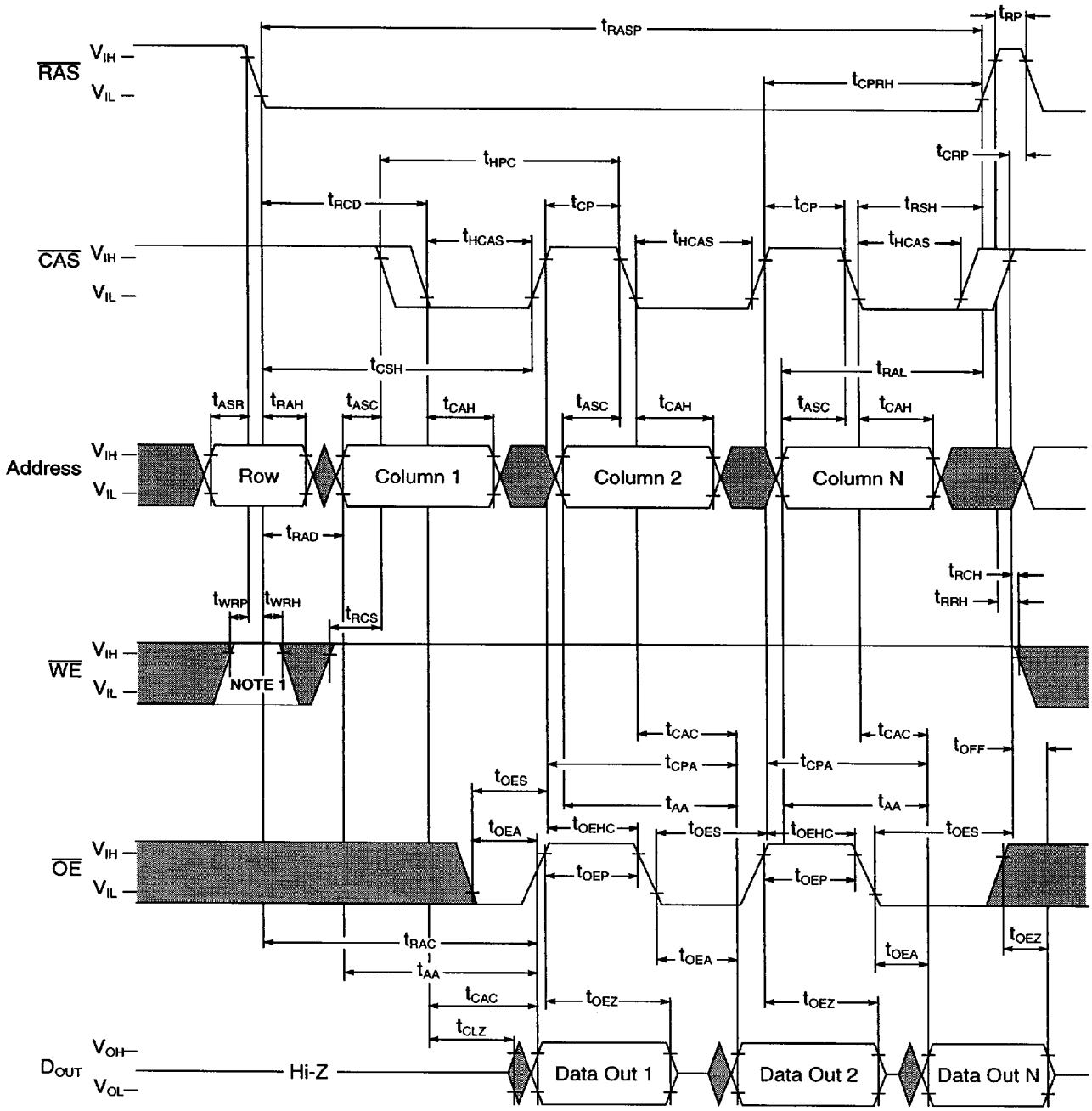
EDO Page Mode Read Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

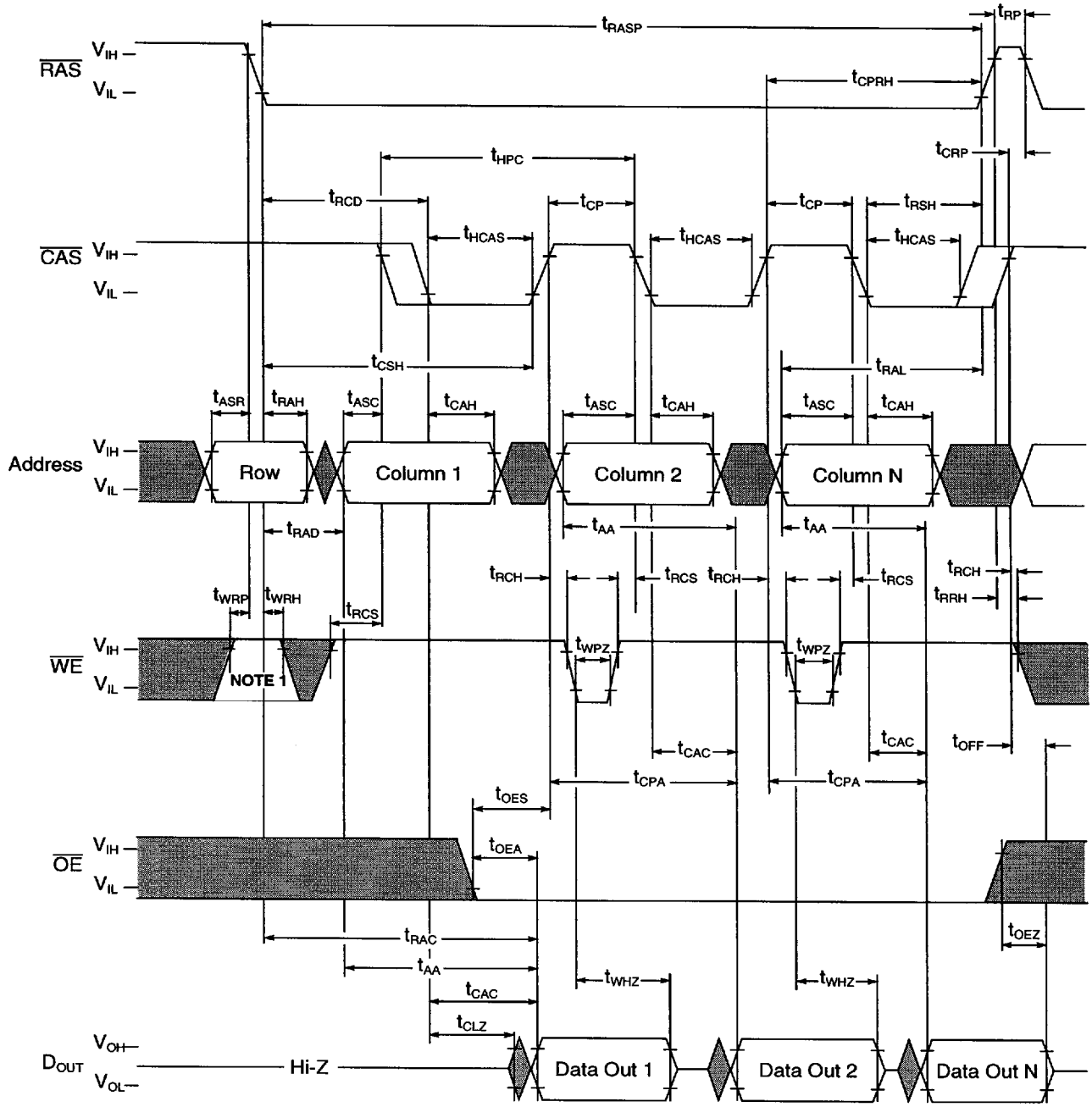
EDO Page Mode Read Cycle ($\overline{OE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

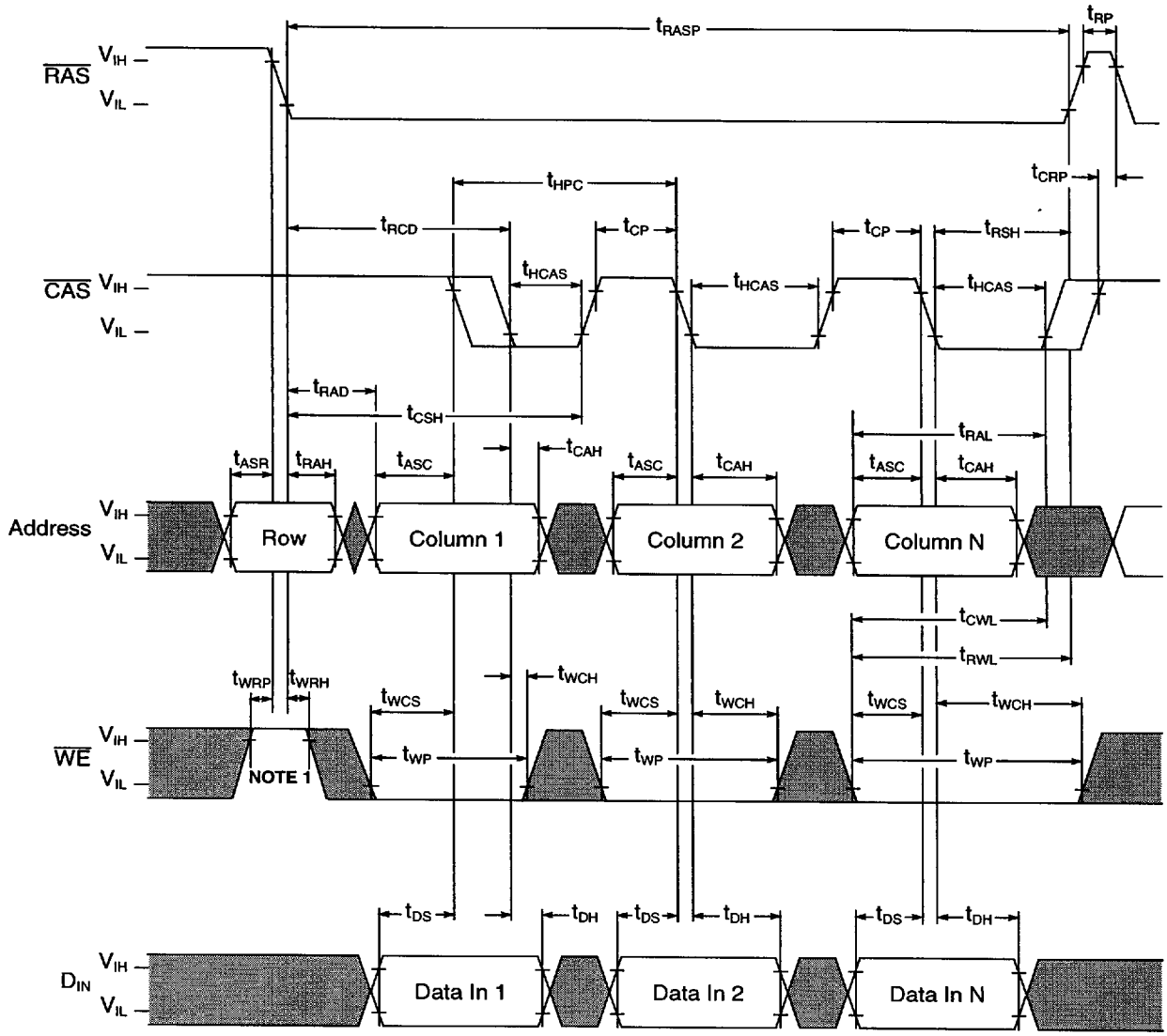
EDO Page Mode Read Cycle ($\overline{WE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO Page Mode Early Write Cycle

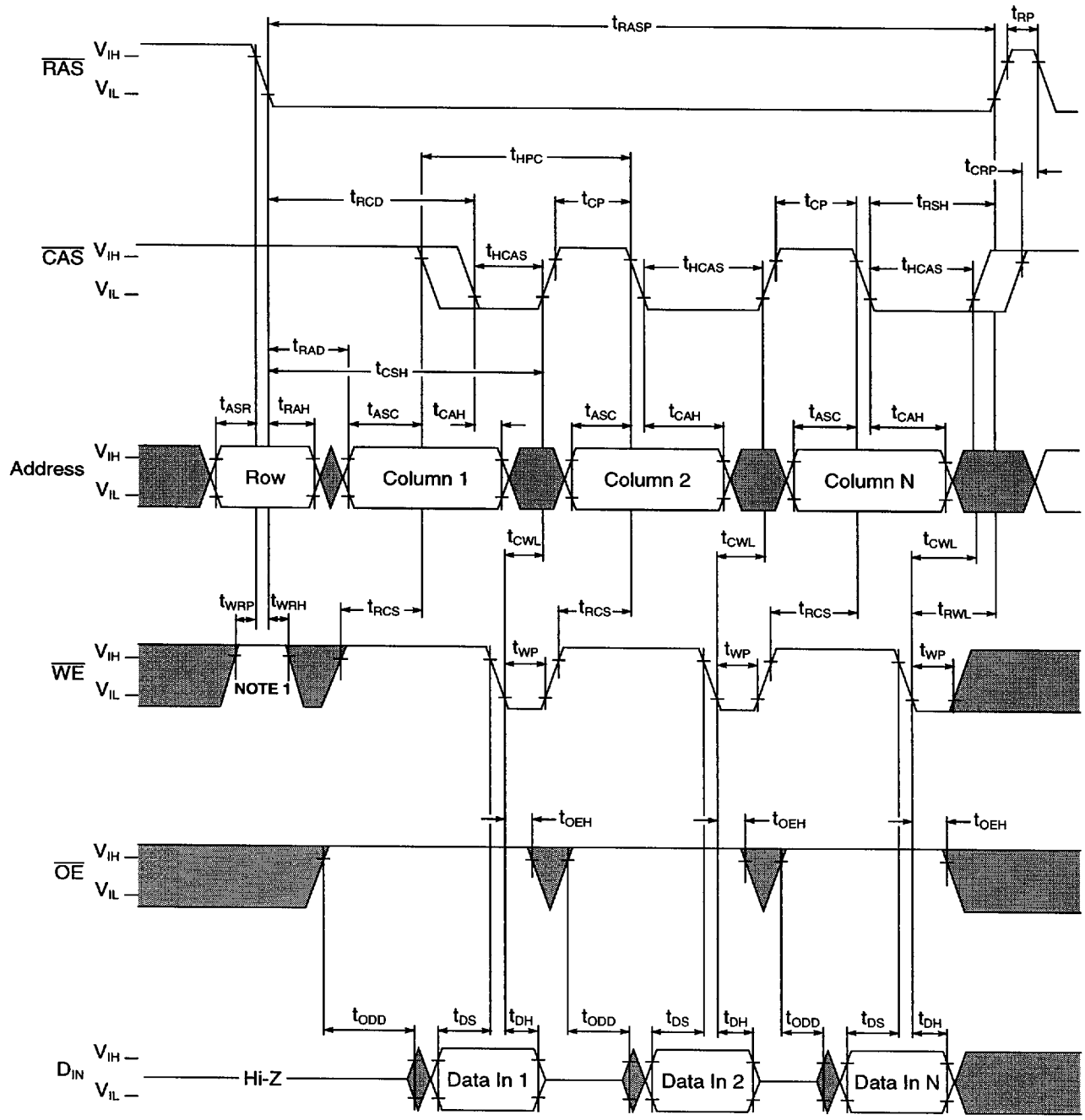


: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

$\overline{OE}$ = Don't care

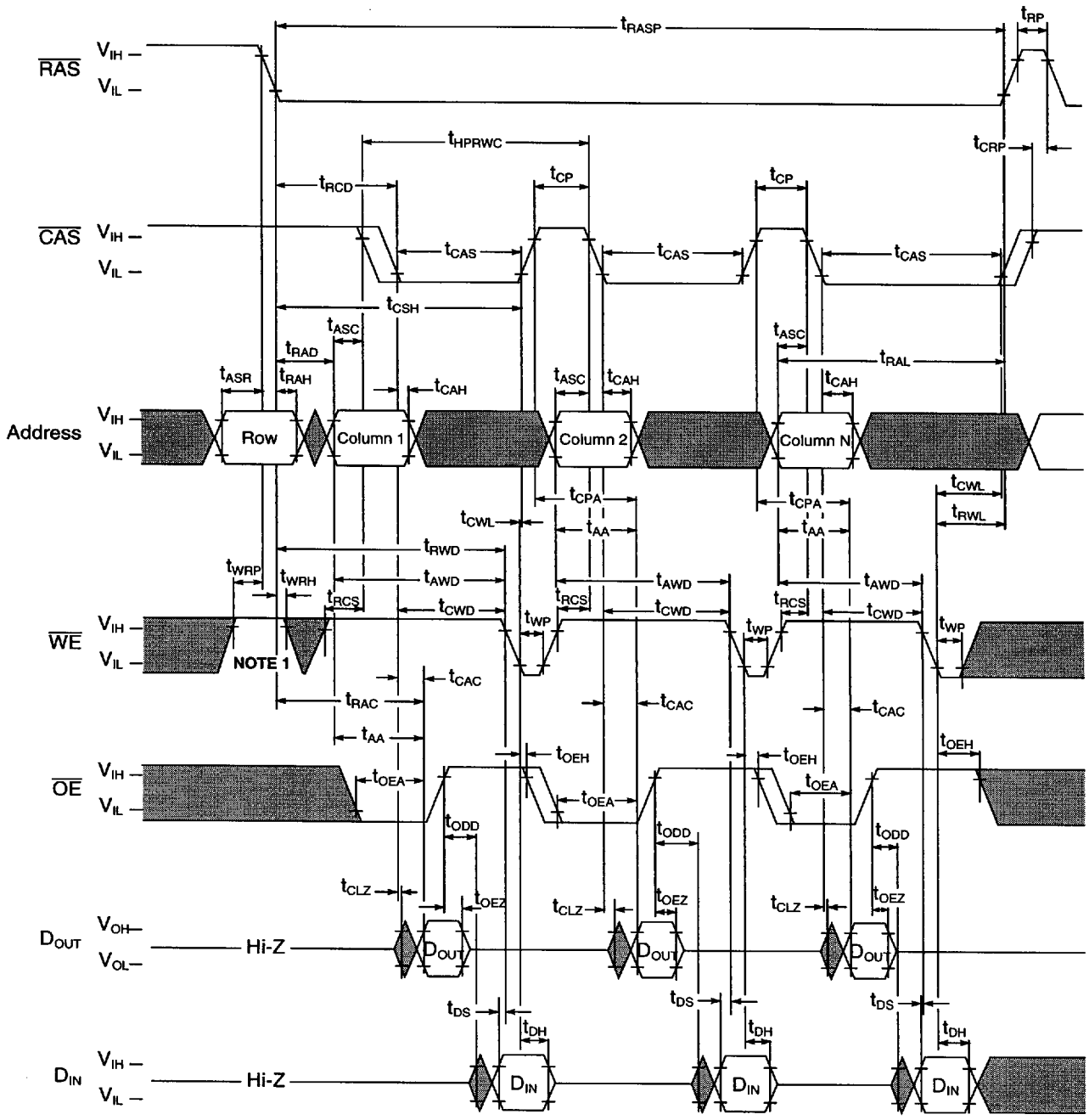
EDO Page Mode Late Write Cycle



: "H" or "L"

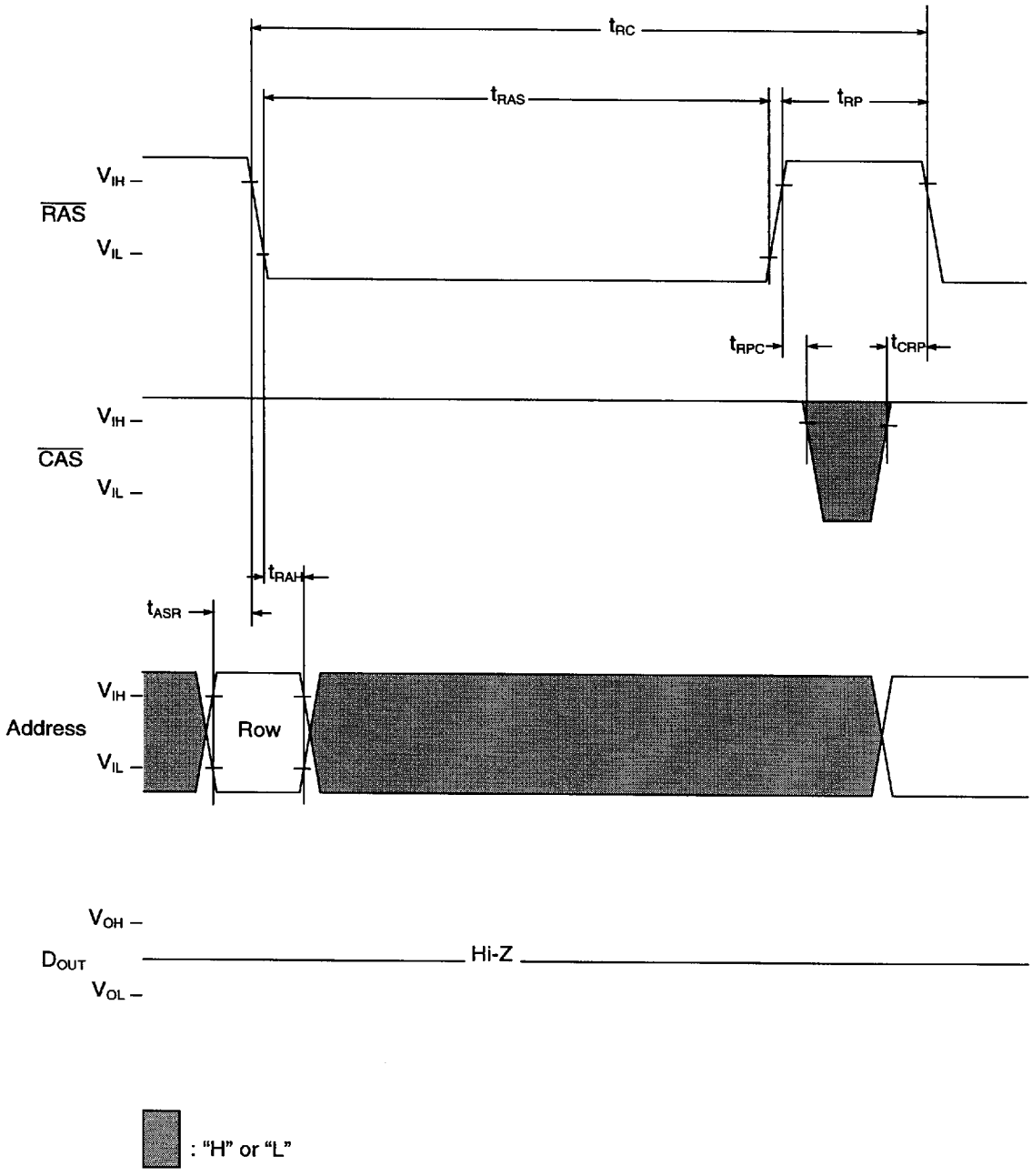
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO Page Mode Read Modify Write Cycle



NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

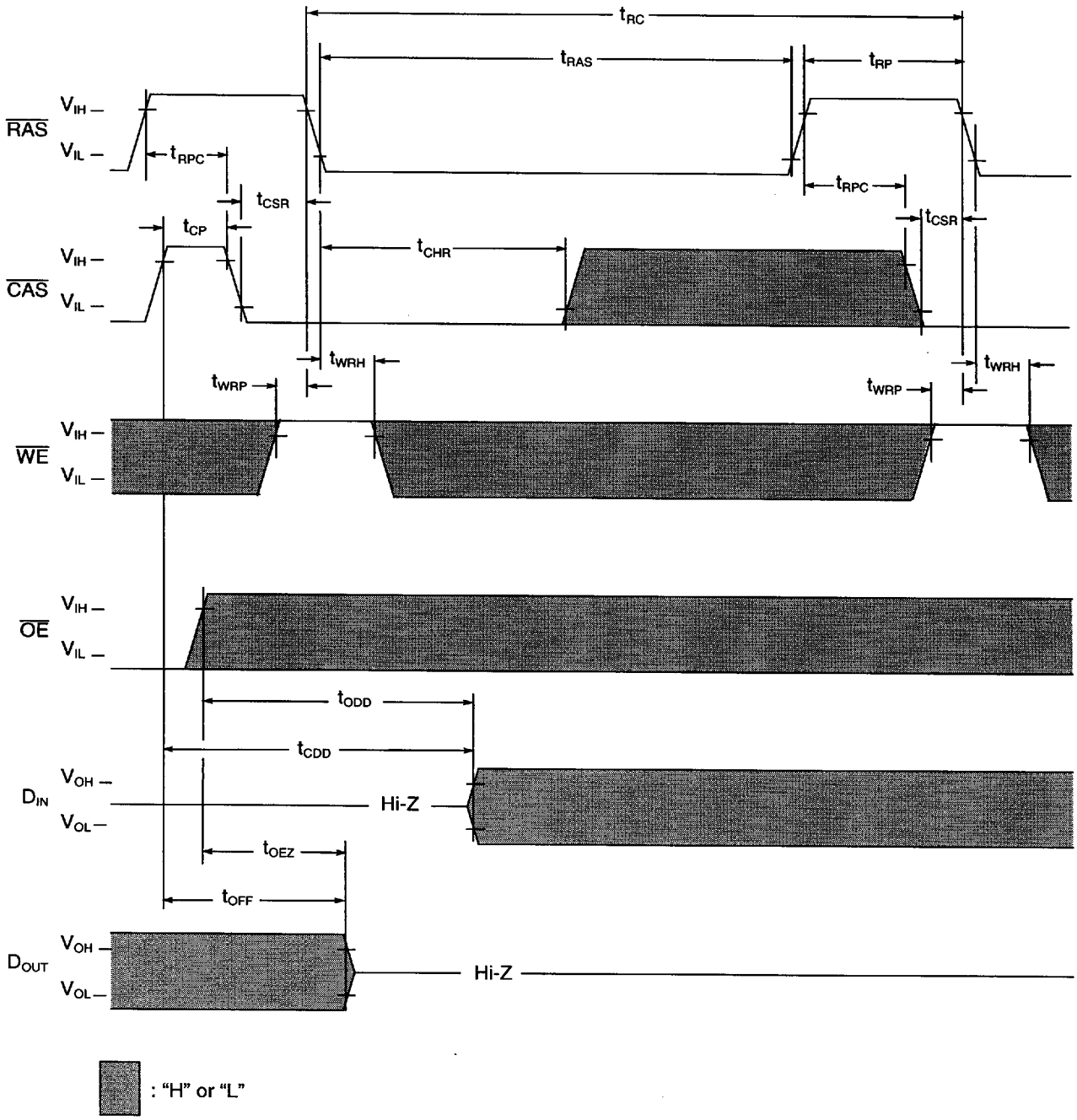
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

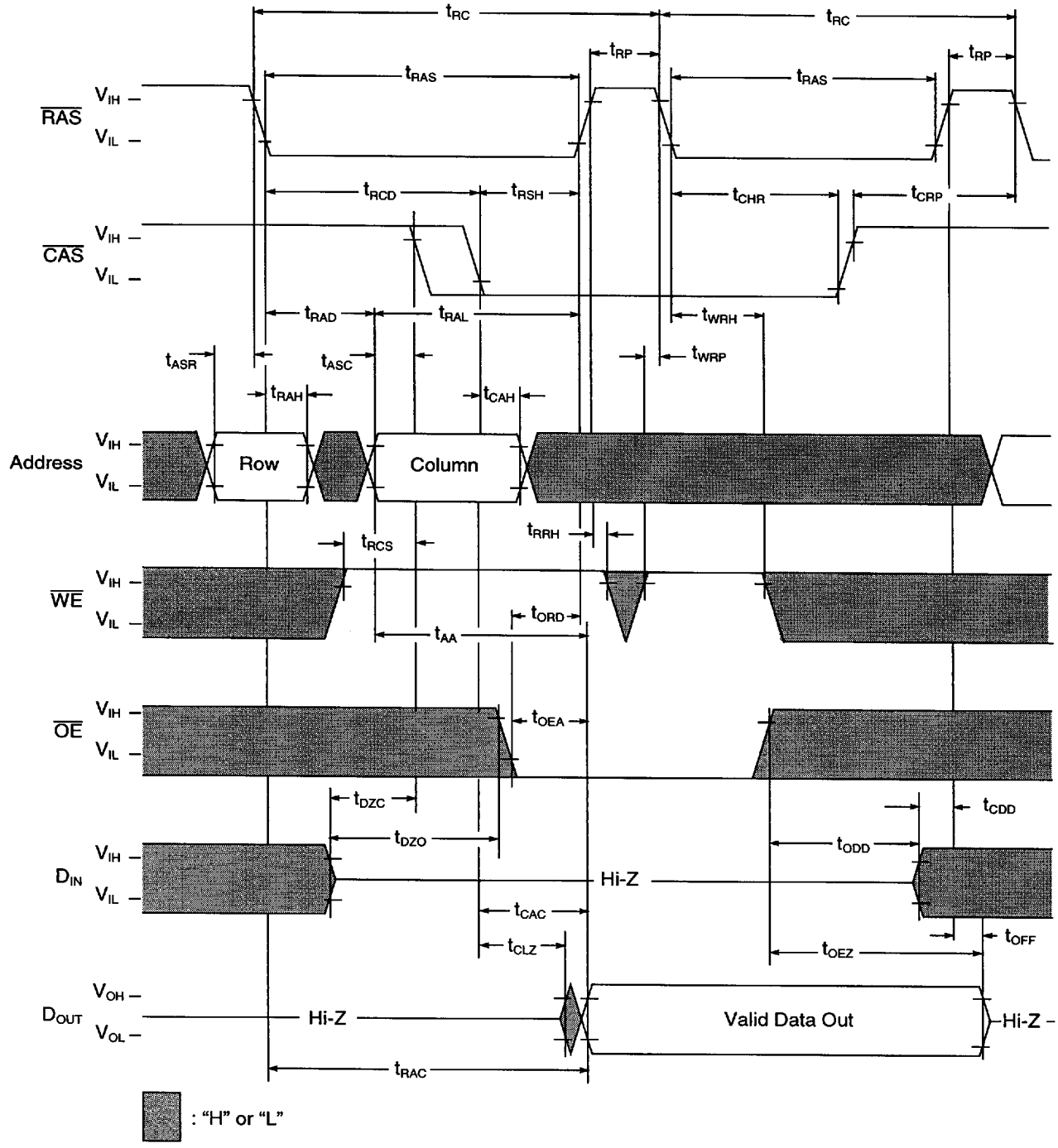
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



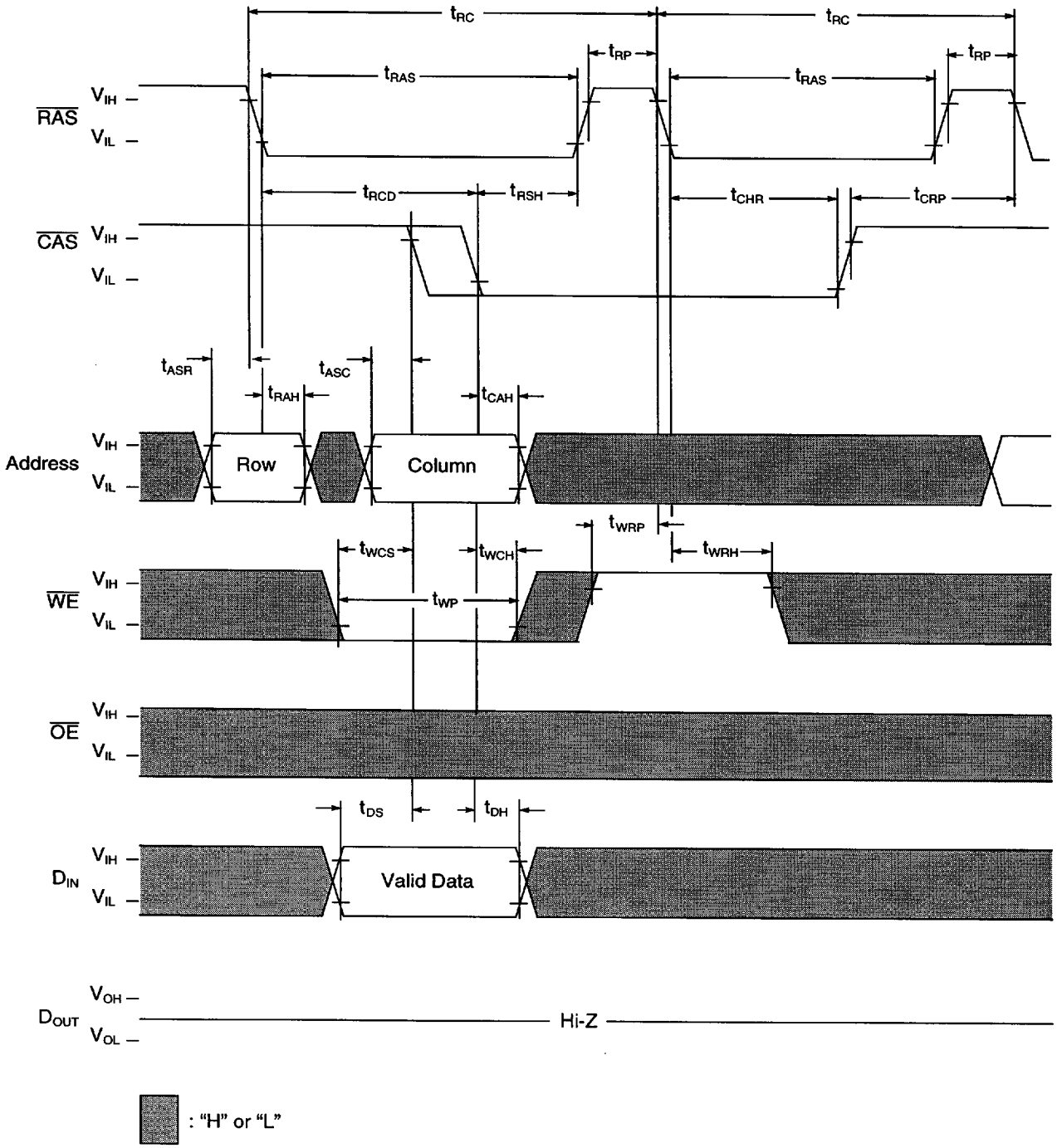
: "H" or "L"

NOTE: Address is "H" or "L"

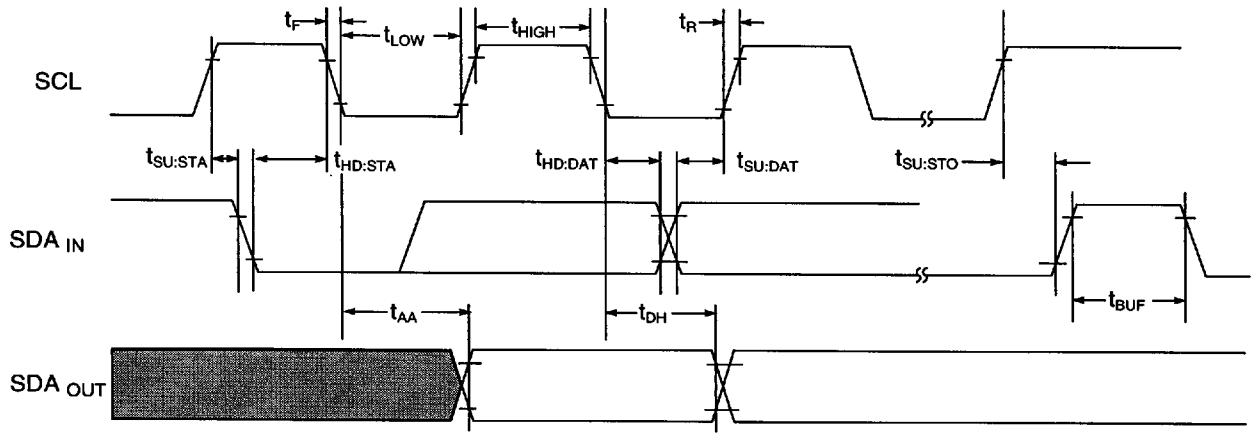
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Presence Detect (EEPROM) Bus Timing



Presence Detect Operation

Clock and Data Conventions: Data states on the SDA line can change only during SCL low. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 1 & Figure 2).

Start Condition: All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is high. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition: All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the serial PD device into standby power mode.

Acknowledge: Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).
The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, The PD device, will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 1. Data Window

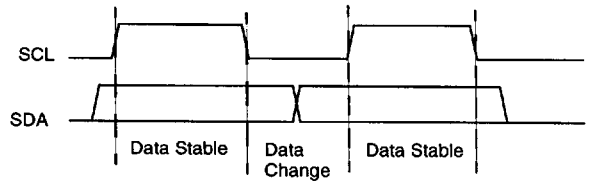


Figure 2. Definition of Start & Stop

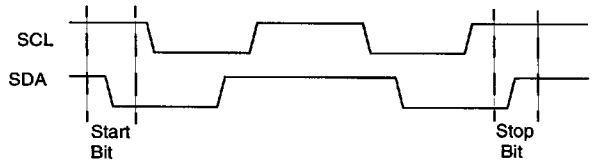
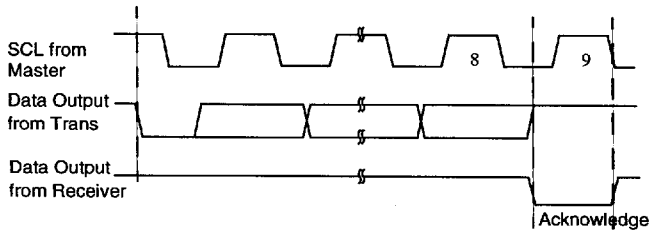
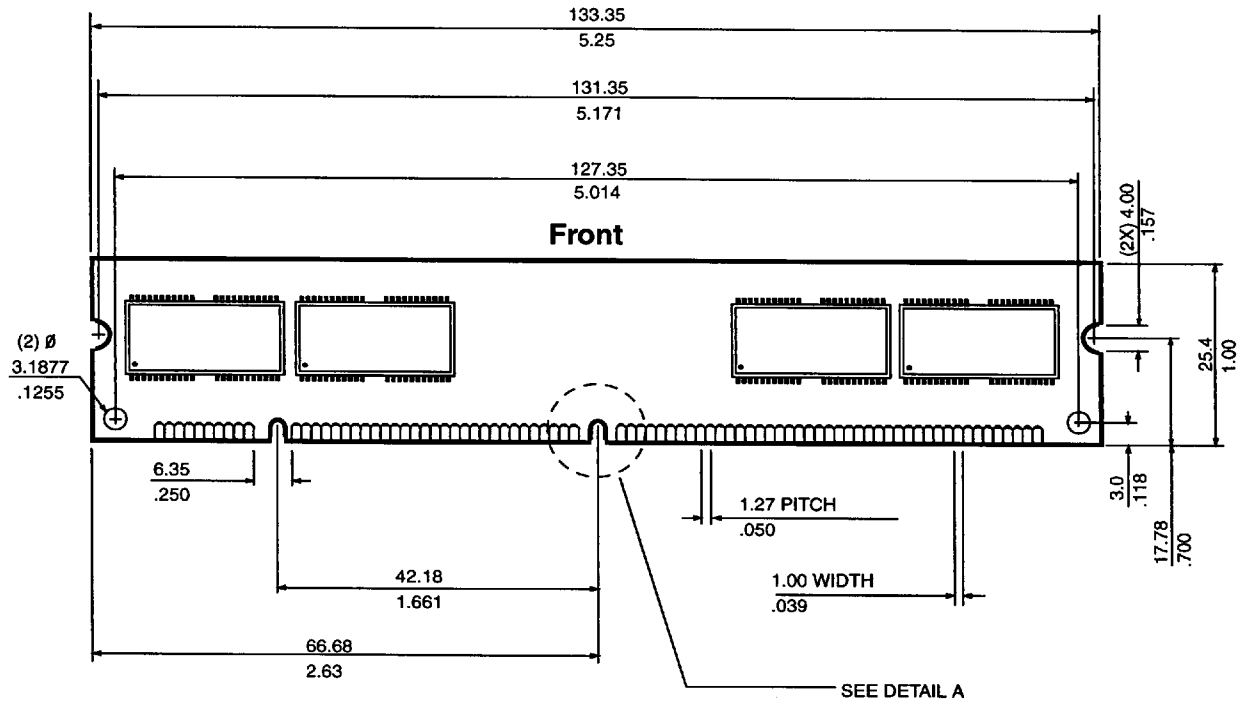
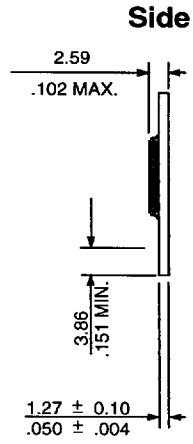


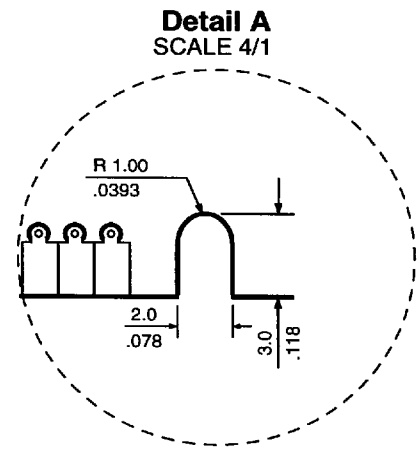
Figure 3. Acknowledge Response From Receiver



Layout Drawing (x64 TSOP)

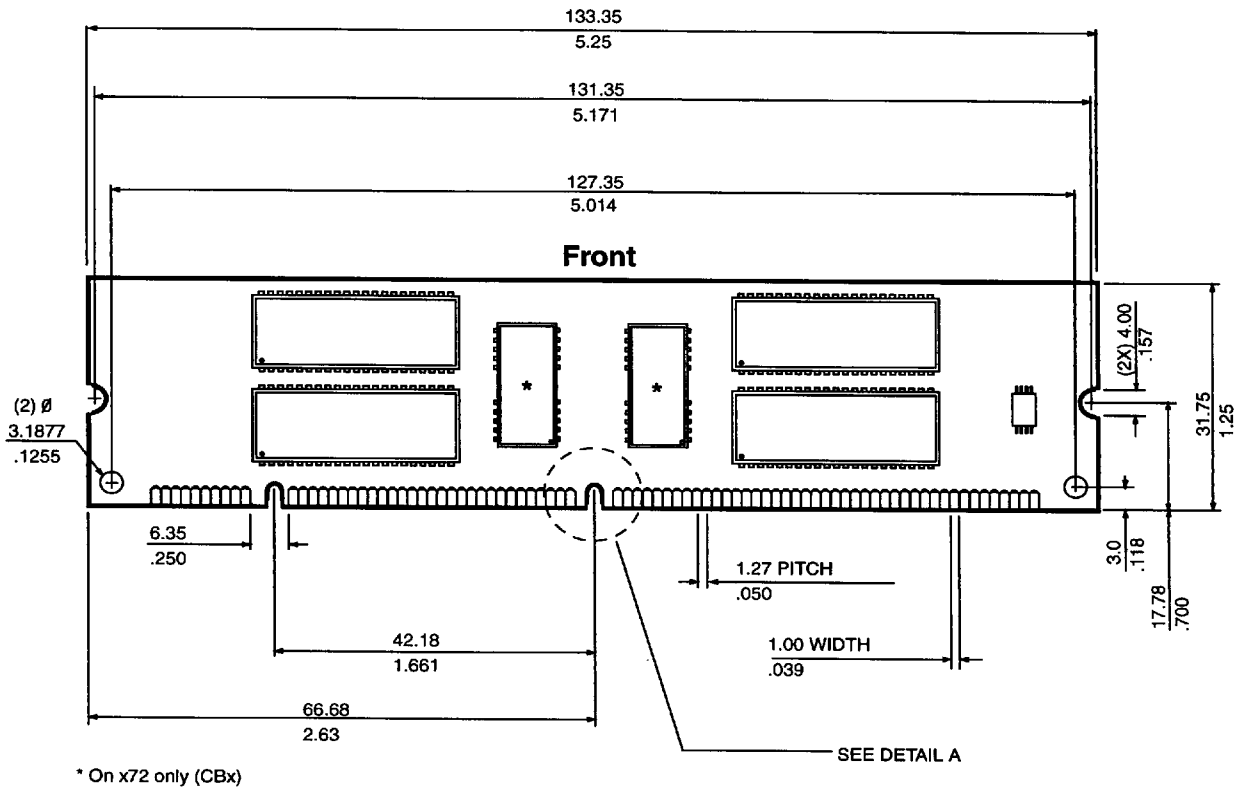


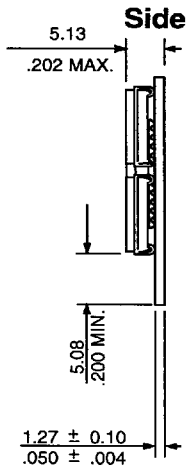


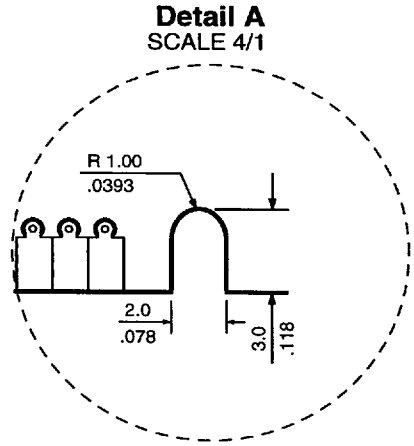


Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Layout Drawing (x64/x72 SOJ)







Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Revision Log

Rev	Contents of Modification
1/96	Initial Release.
5/96	Updated ordering information Added SOJ versions Added 6Rns speed sort Updated capacitance Updated Presence Detect table Updated I_{CC2}, I_{CC5}, I_{OUT} Improved timings t_{CAH}, t_{CDD}, t_{OEZ}, t_{OFF}, PD timings CBR timing diagram was changed to allow $\overline{CAS}$ to remain low for back-to-back CBR cycles. Hidden Refresh Cycle (Read) timing diagram was changed to show data being turned off with $\overline{RAS}$ not $\overline{CAS}$
8/96	Fixed typos