



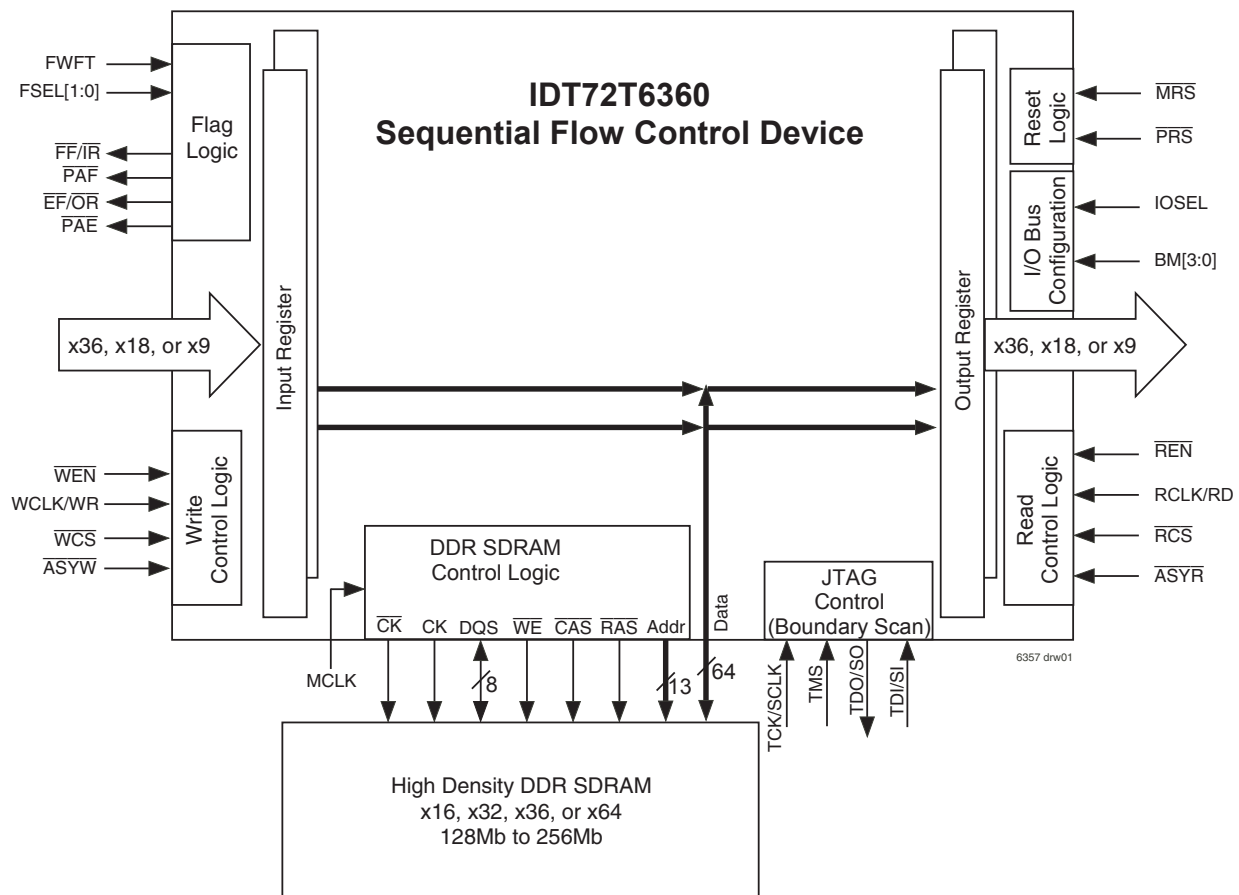
2.5V SEQUENTIAL FLOW-CONTROL DEVICE  
36 BIT WIDE CONFIGURATION  
For use with 128Mb to 256Mb DDR SDRAM

ADVANCE INFORMATION  
IDT72T6360

### FEATURES

- Product to be used with single or multiple external DDR SDRAM to provide significant storage capability of up to 1Gb density
- 166MHz operation (6ns read/write cycle time)
- User selectable input and output port bus-sizing
  - x36in to x36out
  - x36in to x18out
  - x36in to x9out
  - x18in to x36out
  - x18in to x18out
  - x18in to x9out
  - x9in to x36out
  - x9in to x18out
  - x9in to x9out
- For other bus configurations see IDT72T6480 (x12, x24, or x48)
- 2.5V-LVTTL or 3.3V-LVTTL independently configured ports
- Independent and simultaneous read and write access
- User selectable synchronous/asynchronous read and write port timing
- IDT Standard mode or FWFT mode of operation
- Empty and full flags for monitoring memory status
- Programmable Almost-Empty and Almost-Full flags, each flag can default to one of four preselected offsets or serially programmed to a specific value
- Selectable synchronous/asynchronous timing modes for Almost-Empty and Almost-Full flags
- Master Reset clears all data and settings
- Partial Reset clears data, but retains programmable settings
- Depth expandable with multiple devices for densities greater than 1Gb
- Width expandable with multiple devices for bus widths greater than 36 bits
- JTAG functionality (Boundary Scan)
- Available in a 324-pin PBGA, 1mm pitch, 19mm x 19mm
- HIGH performance 0.18µm CMOS technology
- Industrial temperature range (-40°C to +85°C) is available
- Supports industry standard DDR specifications, including Samsung, Micron, and Infineon memories

### FUNCTIONAL BLOCK DIAGRAM



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## DESCRIPTION

The IDT72T6360 sequential flow-control device is a device incorporating a seamless connection to external DDR SDRAM for significant storage capacity supporting high-speed applications. Both read and write ports of the sequential flow-control can operate independently at up to 166MHz. There is a user selectable correction feature that will correct any erroneous single data bit when reading from the SDRAM.

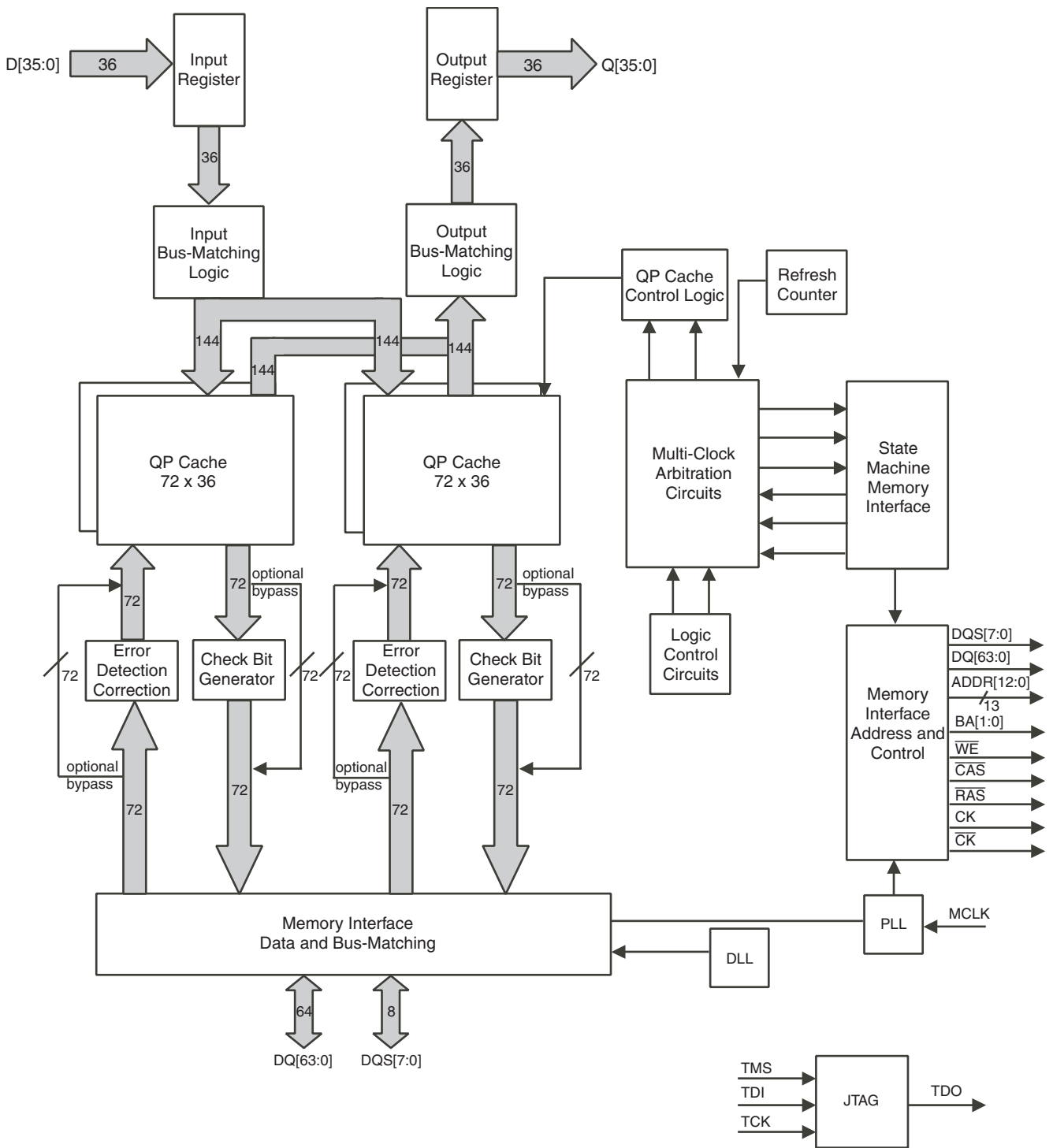
The independent read and write ports each has associated read and write clocks, enables, and chip selects. Both ports can operate either synchronously or asynchronously. Other features include bus-matching, programmable status flags with selectable synchronous/asynchronous timing modes, IDT Standard or FWFT mode timing, and JTAG boundary scan functionality.

The bus-matching feature will allow the inputs and outputs to be configured to x36, x18, or x9 bus width. There are four default offset values available

for the programmable flags ( $\overline{PAE}/\overline{PAF}$ ), as well as the option of serially programming the offsets to a specific value.

The device package is 19mm x 19mm 324-pin PBGA. It operates at a 2.5V core voltage with selectable 2.5V or 3.3V I/Os. The I/O interface to the SDRAM will be 2.5V SSTL only and not 3.3V tolerant. Both industrial and commercial temperature ranges will be offered.

The sequential flow-control device controls individual DDR SDRAM of either 128Mb or 256Mb. The device will support industry standard DDR specification memories (note DDR II is not supported), which include vendors such as Samsung, Micron, and Infineon. The data bus connected to the DDR SDRAM can be 16-bit, 32-bit, or 64-bits wide. The sequential flow-control device can independently control up to four separate external memories for a maximum of density of 1Gb (128MB). Depth expansion mode is available for applications that require more than 1Gb of storage memory.



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Figure 1. Sequential Flow-Control Device Block Diagram

# PIN CONFIGURATION

A1 BALL PAD CORNER

A	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○		
	GND	GND	DQ10	DQ8	DQ4	DQ1	$\overline{CK}$	A1	A5	A9	$\overline{WE}$	$\overline{RAS}$	DQ35	DQ36	DQ38	DQ40	GND	GND	
B	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
	GND	GND	DQS1	DQ9	DQ5	DQ2	AVCC	A0	A4	A10	BA1	DQ32	DQS4	DQ39	DQ44	DQS5	GND	GND	
C	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
	DQ14	DQ13	DQ11	DQ12	DQ6	DQ3	CK	A2	A6	A11	BA0	DQ34	DQ37	DQ41	DQ47	DQ45	DQ49	DQ50	
D	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
	DQ16	DQ15	DQ17	DQ7	DQS0	DQ0	AVCC	A3	A7	A8	A12	$\overline{CAS}$	DQ33	DQ43	DQ46	VREF	DQ51	DQS6	
E	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
	DQ19	DQ18	DQS2	DQ20	DQ21	AGND	AGND	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	DQ42	DQ54	DQ48	DQ52	DQ53
F	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	DQ23	DQ22	DQ24	DQ25	DQ26	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	DQ59	DQ58	DQ55	DQ56	DQ57
G	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	DQS3	DQ27	DQ28	DQ29	DQ30	Vcc	Vcc	GND	GND	GND	GND	Vcc	Vcc	Vcc	DQ62	DQ61	DQS7	DQ60	
H	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	MCLK	DQ31	D0	D1	D2	Vcc	GND	GND	GND	GND	GND	GND	VDDQ	VDDQ	Q2	Q1	DQ63	Q0	
J	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	D4	D3	D5	D6	D7	Vcc	GND	GND	GND	GND	GND	GND	VDDQ	VDDQ	Q6	Q5	Q3	Q4	
K	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	D11	D12	D10	D9	D8	Vcc	GND	GND	GND	GND	GND	GND	VDDQ	VDDQ	Q7	Q12	Q8	Q9	
L	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	D16	D17	D15	D14	D13	Vcc	Vcc	GND	GND	GND	GND	GND	VDDQ	VDDQ	Q13	Q11	Q10	Q14	
M	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	D21	D22	D20	D19	D18	Vcc	Vcc	Vcc	GND	GND	GND	VDDQ	VDDQ	VDDQ	Q28	Q15	Q16	Q17	
N	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	D26	D27	D25	D24	D23	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	VDDQ	VDDQ	Q23	Q29	Q19	Q20	Q18	
P	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	D31	D32	D30	D29	D28	FSEL1	IOSEL	GND	BM3	MIC0	JSEL	TDO/SO	DNC	Q32	Q33	Q31	Q25	Q21	
R	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	D34	D35	D33	Vcc	Vcc	FSEL0	IDEM	MTYPE0	BM2	MIC1	TDI/SI	FF/ IR	DNC	DNC	Q34	Q30	Q26	Q22	
T	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	Vcc	Vcc	Vcc	Vcc	Vcc	$\overline{ASYW}$	WCS	MSPEED	BM1	TMS	$\overline{SWEN}$	PAF	DNC	DNC	Q35	DNC	Q27	Q24	
U	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	GND	GND	Vcc	Vcc	Vcc	$\overline{PRS}$	FWFT	MTYPE1	BM0	MIC2	TCK/ SCLK	$\overline{OE}$	$\overline{PAE}$	DNC	DNC	DNC	GND	GND	
V	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	GND	GND	Vcc	Vcc	MRS	$\overline{ASYR}$	WEN	WCLK	RCLK	REN	SREN	RCS	$\overline{EF/}$ $\overline{OR}$	DNC	DNC	DNC	GND	GND	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

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PBGA (BB324-1, order code: BB)  
 TOP VIEW

## PIN DESCRIPTIONS

Symbol	Pin No. Location	Name	I/O TYPE	Description
A[12:0]	See Pin No. table	Memory Address Bus	OUTPUT	Output address bus to be connected to the input address bus of the external memory to provide row and column address.
ASYR <sup>(1)</sup>	V6	Asynchronous Read Port	INPUT	A HIGH on this input during master reset will select synchronous read operation for the output port. A LOW will select asynchronous operation. If asynchronous is selected the device must operate in IDT Standard mode and the read enable must be tied to GND.
ASYW <sup>(1)</sup>	T6	Asynchronous Write Port	INPUT	A HIGH on this input during master reset will select synchronous write operation for the input port. A LOW will select asynchronous operation. If asynchronous is selected the device must operate in IDT Standard mode and the write enable must be tied to GND.
BA[1:0]	BA1-B11 BA0-C11	Memory Bank Address Input Bit	OUTPUT	Address bits to be connected to the external memory's BA inputs to determine which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
BM[3:0] <sup>(1)</sup>	See Pin tbl.	Bus-Matching Bit	INPUT	Selects the bus width of the read and write ports.
CK	C7	Memory Clock	OUTPUT	Clock output to be connected to the external memory's input clock.
$\overline{CK}$	A7	Memory Clock Inverted	OUTPUT	Differential clock output to be connected to the external memory's differential input clock.
$\overline{CAS}$	D12	Memory Column Address Strobe	OUTPUT	Output enable signal to be connected to the external memory's $\overline{CAS}$ pin to activate and deactivate the column address strobe.
D[35:0]	See Pin tbl.	Data Inputs	INPUT	Data inputs for a 36, 18, and 9-bit bus.
DQ[63:0]	See Pin No. table	Memory Data Bus	Bi-Directional	Input/output data bus for the external memory's data bus.
DQS[7:0]	See Pin No. table	Memory Data Strobe	Bi-Directional	Input/output data strobe to be connected to the external memory's data strobe.
$\overline{EF}/\overline{OR}$	V13	Empty Flag/ Output Ready	OUTPUT	In IDT Standard mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the device memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether or not there is valid data available at the outputs.
$\overline{FF}/\overline{IR}$	R12	Full Flag/Input Ready	OUTPUT	In IDT Standard mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the device memory is full. In FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether or not there is space available for writing to the device memory.
FSEL[1:0] <sup>(1)</sup>	FSEL1-P6 FSEL0-R6	Flag Select Bit	INPUT	During master reset, these inputs will select one of four default values for the programmable flags PAE and PAF. The selected value will apply to both PAE and PAF offset.
FWFT <sup>(1)</sup>	U7	First Word Fall Through	INPUT	During master reset, a HIGH on this input selects FWFT timing mode. A LOW selects IDT Standard timing mode.
IDEM <sup>(1)</sup>	R7	IDT Standard Mode Depth Expansion Mode Select	INPUT	This select pin is used for depth expansion configuration in IDT Standard mode. If this pin is tied HIGH, then the $\overline{FF}/\overline{IR}$ signal will be inverted to provide a seamless depth expansion interface. If this pin is tied LOW, the depth expansion in IDT Standard mode will be deactivated.
IOSEL <sup>(1)</sup>	P7	I/O VDDQ Select	INPUT	This input determines whether the inputs and outputs will tolerate a 2.5V or 3.3V voltage signals. If IOSEL is HIGH, then all I/Os will be 2.5V tolerant. If IOSEL is LOW, then all I/Os will be 3.3V tolerant.
JSEL <sup>(1)</sup>	P11	JTAG Select	INPUT	This pin selects whether the JTAG pins will be used for serial programming. If JSEL is HIGH, the JTAG pins will only be used for JTAG boundary-scan function. If JSEL is LOW, the JTAG function is disabled and the JTAG pins will be used for serial programming of the PAE/PAF offset registers.
MIC[2:0] <sup>(1)</sup>	MIC2-U10 MIC1-R10 MIC0-P10	Memory Configuration	INPUT	These signals enable the EDC feature of the device. See Table 6, Error Detection and Correction Configuration (EDC) for all possible configurations.
MCLK	H1	Master Clock	INPUT	33MHz reference clock used to generate CK and $\overline{CK}$ for external memory interface.
$\overline{MRS}$	V5	Master Reset	INPUT	Master reset initializes the read and write pointers to zero and sets the output register to all zeros. All initialized settings for the device will be configured during master reset.



## PIN DESCRIPTIONS (CONTINUED)

Symbol	Pin No. Location	Name	I/O TYPE	Description
MSPEED <sup>(1)</sup>	T8	Memory Speed	INPUT	This input select the speed of the external memory interfacing the sequential flow-control device. A LOW selects 133MHz, and HIGH selects 166MHz.
MTYPE <sup>(1)</sup> [1:0]	MTYPE1-U8 MTYPE0-R8	Memory Type [1:0]	INPUT	These inputs select which type of external memory is interfacing the sequential flow-control device. See Table 10 for the list of selectable memories.
$\overline{OE}$	U12	Output Enable	INPUT	Asynchronous three-state control of the data outputs. All data outputs Q[35:0] will be placed in high-impedance if this pin is HIGH. Conversely, all data outputs will be active when this pin is LOW.
$\overline{PAE}$	U13	Programmable Almost Empty Flag	OUTPUT	This is the programmable almost empty flag that can be used as an early indicator for the empty boundary condition of the internal memory. $\overline{PAE}$ goes LOW if the number of words in the sequential flow-control device is less than offset n, which is stored in the empty offset register. $\overline{PAE}$ goes HIGH if the number of words in the sequential flow-control device is greater than or equal to the offset n.
$\overline{PAF}$	T12	Programmable Almost Full Flag	OUTPUT	This is the programmable almost full flag that can be used as an early indicator for the full boundary condition of the internal memory. $\overline{PAF}$ goes HIGH if the number of free locations in the sequential flow-control device is more than offset m, which is stored in the full offset register. $\overline{PAF}$ goes LOW if the number of free locations in the sequential flow-control device is less than or equal to the offset m.
$\overline{PRS}$	U6	Partial Reset	INPUT	Partial reset initializes the read and write pointers to zero and sets the output registers to all zeros. All existing configurations in the sequential flow-control device will not be affected. This includes the IDT Standard or FWFT mode timing, programmable flag settings, and bus width and data rate mode.
Q[35:0]	See Pin tbl.	Data Output Bus	OUTPUT	Data outputs for a 36, 18, and 9-bit bus.
$\overline{RAS}$	A12	Memory Row Address Strobe	OUTPUT	Output strobe signal to be connected to the external memory's $\overline{RAS}$ pin to activate and deactivate the row address strobe.
RCLK/ RD	V9	Read Clock/ Read Strobe	INPUT	This is a dual function pin. If synchronous operation of the read port is selected, the rising edge of RCLK reads data from the sequential flow-control device when $\overline{REN}$ is enabled. If asynchronous operation of the read port is selected, a rising edge on RD reads data from the sequential flow-control device without the need of a free-running input read clock.
$\overline{RCS}$	V12	Read Chip Select	INPUT	Synchronous three-state control of the data outputs. Provides another means of controlling the data outputs synchronous to RCLK. Can be regarded as a second output enable signal.
$\overline{REN}$	V10	Read Enable	INPUT	$\overline{REN}$ enables RCLK for reading data from the sequential flow-control device. If asynchronous mode is selected on the read port, this signal should be tied to GND.
$\overline{SREN}$	V11	Serial Read Enable	INPUT	When $\overline{SREN}$ is brought LOW before the rising edge of SCLK, the contents of the $\overline{PAE}$ and $\overline{PAF}$ offset registers are copied to a serial shift register. While $\overline{SREN}$ is maintained LOW, on each rising edge of SCLK, one bit of data is shifted out of this serial shift register through the SDO output pin.
$\overline{SWEN}$	T11	Serial Write Enable	INPUT	On each rising edge of SCLK when $\overline{SWEN}$ is LOW, data from the FWFT pin is serially loaded into the $\overline{PAE}$ and $\overline{PAF}$ registers.
TCK/ SCLK	U11	JTAG Clock/ Serial Clock	INPUT	This is a dual function pin. When the JSEL pin is HIGH, this is the clock input for JTAG boundary-scan function. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data from TMS and TDI are sampled on the rising edge of TCK and outputs change on the falling edge of TCK. When the JSEL pin is LOW, this is the serial clock input for writing and reading the $\overline{PAE}$ / $\overline{PAF}$ offset registers. On the rising edge of every SCLK when $\overline{SWEN}$ is LOW, one bit of data from the SI pin is shifted into the $\overline{PAE}$ and $\overline{PAF}$ offset registers. On the rising edge of each SCLK when $\overline{SREN}$ is LOW, one bit of data from the SO pin is shifted out of the $\overline{PAE}$ and $\overline{PAF}$ offset registers. If the JTAG or serial programming is not used this signal needs to be tied to GND.



## PIN DESCRIPTIONS (CONTINUED)

Symbol	Pin No. Location	Name	I/O TYPE	Description
TDI/SI	R11	JTAG Test Data Input/ Serial Input	INPUT	This is a dual function pin. When the JSEL pin is HIGH, this is the JTAG test data input pin. One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded via the TDI on the rising edge of TCK to the Instruction Register, ID Register and Bypass Register. When the JSEL pin is LOW, this is the serial input pin for the $\overline{\text{PAE}}/\overline{\text{PAF}}$ offset registers. An internal pull-up resistor forces TDI/SI HIGH if left unconnected.
TDO/SO	P12	JTAG Test Data Output/ Serial Output	OUTPUT	This is a dual function pin. When the JSEL pin is HIGH, this is the JTAG test data output pin. One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded output via the TDO on the falling edge of TCK from either the Instruction Register, ID Register and Bypass Register. This output is high-impedance except when shifting, while in SHIFT-DR and SHIFT-IR controller states. When the JSEL pin is LOW, this is the serial data output pin for the $\overline{\text{PAE}}/\overline{\text{PAF}}$ offset registers.
TMS	T10	JTAG Mode Select	INPUT	TMS is a serial input pin. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pull-up resistor forces TMS HIGH if left unconnected.
WCLK/WR	V8	Write Clock/Write Strobe	INPUT	This is a dual function pin. If synchronous operation of the write port is selected, the rising edge of WCLK writes data into the sequential flow-control device when $\overline{\text{WEN}}$ is enabled. If asynchronous operation of the write port is selected, a rising edge on WR writes data into the sequential flow-control device without the need of a free-running input write clock.
$\overline{\text{WCS}}$	T7	Write Chip Select	INPUT	Synchronous three-state control of the data inputs. Provides a means of controlling the data inputs synchronous to WCLK. Typically used to avoid bus-contention when multiple devices are sharing the same input data bus.
$\overline{\text{WE}}$	A11	Memory Write Enable	OUTPUT	Output strobe signal to be connected to the external memory's $\overline{\text{WE}}$ pin to activate and deactivate the write address strobe.
$\overline{\text{WEN}}$	V7	Write Enable	INPUT	$\overline{\text{WEN}}$ enables WCLK for writing data into the sequential flow-control device. If asynchronous mode is selected on the write port, this signal should be tied to GND.
Vcc	See Pin No. table	Core Vcc and Output voltage for DDR SDRAM	Power	The core power supply pins for the device as well as to the external DDR SDRAM. Needs to be connected to a +2.5V Vcc power plane.
AVcc	B7, D7	Internal PLL Vcc	Power	The power supply pins for the internal PLL of the device. Needs to be connected to a +2.5V supply rail.
VDDQ	See Pin No. table	Output rail voltage for I/Os	Power	This pin is used to provide power to the output drivers. The nominal values are 2.5V or 3.3V, depending on the state of the IOSEL pin.
VREF	D16	Reference Voltage	Power	This is a voltage reference input to the SDRAM and must be connected to Vcc/2 or 1.25V.
GND	See Pin table	Ground Pin	Ground	The ground pins for the device that must be connected to the ground plane.
AGND	E6, E7	Ground pin for analog circuit	Ground	The ground pins for the analog circuitry in the device that must be connected to the ground plane.

**NOTE:**

1. These pins should not change after master reset.

*Please see next page for Pin Number Location Table*

## PIN NUMBER LOCATION TABLE

Symbol	Name	I/O TYPE	Pin Number
A[12:0]	Memory Address Bus	OUTPUT	A12-D11, A11-C10, A10-B11, A9-A10, A8-D10, A7-D9, A6-C9, A5-A9, A4-B9, A3-D8, A2-C8, A1-A8, A0-B8
BM[3:0]	Bus-Matching	INPUT	BM3-P9, BM2-R9, BM1-T9, BM0-U9
D[35:0]	Data Inputs	INPUT	D35-R2, D34-R1, D33-R3, D32-P2, D31-P1, D30-P3, D29-P4, D28-P5, D27-N2, D26-N1, D25-N3, D24-N4, D23-N5, D22-M2, D21-M1, D20-M3, D19-M4, D18-M5, D17-L2, D16-L1, D15-L3, D14-L4, D13-L5, D12-K2, D11-K1, D10-K3, D9-K4, D8-K5, D7-J5, D6-J4, D5-J3, D4-J1, D3-J2, D2-H5, D1-H4, D0-H3
DQ[63:0]	Memory Data Bus	Bi-Directional	DQ63-H17, DQ62-G15, DQ61-G16, DQ60-G18, DQ59-F14, DQ58-F15, DQ57-F18, DQ56-F17, DQ55-F16, DQ54-E15, DQ53-E18, DQ52-E17, DQ51-D17, DQ50-C18, DQ49-C17, DQ48-E16, DQ47-C15, DQ46-D15, DQ45-C16, DQ44-B15, DQ43-D14, DQ42-E14, DQ41-C14, DQ40-A16, DQ39-B14, DQ38-A15, DQ37-C13, DQ36-A14, DQ35-A13, DQ34-C12, DQ33-D13, DQ32-B12, DQ31-H2, DQ30-G5, DQ29-G4, DQ28-G3, DQ27-G2, DQ26-F5, DQ25-F4, DQ24-F3, DQ23-F1, DQ22-F2, DQ21-E5, DQ20-E4, DQ19-E1, DQ18-E2, DQ17-D3, DQ16-D1, DQ15-D2, DQ14-C1, DQ13-C2, DQ12-C4, DQ11-C3, DQ10-A3, DQ9-B4, DQ8-A4, DQ7-D4, DQ6-C5, DQ5-B5, DQ4-A5, DQ3-C6, DQ2-B6, DQ1-A6, DQ0-D6,
DQS[7:0]	Memory Data Strobe	Bi-Directional	DQS7-G17, DQS6-D18, DQS5-B16, DQS4-B13, DQS3-G1, DQS2-E3, DQS1-B3, DQS0-D5
Q[35:0]	Data Output Bus	Output	Q35-T15, Q34-R15, Q33-P15, Q32-P14, Q31-P16, Q30-R16, Q29-N15, Q28-M15, Q27-T17, Q26-R17, Q25-P17, Q24-T18, Q23-N14, Q22-R18, Q21-P18, Q20-N17, Q19-N16, Q18-N18, Q17-M18, Q16-M17, Q15-M16, Q14-L18, Q13-L15, Q12-K16, Q11-L16, Q10-L17, Q9-K18, Q8-K17, Q7-K15, Q6-J15, Q5-J16, Q4-J18, Q3-J17, Q2-H15, Q1-H16, Q0-H18
Vcc	Core Vcc & Output voltage for DDR SDRAM	Power	E(8-13), F(6-13), G(6,7,12-14), H6, J6, K6, L(6,7), M(6-8), N(6-11), R(4,5), T(1-5), U(3-5), V(3,4)
VDDQ	Output rail voltage for I/Os	Power	H(13,14), J(13,14), K(13,14), L(13,14), M(12-14), N(12,13)
GND	Ground Pin	Ground	G(8-11), H(7-12), J(7-12), K(7-12), L(8-12), M(9-11), P8
DNC	Do Not Connect	—	P13, R(13,14), T(13,14,16), U(14-16), V(14-16)

## DETAILED DESCRIPTIONS

### SEQUENTIAL FLOW-CONTROL STRUCTURE

The IDT sequential flow-control (SFC) device is comprised of three interfaces: input port, output port, and memory interface. The input and output port can operate independently of each other with selectable bus widths of x9, x18, or x36 bits wide. The third interface, or memory interface, is connected directly to an external memory, which can be used to offload data entering the SFC device.

### WRITING AND READING FROM THE SEQUENTIAL FLOW-CONTROL DEVICE

Writing into the SFC device is accomplished by setting the write enable signal ( $\overline{WEN}$ ) and write chip select ( $\overline{WCS}$ ) low with a free running write clock ( $WCLK$ ). Data will be written on the rising edge of every  $WCLK$  into the Quad-Port (QP) cache of the SFC device. The internal state machine of the device will determine whether to send the data to the DDR SDRAM or send it directly through to the output bus, depending on when the data is to be accessed. This provides “data coherency” and minimizes the path that the data has to travel.

Reading from the SFC device is accomplished by setting the read enable signal ( $\overline{REN}$ ) and read chip select ( $\overline{RCS}$ ) low with a free running read clock ( $RCLK$ ). Data will be sent to the output bus on the rising edge of every  $RCLK$ . This data will be accessed either from the QP cache or the external DDR SDRAM.

### EXTERNAL MEMORY SELECTION

The DDR SDRAM interface of the SFC device can support DDR SDRAM with standard DDR I specifications. The SFC device can support any external memory within the following characteristics:

- Bus width: 16-bit or 32-bit wide
- Speed: 133MHz or 166MHz
- Density: 128Mb or 256Mb

Table 1 lists the DDR SDRAM specifications that are required to meet the sequential flow-control device requirements. Table 2 lists the memory vendors and associated part numbers of DDR SDRAMs that have been validated by IDT to meet the requirements for the DDR SDRAM interface.

**TABLE 1 – DDR SDRAM SPECIFICATIONS**

DDR SDRAM Bus-Width	DDR SDRAM Specifications							Units
	CL	$t_{RCWD}$	$t_{WR}$	$t_{RCDR}$	$t_{RP}$	$t_{RFC}$	$t_{WR} + t_{RP}$	
16-bit	2.5	3	3	3	3	12	6	ns
32-bit	3	2	3	4	4	14	7	ns

**TABLE 2 – SUPPORTED MEMORY VENDORS**

Density	Bus Width	Vendor	Part#
128Mb	16	Samsung	K4M281638E-TCLB3 K4M281638E-TCLA2
128Mb	16	Micron	MT46V8M16TG-6T MT46V8M16TG-75
128Mb	16	Infineon	HYB25D128160ATL-6 HYB25D128160ATL-7
128Mb	32	Samsung	K4D263238E-GC45
256Mb	16	Samsung	K4H561638F-TCLB3 K4H561638F-GCLB3
256Mb	16	Micron	MT46V16M16TG-6T MT46V16M16TG-75
256Mb	16	Infineon	HYB25D256160BTL-6 HYB25D256160BTL-7
256Mb	32	Samsung	K4D553238E-JC50

### EXTERNAL MEMORY CONFIGURATIONS

The DDR SDRAM interface of the sequential flow-control (SFC) device has a 64-bit output data bus that provides up to four (16-bit SDRAM) external DDR SDRAM connections. For multiple memory connections, they must be of the same density configuration and speed grade. For example, two device connected cannot consist of one 128Mb and one 256Mb memory nor two 128Mb with one at 133MHz and the other at 166MHz. Below is a summary of the possible configurations:

- One 16-bit device connecting a x16 interface to the DDR SDRAM
- One 32-bit device connecting a x32 interface to the DDR SDRAM

- Two 16-bit devices connecting a x32 interface to the DDR SDRAM
- Two 32-bit devices connecting a x36 interface to the DDR SDRAM
- Two 32-bit devices connecting a x64 interface to the DDR SDRAM
- Three 16-bit devices connecting a x36 interface to the DDR SDRAM
- Four 16-bit devices connecting a x64 interface to the DDR SDRAM

These various configurations determine the storage density of the SFC device. The storage density can range from a minimum of 128Mb to a maximum of 1Gb. Table 3 lists the possible ways to connect the DDR SDRAMs and the number of chipset solutions to obtain the various storage densities.

**TABLE 3 – TOTAL POSSIBLE EXTERNAL MEMORY CONFIGURATIONS**

Two Chip Solution <sup>(1)</sup>	Three Chip Solution <sup>(1)</sup>	Four Chip Solution <sup>(1)</sup>	Five Chip Solution <sup>(1)</sup>
<sup>(2)</sup> Configuration 1, 2	<sup>(2)</sup> Configurations 3, 4, 5	<sup>(2)</sup> Configuration 6	<sup>(2)</sup> Configuration 7
1 x 128Mb [4M x 32] Total memory: 128Mb	2 x 128Mb [4M x 32] Total memory: 256Mb	N/A	N/A
1 x 256Mb [8M x 32] Total memory: 256Mb	2 x 256Mb [8M x 32] Total memory: 512Mb	N/A	N/A
1 x 128Mb [8M x 16] Total memory: 128Mb	2 x 128Mb [8M x 16] Total memory: 256Mb	3 x 128Mb [8M x 16] Total memory: 384Mb	4 x 128Mb [8M x 16] Total memory: 512Mb
1 x 256Mb [16M x 16] Total memory: 256Mb	2 x 256Mb [16M x 16] Total memory: 512Mb	3 x 256Mb [16M x 16] Total memory: 768Mb	4 x 256Mb [16M x 16] Total memory: 1Gb

**NOTES:**

1. The chip solution number includes the sequential flow-control device and external DDR SDRAM
2. See Figure 2a-2g for the 7 different configurations referenced in the table above.

Below are the various chipset solution configurations available to the sequential flow-control device (see Figure 2a-2g). The external memory interface is designed to seamlessly connect one or more DDR SDRAMs. There are a number of pins on the DDR SDRAM that requires the user to tie to a specified state, which are listed in Table 4.

**TABLE 4 – DDR SDRAM STATIC CONNECTIONS**

SDRAM Pin	Static Connections
CKE	VCC
$\overline{CS}$	GND
DM	GND

DDR SDRAM: 128Mb [4Mb x 32] or 256Mb [8Mb x 32]  
Total Density: 128Mb or 256Mb

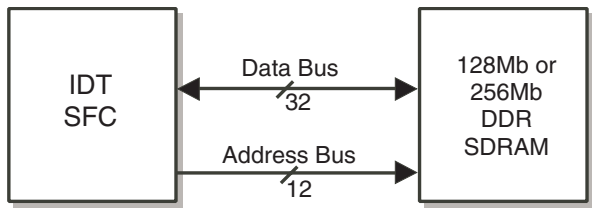


Figure 2a. Configuration 1 - Two Chip Solution

DDR SDRAM: 128Mb [8Mb x 16] or 256Mb [16Mb x 16]  
Total Density: 128Mb or 256Mb

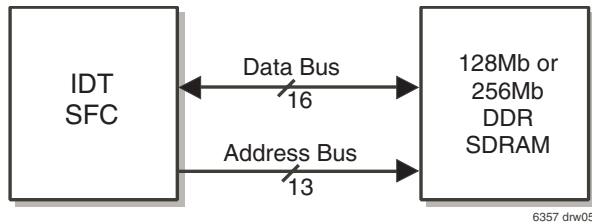


Figure 2b(1). Configuration 2 - Two Chip Solution

DDR SDRAM: 128Mb [4Mb x 32] or 256Mb [8Mb x 32]  
Total Density: 256Mb or 512Mb

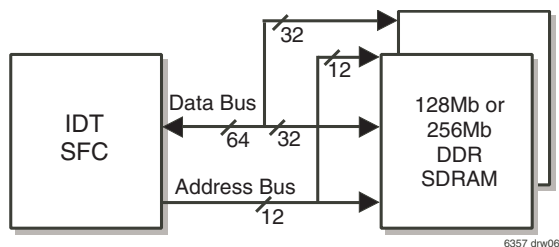


Figure 2c. Configuration 3 - Three Chip Solution

DDR SDRAM: 128Mb [4Mb x 32] or 256Mb [8Mb x 32]  
Total Density: 256Mb or 512Mb

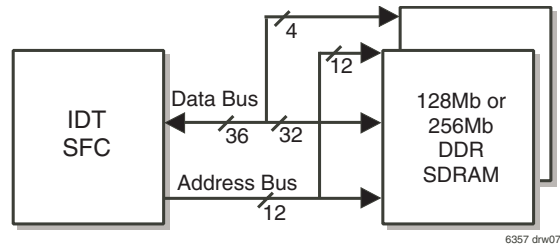


Figure 2d. Configuration 4 - Three Chip Solution

DDR SDRAM: 128Mb [8Mb x 16] or 256Mb [16Mb x 16]  
Total Density: 256Mb or 512Mb

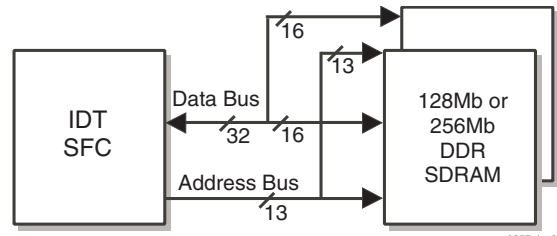


Figure 2e(1). Configuration 5 - Three Chip Solution

DDR SDRAM: 128Mb [8Mb x 16] or 256Mb [16Mb x 16]  
Total Density: 384Mb or 768Mb

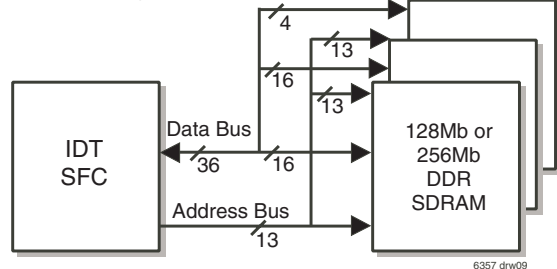


Figure 2f(1). Configuration 6 - Four Chip Solution

DDR SDRAM: 128Mb [8Mb x 16] or 256Mb [16Mb x 16]  
Total Density: 512Mb or 1Gb

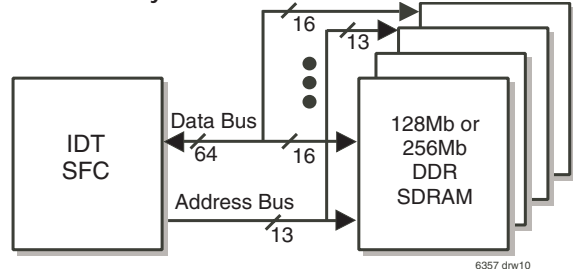


Figure 2g(1). Configuration 7 - Five Chip Solution

**NOTE:**

- 1. • 12-bit address bus for 8Mb x16
- 13-bit address bus for 16Mb x16

**MAXIMUM I/O OPERATING FREQUENCY**

The sequential flow-control (SFC) device is designed to operate at the maximum frequency of 166MHz. There are certain configurations however, that will limit the maximum frequency of the input and output ports. The main

factors that determine the usable memory are the I/O bus-width of the SFC, the density and number of DDR SDRAMs connected, and whether or not EDC is used. Table 5 lists the maximum frequency for the input and output ports of the SFC based on the various configurations.

**TABLE 5 –  
MAXIMUM I/O OPERATING FREQUENCY BASED ON VARIOUS CONFIGURATIONS**

SFC Bus-Width	DDR SDRAM Freq (MHz)	With EDC on or off	Configurations 3, 7	Configurations 4, 6	Configurations 1, 5	Configuration 2
x36	133.33	EDC on	100	66.67	50	33.33
		EDC off	133.33	83.33	66.67	33.33
	166.66	EDC on	133.33	83.33	66.67	33.33
		EDC off	166.67	100	83.33	50
x18	133.33	EDC on	166.67	133.33	100	66.67
		EDC off	166.67	166.67	133.33	83.33
	166.66	EDC on	166.67	166.67	133.33	83.33
		EDC off	166.67	166.67	166.67	166.67
x9	133.33	EDC on	166.67	166.67	166.67	133.33
		EDC off	166.67	166.67	166.67	166.67
	166.66	EDC on	166.67	166.67	166.67	166.67
		EDC off	166.67	166.67	166.67	166.67

**NOTE:**

1. See Figure 2a-2g for a list of all configurations.

**ERROR DETECTION AND CORRECTION**

The optional Error Detection and Correction (EDC) feature implemented in this device is used to ensure data integrity between the DDR SDRAM and the Sequential Flow Control (SFC) device. The EDC will correct single bit errors that are accessed from the DDR SDRAM. Multiple bit errors are not detected nor corrected. The EDC circuit uses a syndrome bit generator to generate 8 syndrome bits that will detect whether there are single bit errors in each data word.

The EDC is enabled using the MIC[2:0] pins. When the EDC is enabled, the dynamics of the total usable memory in the DDR SDRAM and SFC operating frequency will vary. Table 6 shows how to enable or disable the EDC feature for the various memory configurations.

**TABLE 6 – ERROR DETECTION AND CORRECTION CONFIGURATION**

External Pins	External Memory Characteristic							
	x64 off EDC	x64 on EDC	x36 off EDC	x36 on EDC	x32 off EDC	x32 on EDC	x16 off EDC	x16 on EDC
MIC0	1	1	0	0	0	0	1	1
MIC1	1	0	1	0	0	1	0	1
MIC2	1	1	1	1	0	0	0	0

**CONNECTING THE DDR SDRAM**

The memory interface of the sequential flow-control device is designed for seamless connection to the DDR SDRAM. The output signal names should be connected directly to its corresponding input signal on the DDR SDRAM. There

are three signals on the DDR SDRAM that must be tied to a static state: CKE,  $\overline{CS}$ , and DM. Figure 3 and 4 are some examples of the memory interface connections for various density configurations. For information on DDR SDRAM layout recommendations, please see IDT application note AN-423.

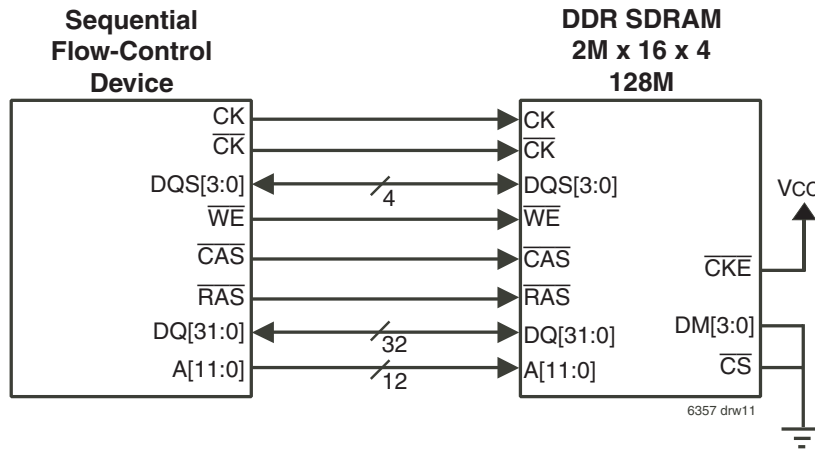


Figure 3. Memory Interface Connection (Single Chip)

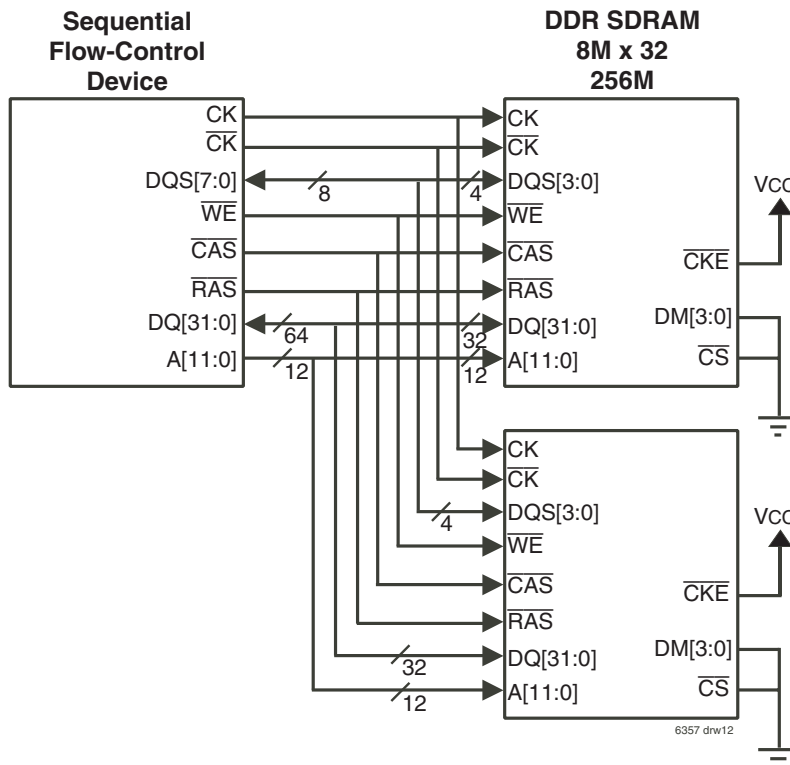


Figure 4. Memory Interface Connection (Two Chip)



**SETTING THE MEMORY INTERFACE SIGNALS**

The configurations listed in Figure 2a-2g can be programmed into the sequential flow-control device by using the MIC[2:0], MTYPE[1:0], and

MSPEED. For information about these signals, please refer to the Signal Description section. Table 7 is a list that shows the settings for the different configurations.

**TABLE 7 – MEMORY CONFIGURATIONS SETTINGS**

	MIC[2:0]	MTYPE[1:0]	MSPEED
<b>Configuration 1</b>	000 - EDC Off 010 - EDC On	00 - (4Mb x 32) 10 - (8Mb x 32)	0 - 133MHz 1 - 166MHz
<b>Configuration 2</b>	001 - EDC Off 011 - EDC On	01 - (8Mb x 16) 11 - (16Mb x 16)	0 - 133MHz 1 - 166MHz
<b>Configuration 3</b>	111 - EDC Off 101 - EDC On	00 - (4Mb x 32) 10 - (8Mb x 32)	0 - 133MHz 1 - 166MHz
<b>Configuration 4</b>	110 - EDC Off 100 - EDC On	00 - (4Mb x 32) 10 - (8Mb x 32)	0 - 133MHz 1 - 166MHz
<b>Configuration 5</b>	000 - EDC Off 010 - EDC On	01 - (8Mb x 16) 11 - (16Mb x 16)	0 - 133MHz 1 - 166MHz
<b>Configuration 6</b>	110 - EDC Off 100 - EDC On	01 - (8Mb x 16) 11 - (16Mb x 16)	0 - 133MHz 1 - 166MHz
<b>Configuration 7</b>	111 - EDC Off 101 - EDC On	01 - (8Mb x 16) 11 - (16Mb x 16)	0 - 133MHz 1 - 166MHz

**TABLE 8 – DEVICE CONFIGURATION**

Signal Pins	Static State	Configuration
ASYR	0	Read port configured in asynchronous mode
	1	Read port configured in synchronous mode
ASYW	0	Write port configured in asynchronous mode
	1	Write port configured in synchronous mode
BW[3:0]	—	See Table 11 - Bus-Matching Configurations
FSEL[1:0]	00	Programmable flag register offset value = 127
	01	Programmable flag register offset value = 1,023
	10	Programmable flag register offset value = 4,095
	11	Programmable flag register offset value = 16,383
FWFT	0	IDT Standard mode
	1	FWFT mode
IDEM	0	Depth expansion in FWFT mode
	1	Depth expansion in IDT Standard mode
IOSEL	0	I/O voltage set to 2.5V levels
	1	I/O voltage set to 3.3V levels
JSEL	0	JTAG function is disabled
	1	JTAG function is enabled
MIC[2:0]	—	See Table 6 - EDC Configuration for description
MSPEED	0	External memory interface clocks set to 133MHz
	1	External memory interface clocks set to 166MHz
MTYPE[1:0]	00	External memory configuration is: 4M x 32
	01	External memory configuration is: 8M x 32
	10	External memory configuration is: 8M x 16
	11	External memory configuration is: 16M x 16

**TABLE 9– DEFAULT PROGRAMMABLE FLAG OFFSETS**

FSEL1	FSEL0	Offset n,m
0	0	127
0	1	1,023
1	0	4,095
1	1	16,383

**TABLE 10– NUMBER OF BITS REQUIRED FOR OFFSET REGISTERS**

Write Port Bus-Width	x36		x18		x9	
	EDC On	EDC Off	EDC On	EDC Off	EDC On	EDC Off
Configuration 1 (128Mb)	21	22	22	23	23	24
Configuration 1 (256Mb)	22	23	23	24	24	25
Configuration 2 (128Mb)	21	22	22	23	23	24
Configuration 2 (256Mb)	22	23	23	24	24	25
Configuration 3 (256Mb)	22	23	23	24	24	25
Configuration 3 (512Mb)	23	24	24	25	25	26
Configuration 4 (256Mb)	22	22	23	23	24	24
Configuration 4 (512Mb)	23	23	24	24	25	25
Configuration 5 (256Mb)	22	23	23	24	24	25
Configuration 5 (512Mb)	23	24	24	25	25	26
Configuration 6 (384Mb)	23	23	24	24	25	25
Configuration 6 (768Mb)	24	24	25	25	26	26
Configuration 7 (512Mb)	23	24	24	25	25	26
Configuration 7 (1Gb)	24	25	25	26	26	27

**FUNCTIONAL DESCRIPTIONS**

**MASTER RESET AND DEVICE CONFIGURATION**

During master reset the sequential flow-control configuration and settings are determined, this includes the following:

1. Synchronous or Asynchronous read and write port operation
2. Bus-width configuration
3. Default offset register values
4. IDT standard or first word fall through (FWFT) timing mode
5. Depth expansion in IDT standard or FWFT mode
6. I/O voltage set to 2.5V or 3.3V levels
7. JTAG function enabled or disabled
8. Configuration of the external memory interface

The state of the configuration inputs during master reset will determine which of the above modes are selected. A master reset comprises of pulsing the MRS input pin from high to low for a period of time (trS) with the configuration inputs held in their respective states. Table 8 summarizes the configuration modes available during master reset. These signals are described in detail in the signal description section.

**PROGRAMMABLE ALMOST EMPTY/ALMOST FULL FLAGS**

The SFC has a set of programmable flags (PAE/PAF) that can be used as an early indicator for the empty and full boundary conditions. These flags have an offset value (n, m) that will determine the almost empty and almost full boundary conditions. There are four default offset values selectable during master reset, these values are shown in Table 9, Default Programmable Flag Offsets.

Offset values can also be programmed using the serial programming pins (SCLK, SI, and SWEN). The SFC has two internal offset registers that are used to store the specific offset value, one for the PAE and one for the PAF. The total number of bits (shown in Table 10, Number of Bits Required for Offset Registers) must be completely programmed to the offset registers. The serial programming sequence begins by writing data into the PAE register followed by the PAF register. See Figure 29, Serial Loading of Programmable Flag Registers for the associated timing diagram. The total number of bits required to program the offset registers will vary depending on the type of configuration that is shown in Figure 2a-2g, the bus-width selected, and whether EDC is used.

The values of n, m are used such that the PAE will become active (LOW) when there are at least one to n words written in the device. Similarly PAF will become active (LOW) when there are at least D – M words or more in the device, where D is the density of the SFC.

## SIGNAL DESCRIPTIONS

### INPUTS

#### DATA INPUTS (D0 - D35)

Data inputs for 36-bit wide data (D0 - D35), data inputs for 18-bit wide data (D0 - D17) or data inputs for 9-bit wide data (D0 - D8).

## CONTROLS

#### MASTER RESET ( $\overline{MRS}$ )

A Master Reset is accomplished whenever the  $\overline{MRS}$  input is toggled LOW then HIGH. This operation sets the internal read and write pointers to the first location of the RAM array.  $\overline{PAE}$  will go LOW,  $\overline{PAF}$  will go HIGH.

If FWFT is LOW during Master Reset then the IDT Standard mode, along with  $\overline{EF}$  and  $\overline{FF}$  are selected.  $\overline{EF}$  will go LOW and  $\overline{FF}$  will go HIGH. If FWFT is HIGH, then the First Word Fall Through mode (FWFT), along with  $\overline{IR}$  and  $\overline{OR}$ , are selected.  $\overline{OR}$  will go HIGH and  $\overline{IR}$  will go LOW.

All configuration control signals must be set prior to the LOW to HIGH transition of  $\overline{MRS}$ .

During a Master Reset, the output register is initialized to all zeroes. A Master Reset is required after power up, before a write operation can take place.  $\overline{MRS}$  is an asynchronous function.

See Figure 6, *Master Reset and Initialization*, for the relevant timing diagram.

#### PARTIAL RESET ( $\overline{PRS}$ )

A Partial Reset is accomplished whenever the  $\overline{PRS}$  input is toggled LOW then HIGH. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array,  $\overline{PAE}$  goes LOW, and  $\overline{PAF}$  goes HIGH.

Whichever mode is active at the time of Partial Reset, IDT Standard mode or First Word Fall Through, that mode will remain selected. If the IDT Standard mode is active, then  $\overline{FF}$  will go HIGH and  $\overline{EF}$  will go LOW. If the First Word Fall Through mode is active, then  $\overline{OR}$  will go HIGH, and  $\overline{IR}$  will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The programming method (parallel or serial) currently active at the time of Partial Reset is also retained. The output register is initialized to all zeroes.  $\overline{PRS}$  is asynchronous.

A Partial Reset is useful for resetting the device during the course of operation, when reprogramming programmable flag offset settings may not be convenient.

See Figure 7, *Partial Reset*, for the relevant timing diagram.

#### ASYNCHRONOUS WRITE ( $\overline{ASYW}$ )

The write port can be configured for either synchronous or asynchronous mode of operation. If during Master Reset the  $\overline{ASYW}$  input is LOW, then asynchronous operation of the write port will be selected. During asynchronous operation of the write port the WCLK input becomes WR input, this is the asynchronous write strobe input. A rising edge on WR will write data present on the data inputs into the sequential flow-control device (SFC). ( $\overline{WEN}$  must be LOW when using the write port in asynchronous mode).

When the write port is configured for asynchronous operation the device must be operating on IDT standard mode, FWFT mode is not permissible. The full flag ( $\overline{FF}$ ) and programmable almost full flag ( $\overline{PAF}$ ) operates in an asynchronous manner, that is, the full flag and  $\overline{PAF}$  flag will be updated based in both a write operation and read operation. Note, if asynchronous mode is selected, FWFT is not permissible. Refer to Figure 24, *Asynchronous Write and  $\overline{PAE}$  flag – IDT Standard mode* and Figure 25, *Asynchronous Write and  $\overline{PAF}$  flag – IDT Standard mode* for relevant timing and operational waveforms.

#### ASYNCHRONOUS READ ( $\overline{ASYR}$ )

The read port can be configured for either synchronous or asynchronous mode of operation. If during a Master Reset the  $\overline{ASYR}$  input is LOW, then asynchronous operation of the read port will be selected. During asynchronous operation of the read port the RCLK input becomes RD input, this is the asynchronous read strobe input. A rising edge on RD will read data from the SFC via the output register and data output port. ( $\overline{REN}$  must be tied LOW during asynchronous operation of the read port).

The  $\overline{OE}$  input provides three-state control of the Qn output bus, in an asynchronous manner.

When the read port is configured for asynchronous operation the device must be operating on IDT standard mode, FWFT mode is not permissible if the read port is asynchronous. The Empty Flag ( $\overline{EF}$ ) and programmable almost empty flag ( $\overline{PAE}$ ) operates in an asynchronous manner, that is, the empty flag and  $\overline{PAE}$  will be updated based on both a read operation and a write operation. Refer to Figure 23, *Asynchronous Read and  $\overline{PAE}$  flag – IDT Standard mode*, Figure 26, *Asynchronous Empty Boundary – IDT Standard mode*, Figure 27, *Asynchronous Full Boundary – IDT Standard mode*, and Figure 28, *Asynchronous Read and  $\overline{PAE}$  flag – IDT Standard mode*, for relevant timing and operational waveforms.

#### FIRST WORD FALL THROUGH (FWFT)

During Master Reset, the state of the FWFT input determines whether the device will operate in IDT standard mode or First Word Fall Through (FWFT) mode.

If, at the time of Master Reset, FWFT is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ( $\overline{EF}$ ) to indicate whether or not there are any words present in the SFC. It also uses the Full Flag function ( $\overline{FF}$ ) to indicate whether or not the SFC has any free space for writing. In IDT Standard mode, every word read from the SFC, including the first, must be requested using the Read Enable ( $\overline{REN}$ ) and RCLK.

If, at the time of Master Reset, FWFT is HIGH, then FWFT mode will be selected. This mode uses Output Ready ( $\overline{OR}$ ) to indicate whether or not there is valid data at the data outputs (Qn). It also uses Input Ready ( $\overline{IR}$ ) to indicate whether or not the SFC has any free space for writing. In the FWFT mode, the first word written to an empty SFC goes directly to Qn after three RCLK rising edges,  $\overline{REN} = \text{LOW}$  is not necessary. Subsequent words must be accessed using the Read Enable ( $\overline{REN}$ ) and RCLK.

#### WRITE STROBE AND WRITE CLOCK (WR/WCLK)

If synchronous operation of the write port has been selected via  $\overline{ASYW}$ , this input behaves as WCLK.

A write cycle is initiated on the rising edge of the WCLK input. Data setup and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. It is permissible to stop the WCLK. Note that while WCLK is idle, the  $\overline{FF}/\overline{IR}$ , and  $\overline{PAF}$  flags will not be updated. The Write and Read Clocks can either be independent or coincident.

If asynchronous operation has been selected this input is WR (write strobe). Data is asynchronously written into the SFC via the Dn inputs whenever there is a rising edge on WR. In this mode the  $\overline{WEN}$  input must be LOW.

#### WRITE ENABLE ( $\overline{WEN}$ )

When the  $\overline{WEN}$  input is LOW, data may be loaded into the SFC on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When  $\overline{WEN}$  is HIGH, no new data is written in the SFC.

To prevent data overflow in the IDT Standard mode,  $\overline{FF}$  will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle,  $\overline{FF}$  will go HIGH allowing a write to occur. The  $\overline{FF}$  is updated by two WCLK cycles + tsKEW after the RCLK cycle.

To prevent data overflow in the FWFT mode,  $\overline{IR}$  will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle,  $\overline{IR}$  will go LOW allowing a write to occur. The  $\overline{IR}$  flag is updated by two WCLK cycles + tsKEW after the valid RCLK cycle.

$\overline{WEN}$  is ignored when the SFC is full in either FWFT or IDT Standard mode.

If asynchronous operation of the write port has been selected, then  $\overline{WEN}$  must be held active.

### READ STROBE AND READ CLOCK (RD/RCLK)

If synchronous operation of the read port has been selected via  $\overline{ASYR}$ , this input behaves as RCLK. A read cycle is initiated on the rising edge of the RCLK input. Data can be read on the outputs, on the rising edge of the RCLK input. It is permissible to stop the RCLK. Note that while RCLK is idle, the  $\overline{EF/OR}$  and  $\overline{PAE}$  flags will not be updated. The Write and Read Clocks can be independent or coincident.

If asynchronous operation has been selected this input is RD (Read Strobe). Data is asynchronously read from the SFC whenever there is a rising edge on RD. In this mode the  $\overline{REN}$  and  $\overline{RCS}$  inputs must be tied LOW. The  $\overline{OE}$  input is used to provide asynchronous control of the three-state Qn outputs.

### WRITE CHIP SELECT ( $\overline{WCS}$ )

The  $\overline{WCS}$  disables all Write data operations (data only) if it is held HIGH. To perform normal operations on the write port, the  $\overline{WCS}$  must be enabled, held LOW.

### READ ENABLE ( $\overline{REN}$ )

When Read Enable is LOW, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When the  $\overline{REN}$  input is HIGH, the output register holds the previous data and then no new data is loaded into the output register. The data outputs Q0-Qn maintain the previous data value.

In the IDT Standard mode, every word accessed at Qn, including the first word written to an empty cache, must be requested using  $\overline{REN}$  provided that  $\overline{RCS}$  is LOW. When the last word has been read from the SFC, the Empty Flag ( $\overline{EF}$ ) will go LOW, inhibiting further read operations.  $\overline{REN}$  is ignored when the SFC is empty. Once a write is performed,  $\overline{EF}$  will go HIGH allowing a read to occur. The  $\overline{EF}$  flag is updated by two RCLK cycles + tsKEW after the valid WCLK cycle. Both  $\overline{RCS}$  and  $\overline{REN}$  must be active, LOW for data to be read out on the rising edge of RCLK.

In the FWFT mode, the first word written to an empty SFC automatically goes to the outputs Qn, on the third valid LOW-to-HIGH transition of RCLK + tsKEW after the first write.  $\overline{REN}$  and  $\overline{RCS}$  do not need to be asserted LOW for the First Word to fall through to the output register. In order to access all other words, a read must be executed using  $\overline{REN}$  and  $\overline{RCS}$ . The RCLK LOW-to-HIGH transition after the last word has been read from the SFC, Output Ready ( $\overline{OR}$ ) will go HIGH with a true read (RCLK with  $\overline{REN} = \text{LOW}; \overline{RCS} = \text{LOW}$ ), inhibiting further read operations.  $\overline{REN}$  is ignored when the SFC is empty.

If asynchronous operation of the Read port has been selected, then  $\overline{REN}$  must be held active, (LOW).

### OUTPUT ENABLE ( $\overline{OE}$ )

When Output Enable is enabled (LOW), the parallel output buffers receive data from the output register. When  $\overline{OE}$  is HIGH, the output data bus (Qn) goes into a high impedance state. During Master or a Partial Reset the  $\overline{OE}$  is the only

input that can place the output bus Qn, into High-Impedance. During Reset the  $\overline{RCS}$  input can be HIGH or LOW, it has no effect on the Qn outputs.

### READ CHIP SELECT ( $\overline{RCS}$ )

The Read Chip Select input provides synchronous control of the Read output port. When  $\overline{RCS}$  goes LOW, the next rising edge of RCLK causes the Qn outputs to go to the Low-Impedance state. When  $\overline{RCS}$  goes HIGH, the next RCLK rising edge causes the Qn outputs to return to HIGH-Z. During a Master or Partial Reset the  $\overline{RCS}$  input has no effect on the Qn output bus,  $\overline{OE}$  is the only input that provides High-Impedance control of the Qn outputs. If  $\overline{OE}$  is LOW the Qn data outputs will be Low-Impedance regardless of  $\overline{RCS}$  until the first rising edge of RCLK after a Reset is complete. Then if  $\overline{RCS}$  is HIGH the data outputs will go to High-Impedance.

The  $\overline{RCS}$  input does not effect the operation of the flags. For example, when the first word is written to an empty SFC, the  $\overline{EF}$  will still go from LOW to HIGH based on a rising edge of RCLK, regardless of the state of the  $\overline{RCS}$  input.

Also, when operating the SFC in FWFT mode the first word written to an empty SFC will still be clocked through to the output register based on RCLK, regardless of the state of  $\overline{RCS}$ . For this reason the user must take care when a data word is written to an empty SFC in FWFT mode. If  $\overline{RCS}$  is disabled when an empty SFC is written into, the first word will fall through to the output register, but will not be available on the Qn outputs which are in HIGH-Z. The user must take  $\overline{RCS}$  active LOW to access this first word, place the output bus in LOW-Z.  $\overline{REN}$  must remain disabled HIGH for at least one cycle after  $\overline{RCS}$  has gone LOW. A rising edge of RCLK with  $\overline{RCS}$  and  $\overline{REN}$  active LOW, will read out the next word. Care must be taken so as not to lose the first word written to an empty SFC when  $\overline{RCS}$  is HIGH. See Figure 15 for *Read Chip Select*. If asynchronous operation of the Read port has been selected, then  $\overline{RCS}$  must be held active, (tied LOW).  $\overline{OE}$  provides three-state control of Qn.

### BUS-MATCHING (BM[3:0])

These pins are used to define the input and output bus widths. During Master Reset, the state of these pins is used to configure the device bus sizes. All flags will operate on the word/byte size boundary as defined by the selection of bus width. See Figures 22-25 for *Bus-Matching Configurations*. See Table 11, Bus-Matching Configurations for the available configurations.

**TABLE 11 – BUS-MATCHINGS**

BM0	BM1	BM2	BM3	Read Bus Width	Write Bus Width
0	0	0	1	x36	x36
1	0	0	1	x18	x36
1	0	1	1	x9	x36
1	1	0	1	x36	x18
1	1	1	1	x36	x9
1	0	0	0	x18	x18
1	0	1	0	x9	x18
1	1	0	0	x18	x9
1	1	1	0	x9	x9

### FLAG SELECT (FSEL[1:0])

During master reset, these inputs will select one of four default values for the programmable flags  $\overline{PAE}$  and  $\overline{PAF}$ . The selected value (listed in Table 12 - MTYPE[1:0] Configurations) will apply to both  $\overline{PAE}$  and  $\overline{PAF}$  offset.



### MEMORY CONFIGURATION (MIC[2:0])

These signals enable the EDC feature of the device. See Table 6, Error Detection and Correction (EDC) for more information.

### MEMORY SPEED (MSPEED)

This pin is used to determine the memory interface clock speed (CK and  $\overline{CK}$ ) for the external memory used. If MSPEED is HIGH, external memory CK and  $\overline{CK}$  will be operating at 166MHz. If MSPEED is LOW, then the external memory CK and  $\overline{CK}$  will be operating at 133MHz.

### MASTER CLOCK (MCLK)

33MHz reference clock used to generate CK and  $\overline{CK}$  for external memory interface.

### MEMORY TYPE (MTYPE[1:0])

These signals select the density configuration of the external DDR SDRAM used. See Table 12, for selection of the memory density configuration.

**TABLE 12 –  
MTYPE[1:0] CONFIGURATIONS**

	Density Configurations			
	4M x 32	8M x 32	8M x 16	16M x 16
MTYPE0	0	0	1	1
MTYPE1	0	1	0	1

### DEPTH EXPANSION MODE SELECT (IDEM)

This select pin is used for depth expansion configuration in IDT Standard mode. If this pin is tied HIGH, then the  $\overline{FF}/\overline{IR}$  signal will be inverted to provide a seamless depth expansion interface. If this pin is tied LOW, the depth expansion in IDT Standard mode will be deactivated. For details on depth expansion configuration, see Figure 34, *Depth Expansion Configuration in IDT Standard Mode* and Figure 35, *Depth Expansion Configuration in FWFT Mode*.

### SERIAL READ ENABLE ( $\overline{SREN}$ )

The serial read enable input is an enable used for reading the value of the programmable offset registers. By setting the JSEL pin to LOW, the serial data output (SO) and serial clock (SCLK) signals can be used with  $\overline{SREN}$  to program the offset registers. When  $\overline{SREN}$  is LOW, data at the SO can be read from the offset register, one bit for each LOW-to-HIGH transition of SCLK. When serial read enable is HIGH, the reading of the offset registers will stop.  $\overline{SREN}$  must be kept LOW in order to read the entire contents of the scan out register. If at any point  $\overline{SREN}$  is toggled HIGH, the read pointer of the offset registers will reset to the first location. The next time  $\overline{SREN}$  is enabled the first contents in the offset register will be read back. Serial read enable functions the same way in both IDT Standard and FWFT modes. See Figure 30, *Reading of Programmable Flag Registers*, for the timing diagram.

### SERIAL WRITE ENABLE ( $\overline{SWEN}$ )

The serial write enable input is an enable used for serial programming of the programmable offset registers. By setting the JSEL pin to LOW, the serial input (SI) and serial clock (SCLK) signals can be used with  $\overline{SWEN}$  to program the offset registers. When  $\overline{SWEN}$  is LOW, data at the SI input are loaded into the offset register, one bit for each LOW-to-HIGH transition of SCLK. When  $\overline{SWEN}$  is HIGH, the offset registers retain the previous settings and no offsets are loaded. Serial write enable functions the same way in both Standard IDT and FWFT

modes. See Figure 29, *Loading of Programmable Flag Registers*, for the timing diagram.

### I/O VDDQ SELECT (IOSEL)

This input determines whether the inputs and outputs will tolerate a 2.5V or 3.3V voltage signals. If IOSEL is HIGH, then all I/Os will be 3.3V levels. If IOSEL is LOW, then all I/Os will be 2.5V levels.

### JTAG SELECT (JSEL)

This input determines whether the JTAG port will be activated or deactivated. If JSEL is HIGH, then the JTAG port is activated and the associated JTAG pins (TCK, TDI, TDO, TMS) are used for the boundary-scan function. If JSEL is LOW, the JTAG port is disabled and the serial programming pins (SCLK, SI, SO) will be used to program and read the offset register values for  $\overline{PAE}$  and  $\overline{PAF}$ . See Figure 29 and 30, *Serial Loading and Reading of Programmable Registers* for information on how to program the registers.

## OUTPUTS

### FULL FLAG/INPUT READY ( $\overline{FF}/\overline{IR}$ )

This is a dual purpose pin. In IDT Standard mode, the Full Flag ( $\overline{FF}$ ) function is selected. When the SFC is full,  $\overline{FF}$  will go LOW, inhibiting further write operations. When  $\overline{FF}$  is HIGH, the SFC is not full. If no reads are performed after a reset (either  $\overline{MRS}$  or  $\overline{PRS}$ ),  $\overline{FF}$  will go LOW. See Figure 12, *Full Boundary - IDT Standard Mode*, for the relevant timing information.

In FWFT mode, the Input Ready ( $\overline{IR}$ ) function is selected.  $\overline{IR}$  goes LOW when memory space is available for writing in data. When there is no longer any free space left,  $\overline{IR}$  goes HIGH, inhibiting further write operations. If no reads are performed after a reset (either  $\overline{MRS}$  or  $\overline{PRS}$ ),  $\overline{IR}$  will go HIGH. See Figure 9 *Write First Word Cycles - FWFT Mode*, for the relevant timing information.

The  $\overline{IR}$  status not only measures the contents of the SFC memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to de-assert  $\overline{IR}$  is one greater than needed to assert  $\overline{FF}$  in IDT Standard mode.

$\overline{FF}/\overline{IR}$  is synchronous and updated on the rising edge of WCLK.  $\overline{FF}/\overline{IR}$  are double register-buffered outputs.

### EMPTY FLAG ( $\overline{EF}/\overline{OR}$ )

This is a dual purpose pin. In the IDT Standard mode, the Empty Flag ( $\overline{EF}$ ) function is selected. When the SFC is empty,  $\overline{EF}$  will go LOW, inhibiting further read operations. When  $\overline{EF}$  is HIGH, the SFC is not empty. *Figure 10, Empty Boundary - IDT Standard Mode* for the relevant timing information.

In FWFT mode, the Output Ready ( $\overline{OR}$ ) function is selected.  $\overline{OR}$  goes LOW at the same time that the first word written to an empty SFC appears valid on the outputs.  $\overline{OR}$  stays LOW after the RCLK LOW to HIGH transition that shifts the last word from the SFC to the outputs.  $\overline{OR}$  goes HIGH only with a true read (RCLK with  $\overline{REN} = \text{LOW}$ ). The previous data stays at the outputs, indicating the last word was read. Further data reads are inhibited until  $\overline{OR}$  goes LOW again. See Figure 11, *Empty Boundary (FWFT Mode)*, for the relevant timing information.

$\overline{EF}/\overline{OR}$  is synchronous and updated on the rising edge of RCLK.

In IDT Standard mode,  $\overline{EF}$  is a double register-buffered output. In FWFT mode,  $\overline{OR}$  is a triple register-buffered output.

### PROGRAMMABLE ALMOST-FULL FLAG ( $\overline{PAF}$ )

The Programmable Almost-Full flag ( $\overline{PAF}$ ) will go LOW when the SFC reaches the almost-full condition. In IDT Standard mode, if no reads are performed after reset ( $\overline{MRS}$ ),  $\overline{PAF}$  will go LOW after (D - m) words are written

to the SFC. See *Figure 22, Synchronous  $\overline{PAF}$  Flag - IDT Standard Mode and FWFT Mode*, for the relevant timing information.

If asynchronous  $\overline{PAF}$  configuration is selected, the  $\overline{PAF}$  is asserted LOW on the LOW-to-HIGH transition of the Write Clock (WCLK).  $\overline{PAF}$  is reset to HIGH on the LOW-to-HIGH transition of the Read Clock (RCLK). If synchronous  $\overline{PAF}$  configuration is selected, the  $\overline{PAF}$  is updated on the rising edge of WCLK.

#### PROGRAMMABLE ALMOST-EMPTY FLAG ( $\overline{PAE}$ )

The Programmable Almost-Empty flag ( $\overline{PAE}$ ) will go LOW when the SFC reaches the almost-empty condition. In IDT Standard mode,  $\overline{PAE}$  will go LOW when there are  $n$  words or less in the SFC. The offset " $n$ " is the empty offset value. The default setting for this value is in Table 8, Device Configuration.

In FWFT mode, the  $\overline{PAE}$  will go LOW when there are  $n+1$  words or less in the SFC. See *Figure 21, Synchronous  $\overline{PAE}$  Flag - IDT Standard Mode and FWFT Mode*, for the relevant timing information.

If asynchronous  $\overline{PAE}$  configuration is selected, the  $\overline{PAE}$  is asserted LOW on the LOW-to-HIGH transition of the Read Clock (RCLK).  $\overline{PAE}$  is reset to HIGH on the LOW-to-HIGH transition of the Write Clock (WCLK). If synchronous  $\overline{PAE}$  configuration is selected, the  $\overline{PAE}$  is updated on the rising edge of RCLK.

#### DATA OUTPUTS (Q0-Q35)

(Q0-Q35) are data outputs for 36-bit wide data, (Q0 - Q17) are data outputs for 18-bit wide data or (Q0-Q8) are data outputs for 9-bit wide data.

#### MEMORY CLOCK OUTPUT (CK)

These signals are to be connected to the external DDR SDRAM's clock input.

#### MEMORY CLOCK OUTPUT INVERTED ( $\overline{CK}$ )

These signals are to be connected to the external DDR SDRAM's differential clock input.

#### MEMORY BANK ADDRESS INPUT BIT (BA[1:0])

These signals are to be connected to the external DDR SDRAM's bank address input bits.

#### MEMORY COLUMN ADDRESS STROBE ( $\overline{CAS}$ )

These signals are to be connected to the external DDR SDRAM's column address strobe input.

#### MEMORY ADDRESS BUS (A[12:0])

These signals are to be connected to the external DDR SDRAM's address bus.

#### MEMORY WRITE ENABLE ( $\overline{WE}$ )

These signals are to be connected to the external DDR SDRAM's write enable.

#### MEMORY ROW ADDRESS STROBE ( $\overline{RAS}$ )

These signals are to be connected to the external DDR SDRAM's row address strobe input.

### BI-DIRECTIONAL I/O

#### MEMORY DATA INPUTS/OUTPUTS DQ[63:0]

These signals are to be connected to the external DDR SDRAM's data input bus.

#### MEMORY DATA STROBE OUTPUT DQS[7:0]

These signals are to be connected to the external DDR SDRAM's data strobe inputs.

## ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Unit
V <sub>TERM</sub>	Terminal Voltage with respect to GND	-0.5 to +3.6 <sup>(2)</sup>	V
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
T <sub>JMAX</sub>	Maximum Junction Temp.	150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Compliant with JEDEC JESD8-5. V<sub>CC</sub> terminal only.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub> <sup>(2,3)</sup>	Input Capacitance	V <sub>IN</sub> = 0V	10 <sup>(3)</sup>	pF
C <sub>OUT</sub> <sup>(1,2)</sup>	Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

### NOTES:

- With output deselected, ( $\overline{OE} \geq V_{IH}$ ).
- Characterized values, not currently tested.
- C<sub>IN</sub> for V<sub>ref</sub> is 20pF.

## PACKAGE THERMAL DATA

Symbol	Parameter	Industrial/ Commercial	Unit
θ <sub>JC</sub>	Junction to case thermal resistance	3.8	C/W
θ <sub>JA</sub>	Junction to air thermal resistance airflow @ 0m/s @ 1m/s @ 2m/s @ 3m/s @ 4m/s @ 5m/s	27.4 22.8 20.3 19.5 18.2 17.8	C/W
MSL	Moisture sensitivity level	3	

## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	2.375	2.5	2.625	V
V <sub>DDQ</sub>	Output Rail Voltage for I/Os	2.375	—	3.45	V
GND	Supply Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage @ 3.3V @ 2.5V	2.0 1.7	— —	5.5 3.45	V V
V <sub>IL</sub>	Input Low Voltage @ 3.3V @ 2.5V	— -0.3	— —	0.8 0.7	V V
V <sub>REF</sub>	Voltage Reference Input	1.15	1.25	1.35	V
T <sub>A</sub>	Operating Temperature (Commercial)	0	—	70	°C
T <sub>A</sub>	Operating Temperature (Industrial)	-40	—	85	°C



## DC ELECTRICAL CHARACTERISTICS

(Commercial:  $V_{CC} = 2.5V \pm 0.125V$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ; Industrial:  $V_{CC} = 2.5V \pm 0.125V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{LI}^{(1)}$	Input leakage current	-10	—	10	mA
$I_{LO}^{(2)}$	Output leakage current	-10	—	10	mA
$V_{OH1}$	Read/Write interface output logic "1" voltage	$V_{DDQ} = 3.3V$	$V_{DDQ} - 0.4$	—	V
		$V_{DDQ} = 2.5V$	$V_{DDQ} - 0.4$	—	V
$V_{OH2}$	Memory interface output logic "1" voltage	1.46	—	2.8	V
$V_{OL1}$	Read/Write interface output logic "0" voltage	$V_{DDQ} = 3.3V$	—	0.4	V
		$V_{DDQ} = 2.5V$	—	0.4	V
$V_{OL2}$	Memory interface output logic "0" voltage	—	—	1.04	V
$I_{OH1}$	Read/Write interface output high current (source current)	-8	—	—	mA
$I_{OH2}$	Read/Write interface output low current (sink current)	-16	—	—	mA
$I_{OL1}$	Read/Write interface output low current (sink current)	8	—	—	mA
$I_{OL2}$	Memory interface output low current (sink current)	16	—	—	mA
$I_{CC}^{(5)}$	Active $V_{CC}$ current	—	380	1300	mA
$I_{SB}$	Standby $V_{CC}$ current	—	—	50	mA

### NOTES:

- Measurements with  $0.4 \leq V_{IN} \leq V_{CC}$ .
- $\overline{OE} \geq V_{IH}$ ,  $0.4 \leq V_{OUT} \leq V_{CC}$ .
- Tested with outputs open ( $I_{OUT} = 0$ ).
- RCLK and WCLK toggle at 20MHz and data inputs switch at 10MHz.
- Typical values represent frequency = 0MHz. Maximum values represent frequency = 166MHz.
- This is the formula used for calculating  $I_{CC}$ :

$$P = C \times V^2 \times f \times D \times BW$$

$$I_{CC} = \frac{P}{V}$$

- f = operating frequency
- C = capacitive load
- V =  $V_{CC}$  voltage
- D = duty cycle
- BW = bus width

### 2.5V AC TEST CONDITIONS

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	1ns
Input Timing Reference Levels	V <sub>CC</sub> /2
Output Reference Levels	V <sub>DDQ</sub> /2

### AC TEST LOADS

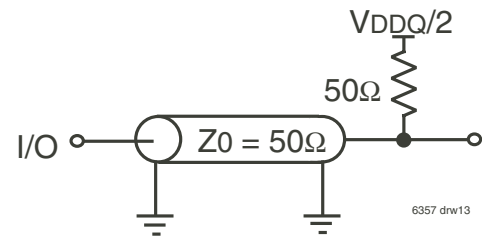


Figure 5a. AC Test Load

### 3.3V AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

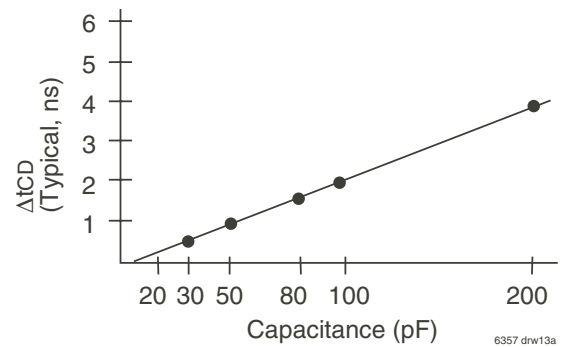


Figure 5b. Lumped Capacitive Load, Typical Derating

## AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup> — SYNCHRONOUS TIMING

(Commercial: VCC = 2.5V ± 5%, TA = 0°C to +70°C; Industrial: VCC = 2.5V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Commercial		Com'l & Ind'l <sup>(2)</sup>		Unit
		IDT72T6360L6		IDT72T6360L7-5		
		Min.	Max.	Min.	Max.	
f <sub>s</sub>	Synchronous Clock Cycle Frequency	—	166	—	133	MHz
t <sub>A</sub>	Data Access Time	1	4	1	5	ns
t <sub>CLK</sub>	Clock Cycle Time	6	—	7.5	—	ns
t <sub>CLKH</sub>	Clock High Time	2.7	—	3.5	—	ns
t <sub>CLKL</sub>	Clock Low Time	2.7	—	3.5	—	ns
t <sub>DS</sub>	Data Setup Time	2	—	2.5	—	ns
t <sub>DH</sub>	Data Hold Time	0.5	—	0.5	—	ns
t <sub>ENS</sub>	Enable Setup Time	2	—	2.5	—	ns
t <sub>ENH</sub>	Enable Hold Time	0.5	—	0.5	—	ns
t <sub>RS</sub>	Reset Pulse Width	200	—	200	—	ns
t <sub>RSU</sub>	Reset Setup Time	15	—	15	—	ns
t <sub>RSH</sub>	Reset Hold Time	10	—	10	—	ns
t <sub>PL</sub>	Reset to PLL Lock	20	—	20	—	μs
t <sub>RSF</sub>	Reset to Flag and Output	—	15	—	15	ns
t <sub>OHZ</sub>	Output enable to High-Z	1	4	1	5	ns
t <sub>OE</sub>	Output Enable Valid	1	4	1	5	ns
f <sub>M</sub>	Master Clock Cycle Frequency	32	34	32	34	MHz
t <sub>MCYC</sub>	Master Clock Cycle Time	29.4	31.3	29.4	31.3	ns
t <sub>MCKH</sub>	Master Clock Cycle HIGH	0.45	0.55	0.45	0.55	t <sub>MCYC</sub>
t <sub>MCKL</sub>	Master Clock Cycle LOW	0.45	0.55	0.45	0.55	t <sub>MCYC</sub>
f <sub>S</sub>	Serial Clock Cycle Frequency	—	10	—	10	MHz
t <sub>SCLK</sub>	Serial Clock Cycle	100	—	100	—	ns
t <sub>SCLKH</sub>	Serial Clock HIGH	45	—	45	—	ns
t <sub>SCLKL</sub>	Serial Clock LOW	45	—	45	—	ns
t <sub>SDS</sub>	Serial Data Setup	15	—	15	—	ns
t <sub>SDH</sub>	Serial Data Hold	5	—	5	—	ns
t <sub>SENS</sub>	Serial Enable Setup	5	—	5	—	ns
t <sub>ENH</sub>	Serial Enable Hold	5	—	5	—	ns
t <sub>ASO</sub>	Serial Output Data Access Time	—	20	—	20	ns
t <sub>WFFs</sub>	Write Clock to Synchronous $\overline{FF}/\overline{IR}$	—	4	—	5	ns
t <sub>REFs</sub>	Read Clock to Synchronous $\overline{EF}/\overline{OR}$	—	4	—	5	ns
t <sub>PAFs</sub>	WCLK to Synchronous $\overline{PAF}$	—	4	—	5	ns
t <sub>PAEs</sub>	RCLK to Synchronous $\overline{PAE}$	—	4	—	5	ns
t <sub>SKEW1</sub>	Skew time between RCLK and WCLK for $\overline{EF}/\overline{OR}$ and $\overline{FF}/\overline{IR}$ in SDR	4	—	5	—	ns
t <sub>SKEW2</sub>	Skew time between RCLK and WCLK for $\overline{PAE}/\overline{PAF}$	5	—	7	—	ns
t <sub>WCSS</sub>	WCS Setup Time	2	—	2.5	—	ns
t <sub>WCSH</sub>	WCS Hold Time	0.5	—	0.5	—	ns
f <sub>c1</sub>	Memory Clock Cycle Frequency at 166MHz	160	170	—	—	MHz
f <sub>c2</sub>	Memory Clock Cycle Frequency at 133MHz	128	136	128	136	MHz
t <sub>CK1</sub>	Memory Clock Cycle Time at 166MHz	6.2	5.9	—	—	ns
t <sub>CK2</sub>	Memory Clock Cycle Time at 133MHz	7.8	7.3	7.8	7.3	ns
t <sub>CKH1</sub>	Memory Clock Cycle HIGH at 166MHz	0.45	0.55	—	—	t <sub>CK1</sub>
t <sub>CKH2</sub>	Memory Clock Cycle HIGH at 133MHz	0.45	0.55	0.45	0.55	t <sub>CK2</sub>
t <sub>CKL1</sub>	Memory Clock Cycle LOW at 166MHz	0.45	0.55	—	—	t <sub>CK1</sub>
t <sub>CKL2</sub>	Memory Clock Cycle LOW at 133MHz	0.45	0.55	0.45	0.55	t <sub>CK2</sub>

### NOTES:

- All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
- Industrial temperature range product for the 7.5ns speed grade is available as a standard device. All other speed grades are available by special order.

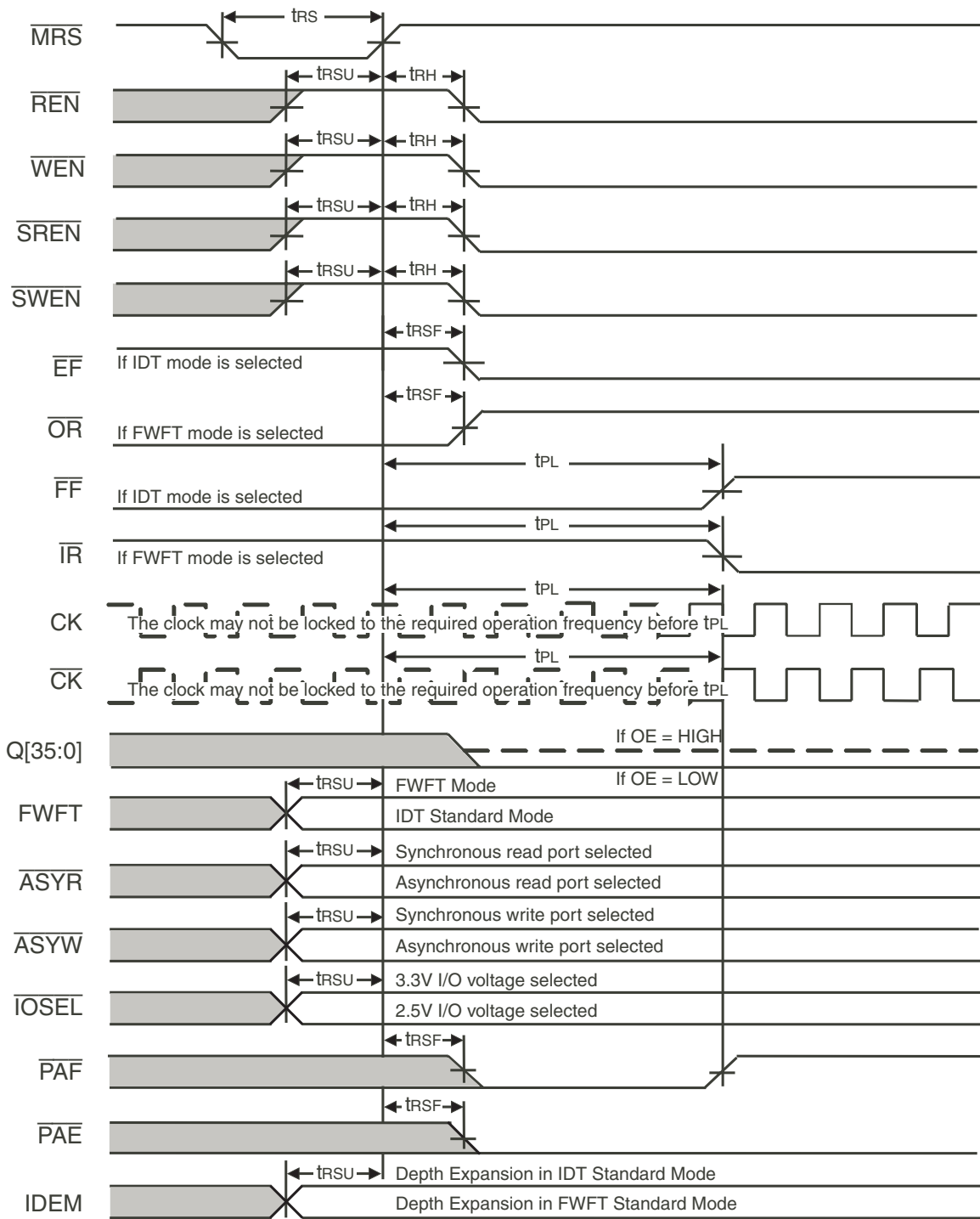
## AC ELECTRICAL CHARACTERISTICS — ASYNCHRONOUS TIMING

(Commercial:  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ; Industrial:  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Symbol	Parameter	Commercial		Com'l & Ind'l <sup>(2)</sup>		Unit
		IDT72T6360L6		IDT72T6360L7-5		
		Min.	Max.	Min.	Max.	
$f_A$	Asynchronous Clock Cycle Frequency	—	100	—	83	MHz
$t_{Aa}$	Data Access Time	0.6	8	0.6	10	ns
$t_{CYC}$	Cycle Time	10	—	12	—	ns
$t_{CYCH}$	Cycle HIGH Time	4.5	—	5	—	ns
$t_{CYCL}$	Cycle LOW Time	4.5	—	5	—	ns
$t_{FFa}$	Rising Edge to $\overline{FF}$	—	8	—	10	ns
$t_{EFa}$	Rising Edge to $\overline{EF}$	—	8	—	10	ns
$t_{PAFa}$	Rising Edge to $\overline{PAF}$	—	8	—	10	ns
$t_{PAEa}$	Rising Edge to $\overline{PAE}$	—	8	—	10	ns
$t_{RPE}$	Read Pulse after $\overline{EF}$ HIGH	8	—	10	—	ns

### NOTES:

1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Industrial temperature range product for the 7.5ns speed grade is available as a standard device. All other speed grades are available by special order.



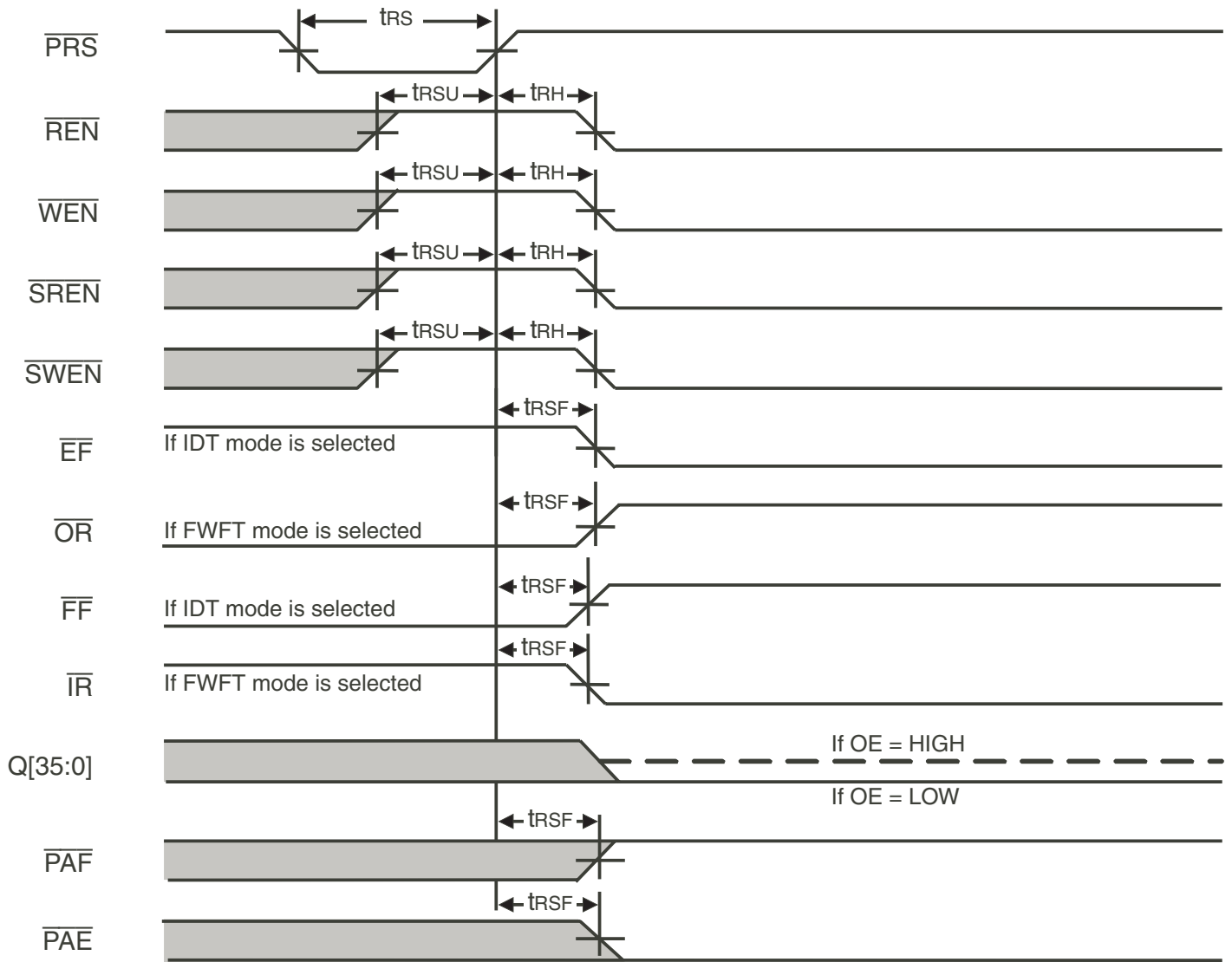
6357 drw20

**NOTE:**

1. For other signals that are latched during master reset, refer to Master Reset and Device Configuration section.

Symbol	Parameter	Min.	Max.	Unit
$t_{rs}$	Reset Pulse Width	200	—	ns
$t_{rsu}$	Reset Setup Time	15	—	ns
$t_{rsh}$	Reset Hold Time	10	—	ns
$t_{PL}$	Reset to PLL Lock	20	—	$\mu$ s
$t_{rsf}$	Reset to Flag and Output	—	15	ns

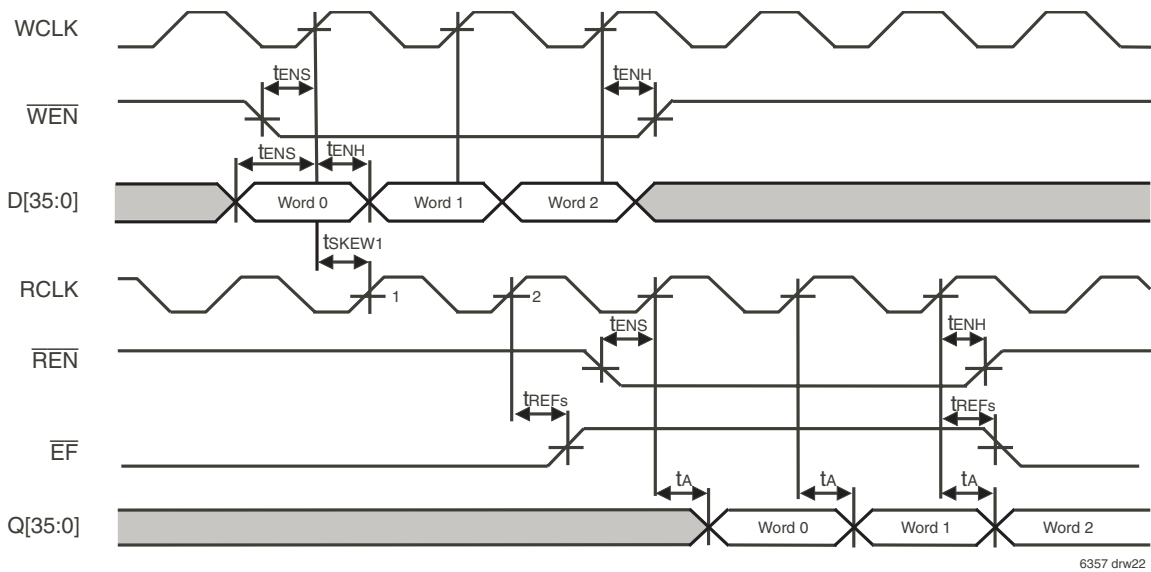
Figure 6. Master Reset and Initialization



6357 dnrw21

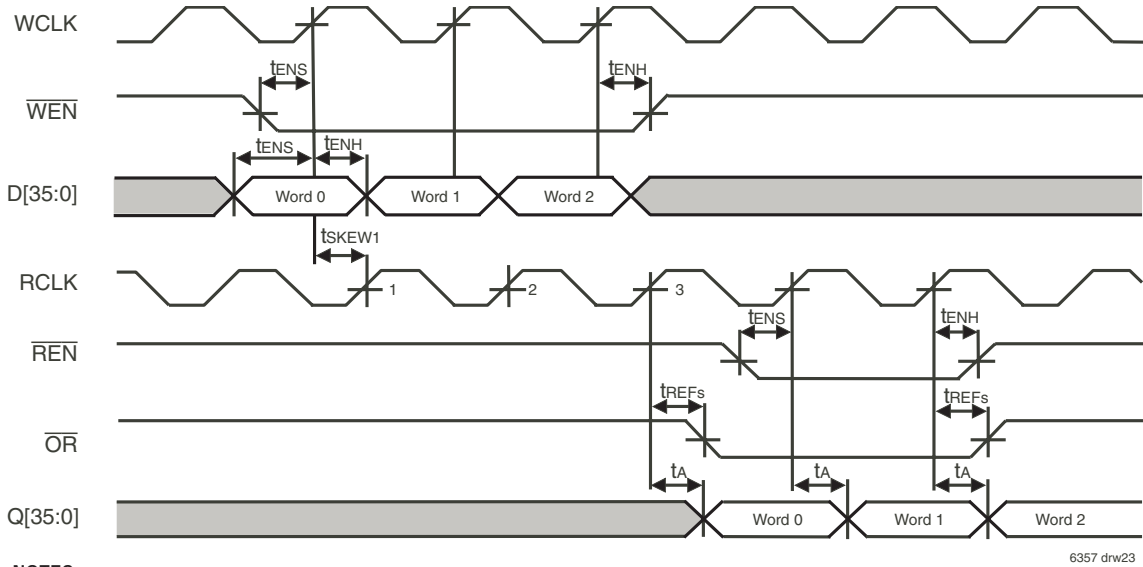
Symbol	Parameter	Min.	Max.	Unit
$t_{RS}$	Reset Pulse Width	200	—	ns
$t_{RSU}$	Reset Setup Time	15	—	ns
$t_{RH}$	Reset Hold Time	10	—	ns
$t_{PL}$	Reset to PLL Lock	20	—	$\mu$ s
$t_{RSF}$	Reset to Flag and Output	—	15	ns

Figure 7. Partial Reset



- NOTES:**
1. tsKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH after one RCLK cycle (plus tREFs). If tsKEW1 is not met, then  $\overline{EF}$  de-assertion may be delayed one extra RCLK cycle.
  2. Settings:  $\overline{OE}$  = LOW, RCS = LOW, WCS = LOW, BM[3:0] = 1000, FWFT = LOW, ASYR = HIGH, and ASYW = HIGH.

Figure 8. Write First Word Cycles - IDT Standard Mode

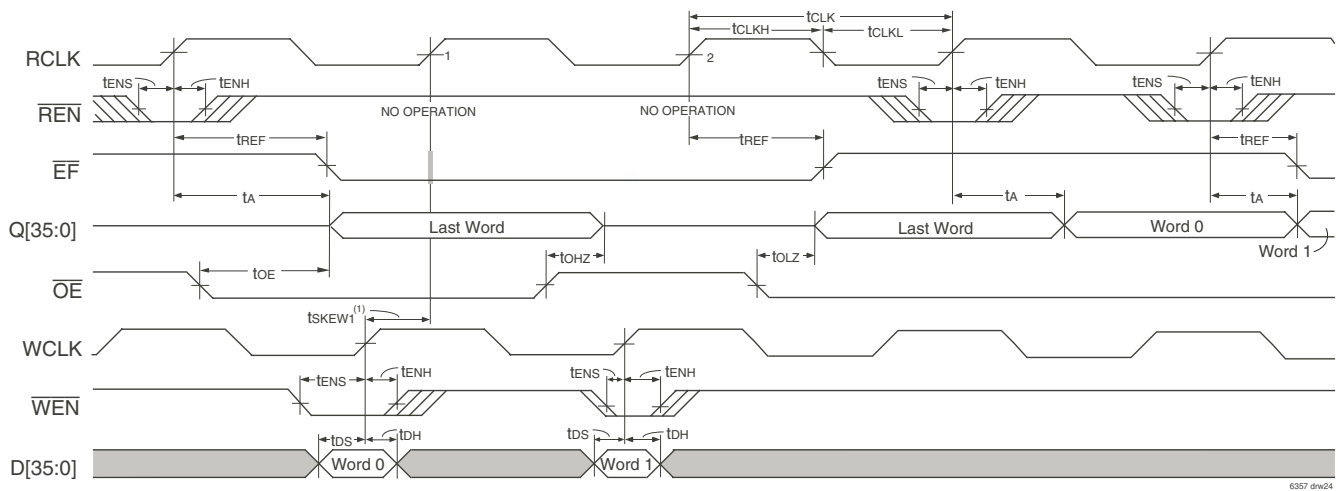


- NOTES:**
1. tsKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH after one RCLK cycle (plus tREFs). If tsKEW1 is not met, then  $\overline{EF}$  de-assertion may be delayed one extra RCLK cycle.
  2. Settings:  $\overline{OE}$  = LOW, RCS = LOW, WCS = LOW, BM[3:0] = 1000, FWFT = HIGH, ASYR = HIGH, and ASYW = HIGH.

Figure 9. Write First Word Cycles - FWFT Mode

Symbol	Parameter	6ns		7-5ns		Unit
		Min.	Max.	Min.	Max.	
tsENS	Serial Enable Setup	5	—	5	—	ns
tsENH	Serial Enable Hold	5	—	5	—	ns
ta	Data Access Time	1	4	1	5	ns
tsKEW1	Skew time between RCLK and WCLK for $\overline{EF}/\overline{OR}$ and $\overline{FF}/\overline{IR}$ in SDR	4	—	5	—	ns
tREFs	Read Clock to Synchronous $\overline{EF}/\overline{OR}$	—	4	—	5	ns

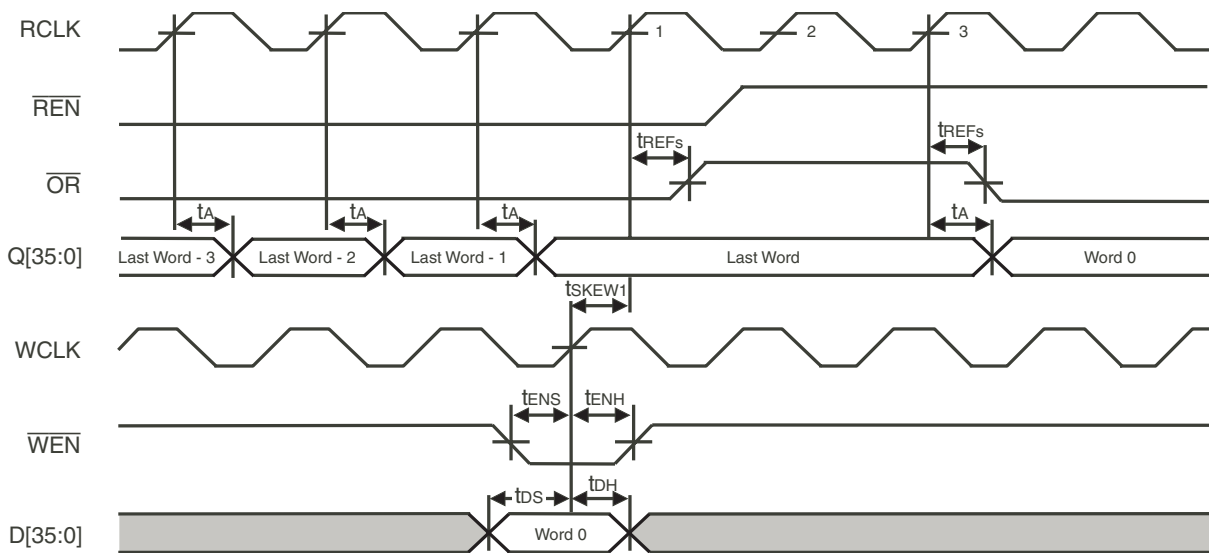




**NOTES:**

1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH after one RCLK cycle (plus tREFs). If tSKEW1 is not met, then  $\overline{EF}$  de-assertion may be delayed one extra RCLK cycle.
2. Settings: RCS = LOW, WCS = LOW, BM[3:0] = 1000, FWFT = LOW, ASYR = HIGH, and ASYW = HIGH.

**Figure 10. Empty Boundary - IDT Standard Mode**

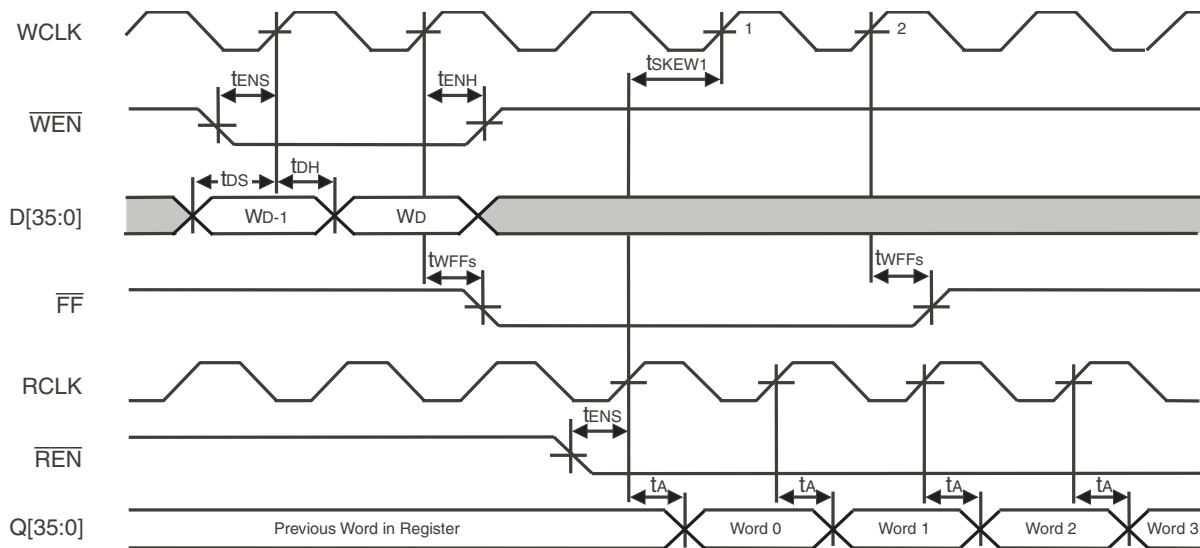


**NOTES:**

1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH after one RCLK cycle (plus tREFs). If tSKEW1 is not met, then  $\overline{EF}$  de-assertion may be delayed one extra RCLK cycle.
2. Settings: OE = LOW, RCS = LOW, WCS = LOW, BM[3:0] = 1000, FWFT = HIGH, ASYR = HIGH, and ASYW = HIGH.

**Figure 11. Empty Boundary - FWFT Mode**

Symbol	Parameter	6ns		7-5ns		Unit
		Min.	Max.	Min.	Max.	
tCLK	Clock Cycle Time	6	—	7.5	—	ns
tCLKH	Clock High Time	2.7	—	3.5	—	ns
tCLKL	Clock Low Time	2.7	—	3.5	—	ns
tDS	Data Setup Time	2	—	2.5	—	ns
tDH	Data Hold Time	0.5	—	0.5	—	ns
tENS	Enable Setup Time	2	—	2.5	—	ns
tENH	Enable Hold Time	0.5	—	0.5	—	ns
tA	Data Access Time	1	4	1	5	ns
tREFs	Read Clock to Synchronous $\overline{EF}/\overline{OR}$	—	4	—	5	ns
tSKEW1	Skew time between RCLK and WCLK for $\overline{EF}/\overline{OR}$ and $\overline{FF}/\overline{IR}$ in SDR	4	—	5	—	ns

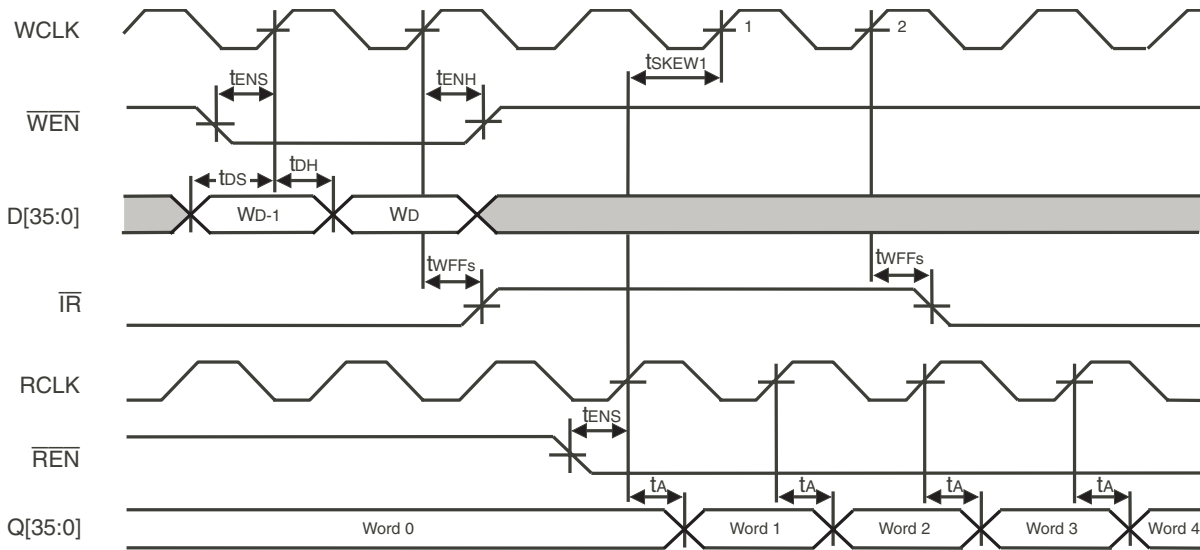


**NOTES:**

1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that  $\overline{FF}$  will go HIGH after one WCLK cycle (plus tWFFs). If tSKEW1 is not met, then  $\overline{FF}$  de-assertion may be delayed one extra WCLK cycle.
2. Settings:  $\overline{OE}$  = LOW, RCS = LOW, WCS = LOW, BM[3:0] = 1000, FWFT = LOW, ASYR = HIGH, and  $\overline{ASYW}$  = HIGH.

6357 drw26

**Figure 12. Full Boundary - IDT Standard Mode**



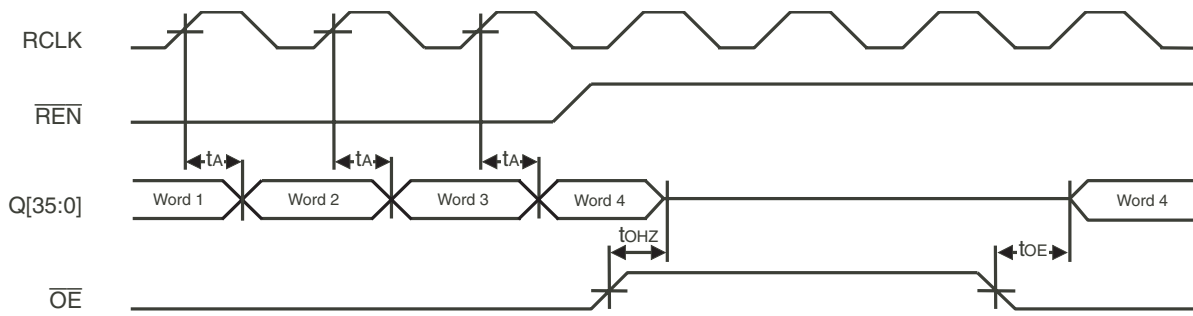
**NOTES:**

1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH after one RCLK cycle (plus tREFs). If tSKEW1 is not met, then  $\overline{EF}$  de-assertion may be delayed one extra RCLK cycle.
2. Settings: RCS = LOW, WCS = LOW, BM[3:0] = 1000, FWFT = HIGH, ASYR = HIGH, and  $\overline{ASYW}$  = HIGH.

6357 drw27

**Figure 13. Full Boundary - FWFT Mode**

Symbol	Parameter	6ns		7.5ns		Unit
		Min.	Max.	Min.	Max.	
tDS	Data Setup Time	2	—	2.5	—	ns
tDH	Data Hold Time	0.5	—	0.5	—	ns
tENS	Enable Setup Time	2	—	2.5	—	ns
tENH	Enable Hold Time	0.5	—	0.5	—	ns
tA	Data Access Time	1	4	1	5	ns
tWFFs	Write Clock to Synchronous $\overline{FF}/\overline{IR}$	—	4	—	5	ns
tSKEW1	Skew time between RCLK and WCLK for $\overline{EF}/\overline{OR}$ and $\overline{FF}/\overline{IR}$ in SDR	4	—	5	—	ns

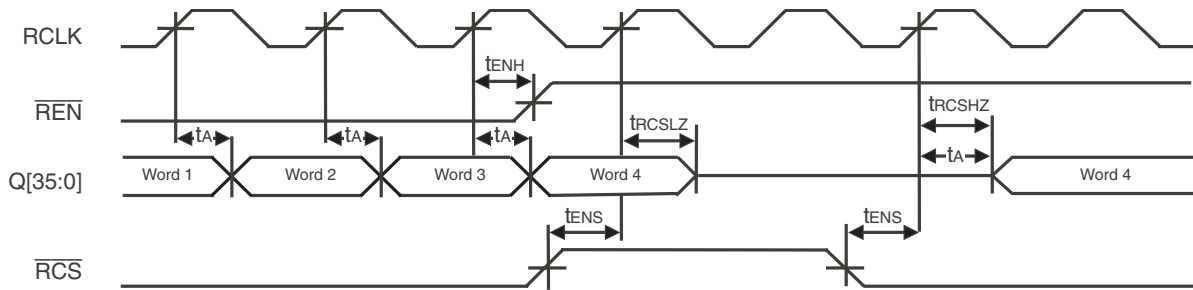


6357 drw28

**NOTE:**

1. Settings:  $\overline{RCS}$  = LOW,  $BM[3:0]$  = 1000,  $FWFT$  = LOW,  $\overline{ASYR}$  = HIGH, and  $\overline{ASYW}$  = HIGH.

Figure 14. Output Enable

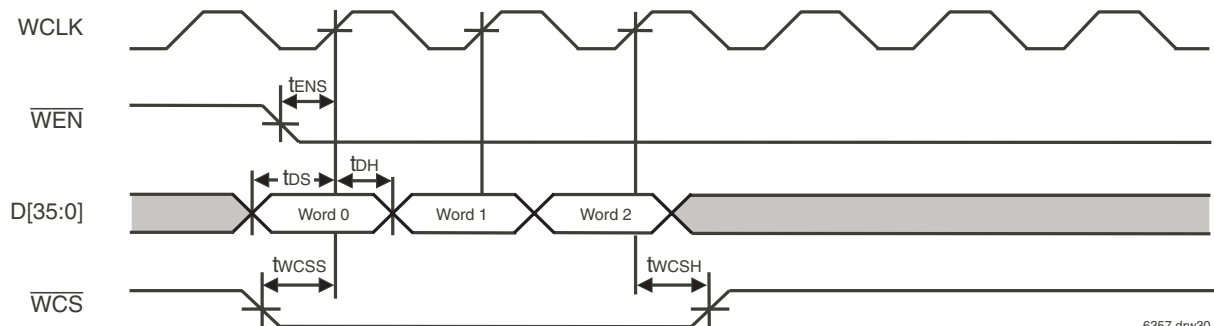


6357 drw29

**NOTE:**

1. Settings:  $\overline{OE}$  = LOW,  $BM[3:0]$  = 1000,  $FWFT$  = LOW,  $\overline{ASYR}$  = HIGH, and  $\overline{ASYW}$  = HIGH.

Figure 15. Read Chip Select



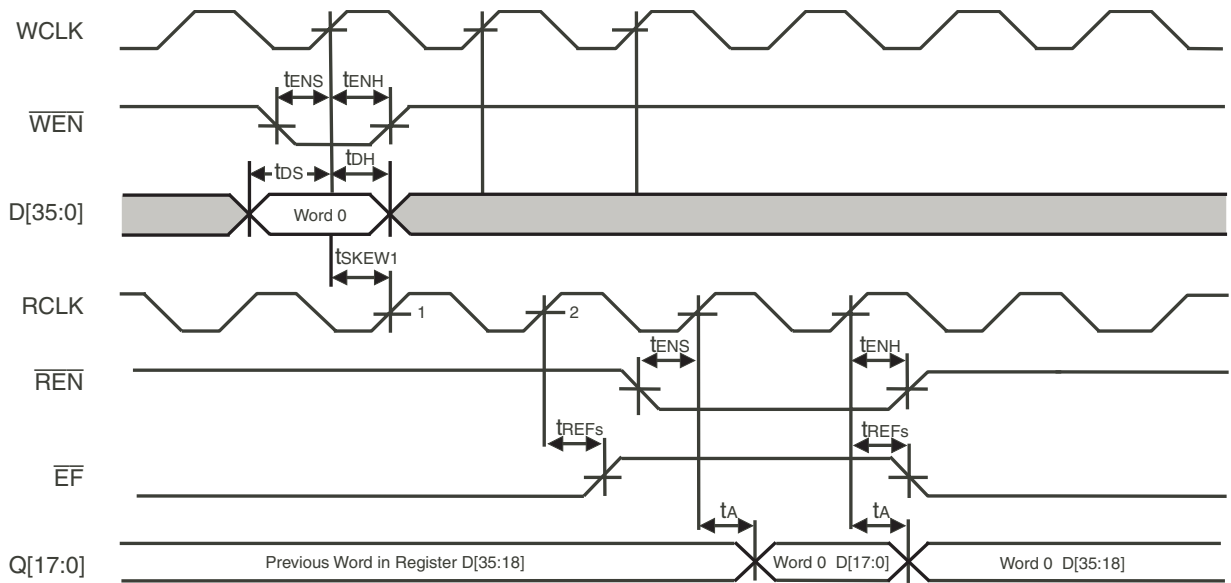
6357 drw30

**NOTE:**

1. Settings:  $BM[3:0]$  = 1000,  $FWFT$  = LOW,  $\overline{ASYR}$  = HIGH, and  $\overline{ASYW}$  = HIGH.

Figure 16. Write Chip Select

Symbol	Parameter	6ns		7.5ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>DS</sub>	Data Setup Time	2	—	2.5	—	ns
t <sub>DH</sub>	Data Hold Time	0.5	—	0.5	—	ns
t <sub>ENS</sub>	Enable Setup Time	2	—	2.5	—	ns
t <sub>ENH</sub>	Enable Hold Time	0.5	—	0.5	—	ns
t <sub>A</sub>	Data Access Time	1	4	1	5	ns
t <sub>OHZ</sub>	Output enable to High-Z	1	4	1	5	ns
t <sub>OE</sub>	Output Enable Valid	1	4	1	5	ns
t <sub>WCSS</sub>	$\overline{WCS}$ Setup Time	2	—	2.5	—	ns
t <sub>WCSH</sub>	$\overline{WCS}$ Hold Time	0.5	—	0.5	—	ns

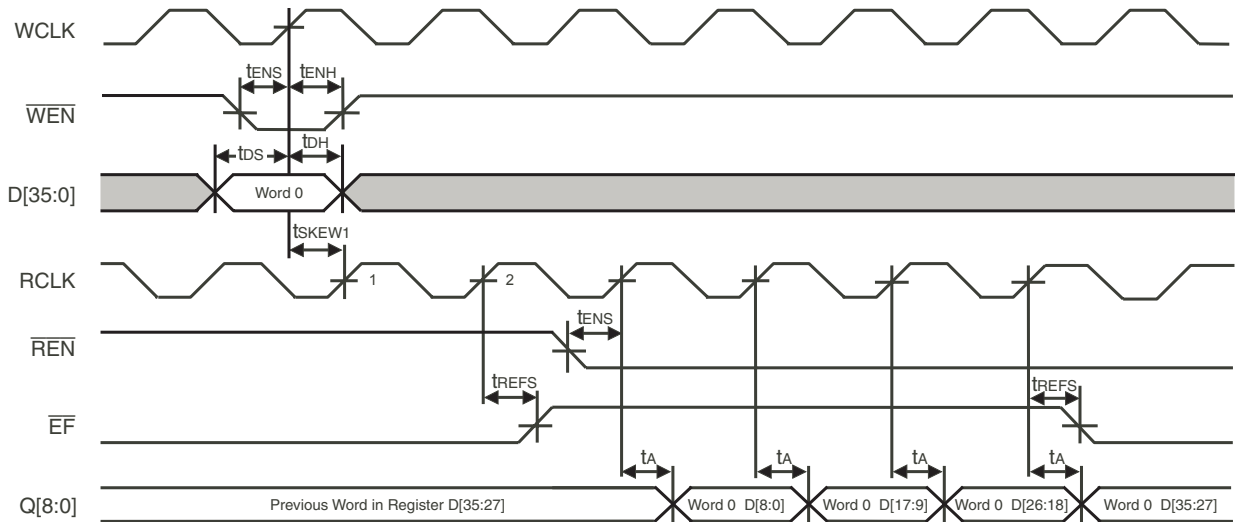


**NOTES:**

1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH after one RCLK cycle (plus tREFS). If tSKEW1 is not met, then  $\overline{EF}$  de-assertion may be delayed one extra RCLK cycle.
2. Settings:  $\overline{OE}$  = LOW, RCS = LOW, WCS = LOW, BM[3:0] = 1011, FWFT = LOW, ASYR = HIGH, and ASYW = HIGH.

6357 drw31

**Figure 17. Bus-Matching Configuration - x36 In to x18 Out - IDT Standard Mode**



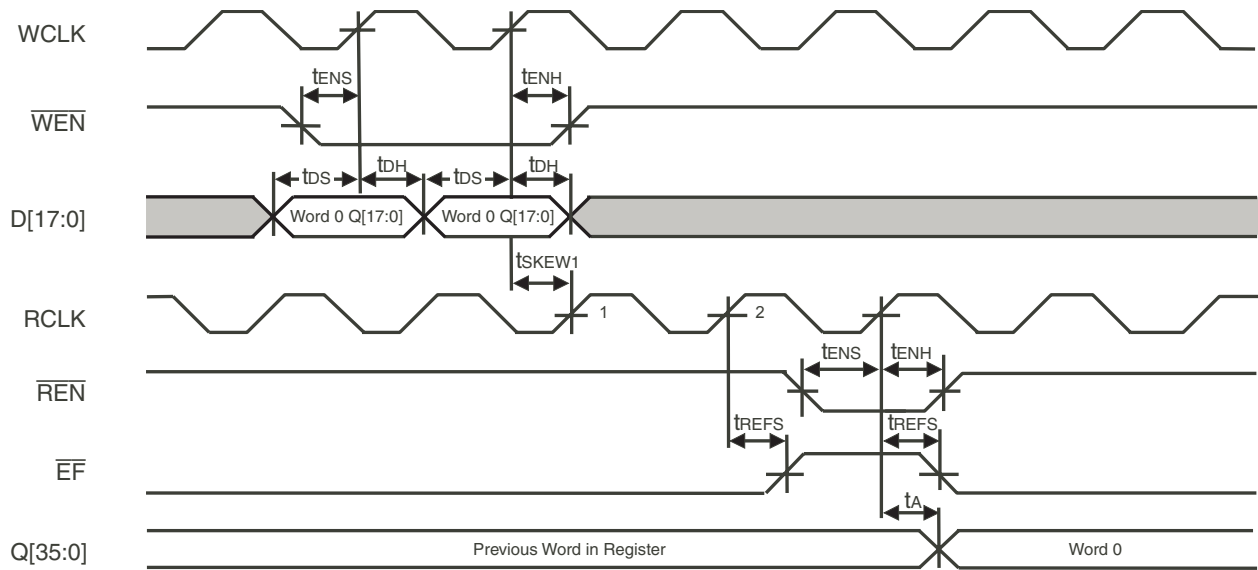
**NOTES:**

1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH after one RCLK cycle (plus tREFS). If tSKEW1 is not met, then  $\overline{EF}$  de-assertion may be delayed one extra RCLK cycle.
2. Settings:  $\overline{OE}$  = LOW, RCS = LOW, WCS = LOW, BM[3:0] = 1111, FWFT = LOW, ASYR = HIGH, and  $\overline{ASYW}$  = HIGH.

6358 drw32

**Figure 18. Bus-Matching Configuration - x36 In to x9 Out - IDT Standard Mode**

Symbol	Parameter	6ns		7-5ns		Unit
		Min.	Max.	Min.	Max.	
tDS	Data Setup Time	2	—	2.5	—	ns
tDH	Data Hold Time	0.5	—	0.5	—	ns
tENS	Enable Setup Time	2	—	2.5	—	ns
tENH	Enable Hold Time	0.5	—	0.5	—	ns
tA	Data Access Time	1	4	1	5	ns
tREFS	Read Clock to Synchronous $\overline{EF}/\overline{OR}$	—	4	—	5	ns
tSKEW1	Skew time between RCLK and WCLK for $\overline{EF}/\overline{OR}$ and $\overline{FF}/\overline{IR}$ in SDR	4	—	5	—	ns

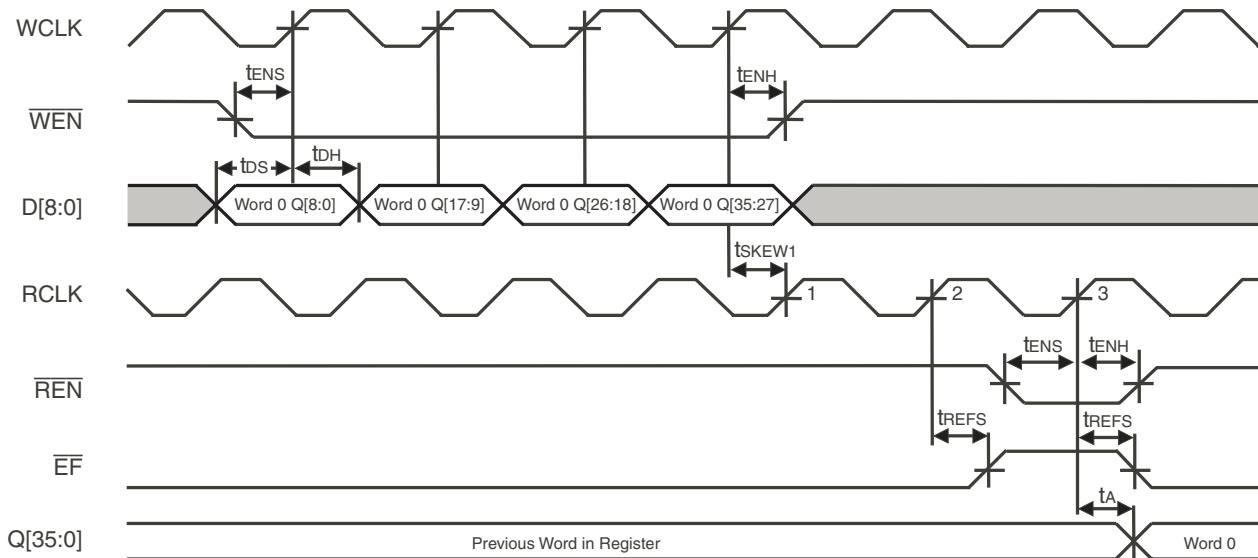


**NOTES:**

1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH after one RCLK cycle (plus tREFS). If tSKEW1 is not met, then  $\overline{EF}$  de-assertion may be delayed one extra RCLK cycle.
2. Settings:  $\overline{OE}$  = LOW, RCS = LOW, WCS = LOW, BM[3:0] = 1001, FWFT = LOW,  $\overline{ASYR}$  = HIGH, and  $\overline{ASYW}$  = HIGH.

6357 dnr33

**Figure 19. Bus-Matching Configuration - x18 In to x36 Out - IDT Standard Mode**



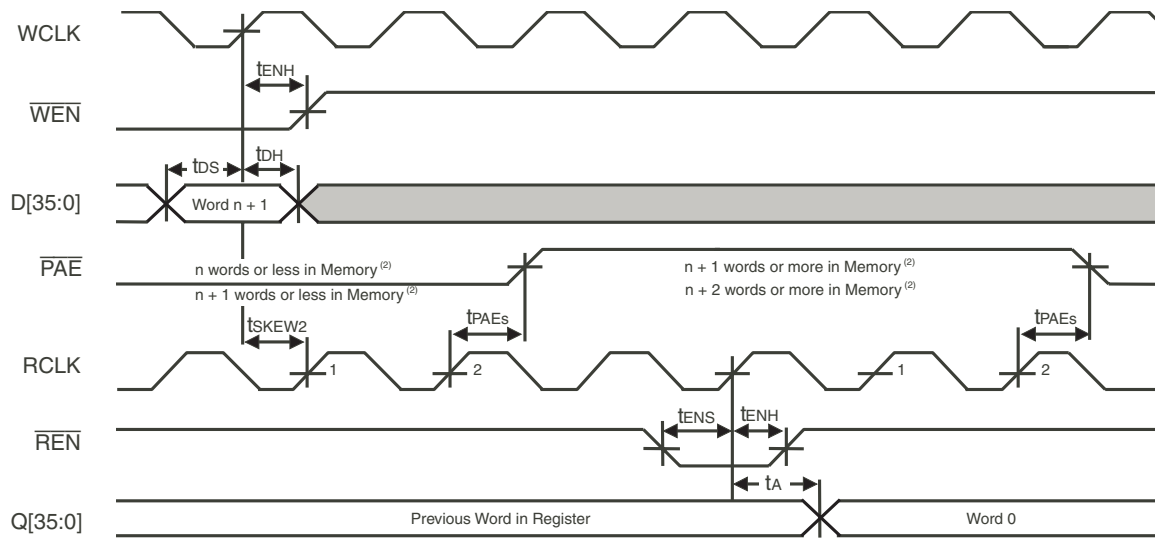
**NOTES:**

1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH after one RCLK cycle (plus tREFS). If tSKEW1 is not met, then  $\overline{EF}$  de-assertion may be delayed one extra RCLK cycle.
2. Settings:  $\overline{OE}$  = LOW, RCS = LOW, WCS = LOW, BM[3:0] = 1101, FWFT = LOW,  $\overline{ASYR}$  = HIGH, and  $\overline{ASYW}$  = HIGH.

6357 dnr34

**Figure 20. Bus-Matching Configuration - x9 In to x36 Out - IDT Standard Mode**

Symbol	Parameter	6ns		7-5ns		Unit
		Min.	Max.	Min.	Max.	
tDS	Data Setup Time	2	—	2.5	—	ns
tDH	Data Hold Time	0.5	—	0.5	—	ns
tENS	Enable Setup Time	2	—	2.5	—	ns
tENH	Enable Hold Time	0.5	—	0.5	—	ns
tA	Data Access Time	1	4	1	5	ns
tREFS	Read Clock to Synchronous $\overline{EF}/\overline{OR}$	—	4	—	5	ns
tSKEW1	Skew time between RCLK and WCLK for $\overline{EF}/\overline{OR}$ and $\overline{FF}/\overline{IR}$ in SDR	4	—	5	—	ns

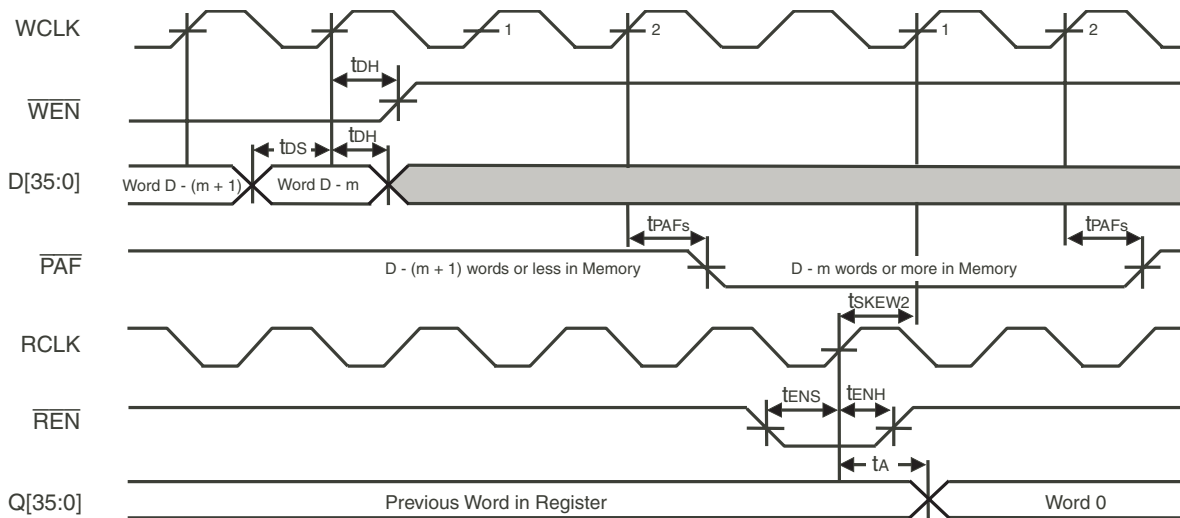


6357 drw35

**NOTES:**

1. tSKEW2 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{PAE}$  will go HIGH after one RCLK cycle (plus tPAEs). If tSKEW2 is not met, then  $\overline{PAE}$  de-assertion may be delayed one extra RCLK cycle.
2. n = PAE offset, see Table10 for information on setting PAE offset values.
3. Settings:  $\overline{OE}$  = LOW,  $\overline{RCS}$  = LOW, BM[3:0] = 1000,  $\overline{ASYR}$  = HIGH, and  $\overline{ASYW}$  = HIGH.

**Figure 21. Synchronous  $\overline{PAE}$  Flag - IDT Standard Mode and FWFT Mode**



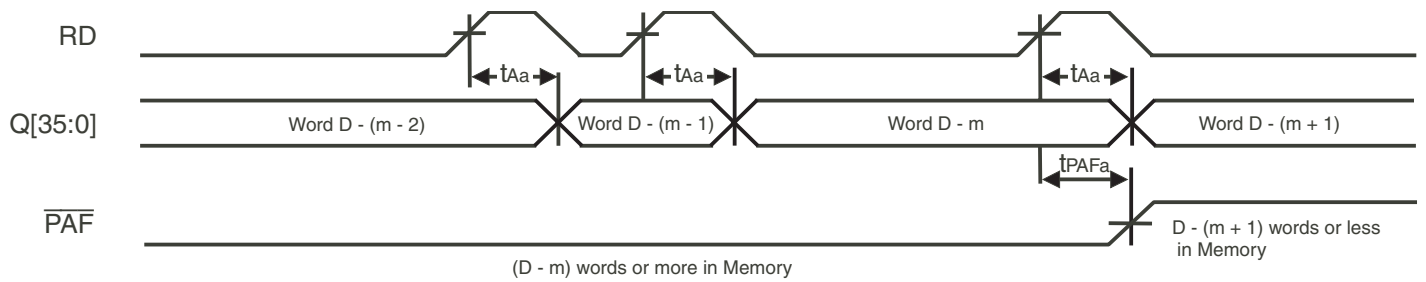
6357 drw36

**NOTES:**

1. tSKEW2 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{PAF}$  will go HIGH after one RCLK cycle (plus tPAFs). If tSKEW2 is not met, then  $\overline{PAF}$  de-assertion may be delayed one extra RCLK cycle.
2. m = PAF offset, D = density of SFC, see Table10 for information on setting PAF offset values.
3. Settings:  $\overline{OE}$  = LOW,  $\overline{RCS}$  = LOW, BM[3:0] = 1000,  $\overline{ASYR}$  = HIGH, and  $\overline{ASYW}$  = HIGH.

**Figure 22. Synchronous  $\overline{PAF}$  Flag - IDT Standard Mode and FWFT Mode**

Symbol	Parameter	6ns		7-5ns		Unit
		Min.	Max.	Min.	Max.	
tDS	Data Setup Time	2	—	2.5	—	ns
tDH	Data Hold Time	0.5	—	0.5	—	ns
tENH	Enable Hold Time	0.5	—	0.5	—	ns
tA	Data Access Time	1	4	1	5	ns
tPAFs	WCLK to Synchronous $\overline{PAF}$	—	4	—	5	ns
tPAEs	RCLK to Synchronous $\overline{PAE}$	—	4	—	5	ns
tSKEW2	Skew time between RCLK and WCLK for $\overline{PAE}/\overline{PAF}$	5	—	7	—	ns

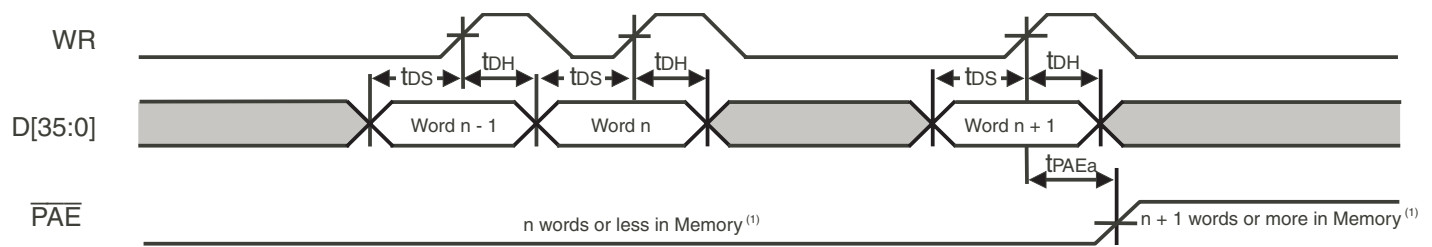


**NOTES:**

1.  $m = \overline{PAF}$  offset, see Table10 for information on  $\overline{PAF}$  offset values.  $D =$  density of SFC.
2. Settings:  $\overline{OE} = \text{LOW}$ ,  $\overline{RCS} = \text{LOW}$ ,  $BM[3:0] = 1000$ ,  $FWFT = \text{LOW}$ ,  $\overline{ASYR} = \text{LOW}$ , and  $\overline{ASYW} = \text{LOW}$ .
3. Asynchronous read is available in IDT standard mode only.

6357 drw37

**Figure 23. Asynchronous Read and  $\overline{PAF}$  Flag - IDT Standard Mode**

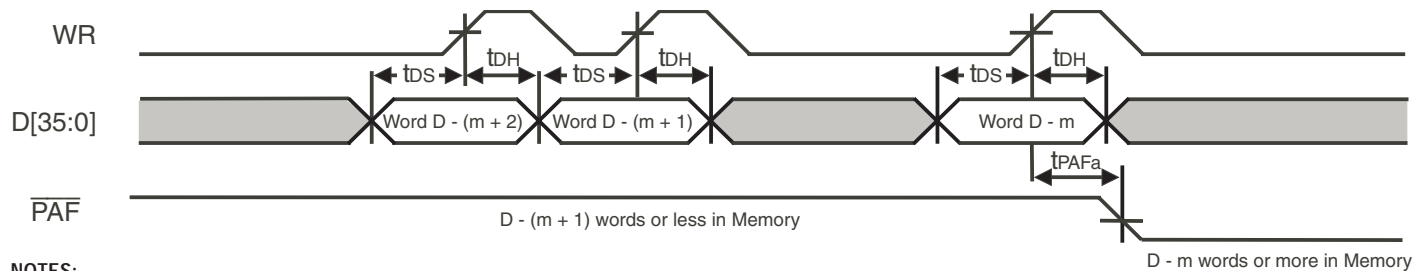


**NOTES:**

1.  $n = \overline{PAE}$  offset, see Table10 for information on  $\overline{PAE}$  offset values.
2. Settings:  $\overline{WCS} = \text{LOW}$ ,  $BM[3:0] = 1000$ ,  $FWFT = \text{LOW}$ ,  $\overline{ASYR} = \text{LOW}$ , and  $\overline{ASYW} = \text{LOW}$ .
3. Asynchronous read is available in IDT standard mode only.

6357 drw38

**Figure 24. Asynchronous Write and  $\overline{PAE}$  Flag - IDT Standard Mode**



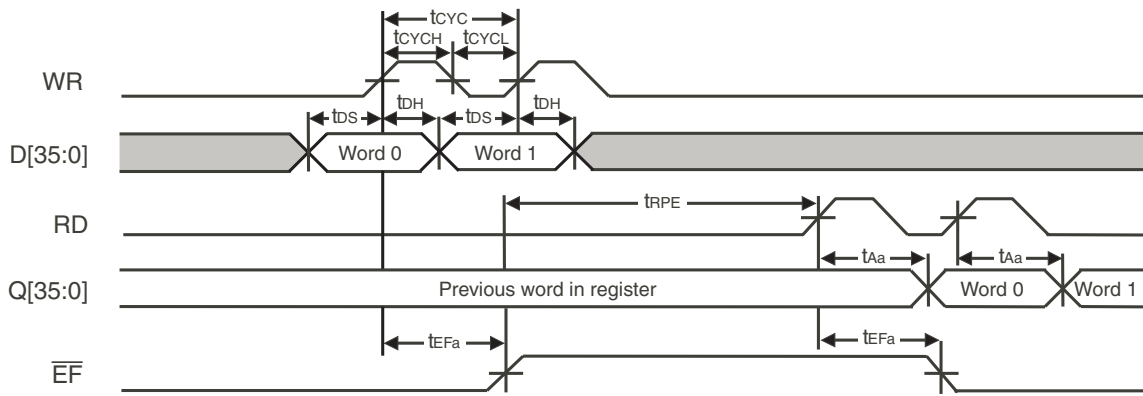
**NOTES:**

1.  $m = \overline{PAF}$  offset, see Table10 for information on  $\overline{PAF}$  offset values.  $D =$  density of SFC.
2. Settings:  $\overline{WCS} = \text{LOW}$ ,  $BM[3:0] = 1000$ ,  $FWFT = \text{LOW}$ ,  $\overline{ASYR} = \text{LOW}$ , and  $\overline{ASYW} = \text{LOW}$ .
3. Asynchronous read is available in IDT standard mode only.

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**Figure 25. Asynchronous Write and  $\overline{PAF}$  Flag - IDT Standard Mode**

Symbol	Parameter	6ns		7-5ns		Unit
		Min.	Max.	Min.	Max.	
tDS	Data Setup Time	2	—	2.5	—	ns
tDH	Data Hold Time	0.5	—	0.5	—	ns
tAa	Data Access Time	0.6	8	0.6	10	ns
tPAFa	Rising Edge to $\overline{PAF}$	—	8	—	10	ns

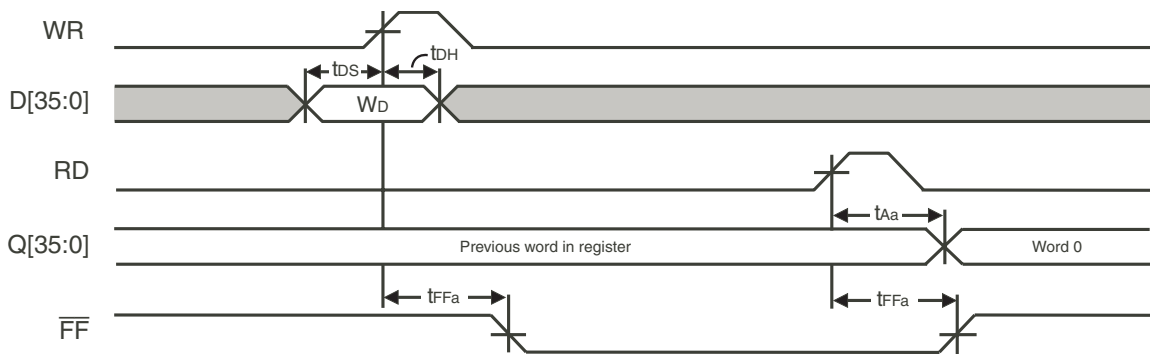


6357 drw40

**NOTES:**

1. Settings:  $\overline{OE} = \text{LOW}$ ,  $\overline{RCS} = \text{LOW}$ ,  $\overline{WCS} = \text{LOW}$ ,  $\overline{FWFT} = \text{LOW}$ ,  $\overline{ASYR} = \text{LOW}$ , and  $\overline{ASYW} = \text{LOW}$ .
2. Asynchronous read is available in IDT standard mode only.

**Figure 26. Asynchronous Empty Boundary - IDT Standard Mode**

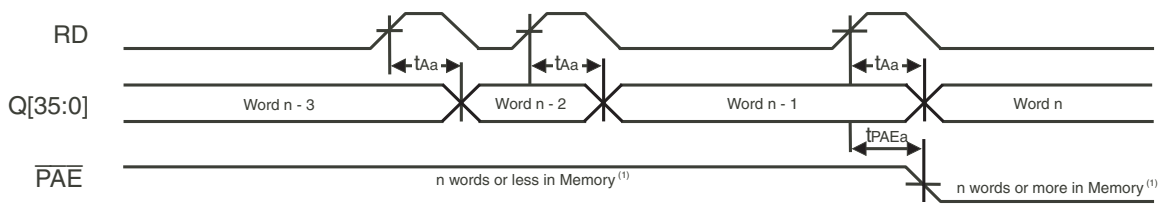


6357 drw41

**NOTES:**

1. Settings:  $\overline{OE} = \text{LOW}$ ,  $\overline{RCS} = \text{LOW}$ ,  $\overline{WCS} = \text{LOW}$ ,  $\overline{FWFT} = \text{LOW}$ ,  $\overline{ASYR} = \text{LOW}$ , and  $\overline{ASYW} = \text{LOW}$ .
2. Asynchronous read is available in IDT standard mode only.

**Figure 27. Asynchronous Full Boundary - IDT Standard Mode**



6357 drw42

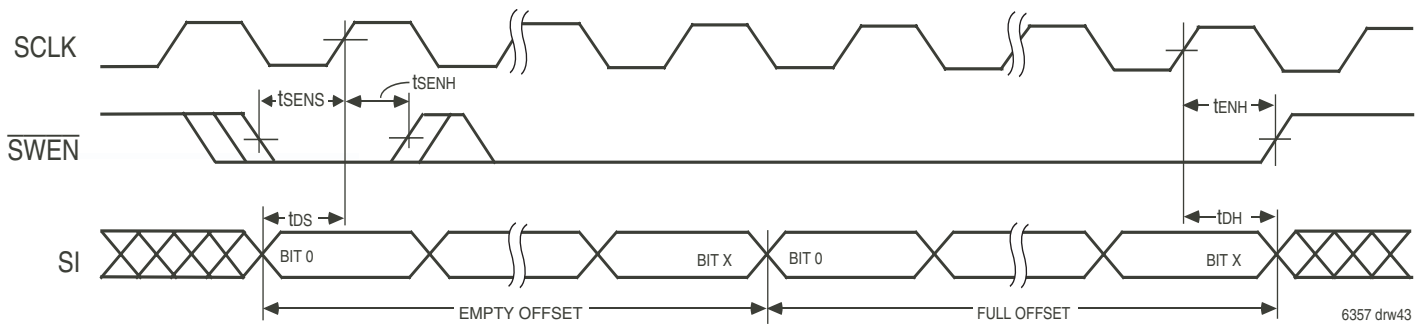
**NOTES:**

1. n =  $\overline{PAE}$  offset, see Table10 for information on  $\overline{PAE}$  offset values.
2. Asynchronous read is available in IDT standard mode only.

**Figure 28. Asynchronous Read and  $\overline{PAE}$  Flag - IDT Standard Mode**

Symbol	Parameter	6ns		7-5ns		Unit
		Min.	Max.	Min.	Max.	
tAa	Data Access Time	0.6	8	0.6	10	ns
tcyc	Cycle Time	10	—	12	—	ns
tcych	Cycle HIGH Time	4.5	—	5	—	ns
tcycl	Cycle LOW Time	4.5	—	5	—	ns
tdh	Data Hold Time	0.5	—	0.5	—	ns
tds	Data Setup Time	2	—	2.5	—	ns
tEFa	Rising Edge to $\overline{EF}$	—	8	—	10	ns
tFFa	Rising Edge to $\overline{FF}$	—	8	—	10	ns
tPAEa	Rising Edge to $\overline{PAE}$	—	8	—	10	ns
trPE	Read Pulse after $\overline{EF}$ HIGH	8	—	10	—	ns

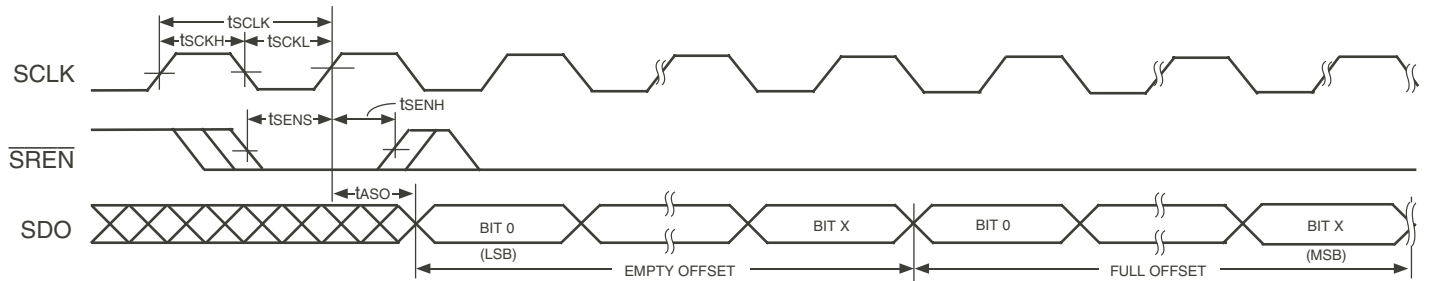




**NOTES:**

- Settings: JSEL = LOW.
- x is the required number of bits to program the  $\overline{\text{PAE}}$  and  $\overline{\text{PAF}}$  offset registers. See Table 5 for the numbers based on the values external configurations.

**Figure 29. Serial Loading of Programmable Flag Registers (IDT Standard and FWFT Modes)**

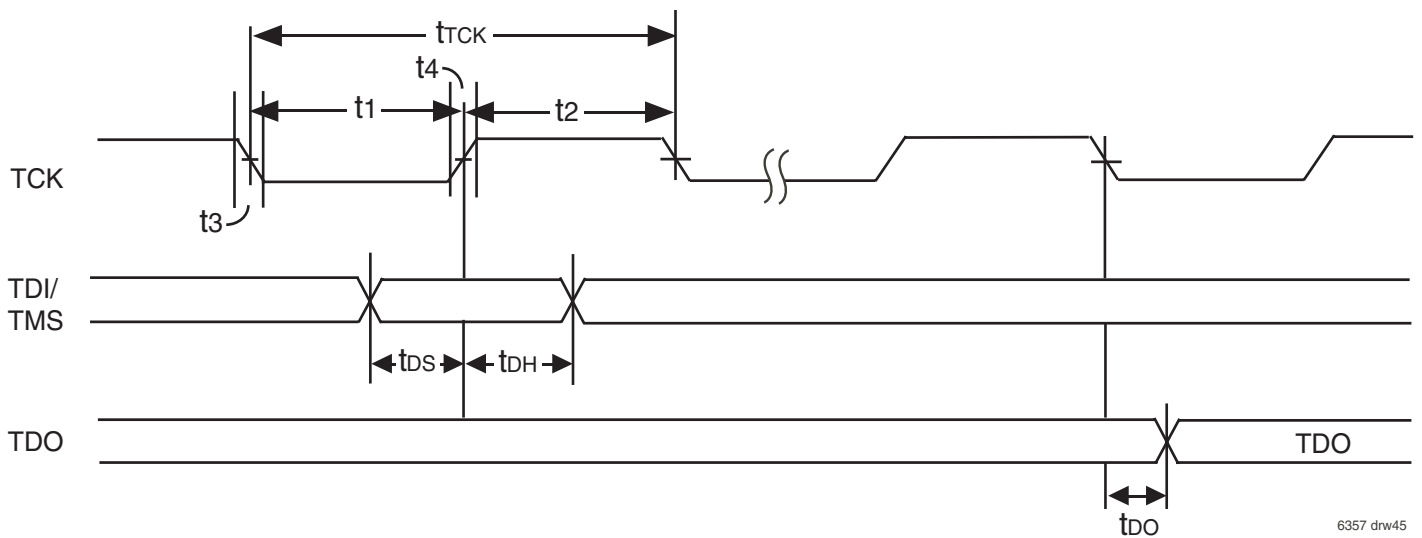


**NOTES:**

- Settings: JSEL = LOW.
- x is the required number of bits to program the  $\overline{\text{PAE}}$  and  $\overline{\text{PAF}}$  offset registers. See Table 5 for the numbers based on the values external configurations.

**Figure 30. Reading of Programmable Flag Registers (IDT Standard and FWFT Modes)**

Symbol	Parameter	6ns		7-5ns		Unit
		Min.	Max.	Min.	Max.	
tDH	Data Hold Time	0.5	—	0.5	—	ns
tDS	Data Setup Time	2	—	2.5	—	ns
tASO	Serial Output Data Access Time	—	20	—	20	ns
tSENS	Serial Enable Setup	5	—	5	—	ns
tSENH	Serial Enable Hold	5	—	5	—	ns
tSCLK	Serial Clock Cycle	10	—	10	—	ns
tSCLKH	Serial Clock HIGH	45	—	45	—	ns
tSCLKL	Serial Clock LOW	45	—	45	—	ns



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Notes to diagram:  
 t1 = tTCKLOW  
 t2 = tTCKHIGH  
 t3 = tTCKFALL  
 t4 = tTCKRISE

Figure 31. Standard JTAG Timing

**SYSTEM INTERFACE PARAMETERS**

Parameter	Symbol	Test Conditions	IDT72T6360		
			Min.	Max.	Units
Data Output	tDO <sup>(1)</sup>		-	20	ns
Data Output Hold	tDOH <sup>(1)</sup>		0	-	ns
Data Input	tDS	t <sub>rise</sub> =3ns	10	-	ns
	tDH	t <sub>fall</sub> =3ns	10	-	ns

NOTE:  
 1. 50pf loading on external output signals.

**JTAG  
 AC ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = 2.5V ± 5%; Tambient (Industrial) = 0°C to +85°C)

Parameter	Symbol	Test Conditions			
			Min.	Max.	Units
JTAG Clock Input Period	tCK	-	100	-	ns
JTAG Clock HIGH	tCKHIGH	-	40	-	ns
JTAG Clock Low	tCKLOW	-	40	-	ns
JTAG Clock Rise Time	tCKRISE	-	-	5 <sup>(1)</sup>	ns
JTAG Clock Fall Time	tCKFALL	-	-	5 <sup>(1)</sup>	ns

NOTE:  
 1. Guaranteed by design.

## JTAG TIMING SPECIFICATIONS (IEEE 1149.1 COMPLIANT)

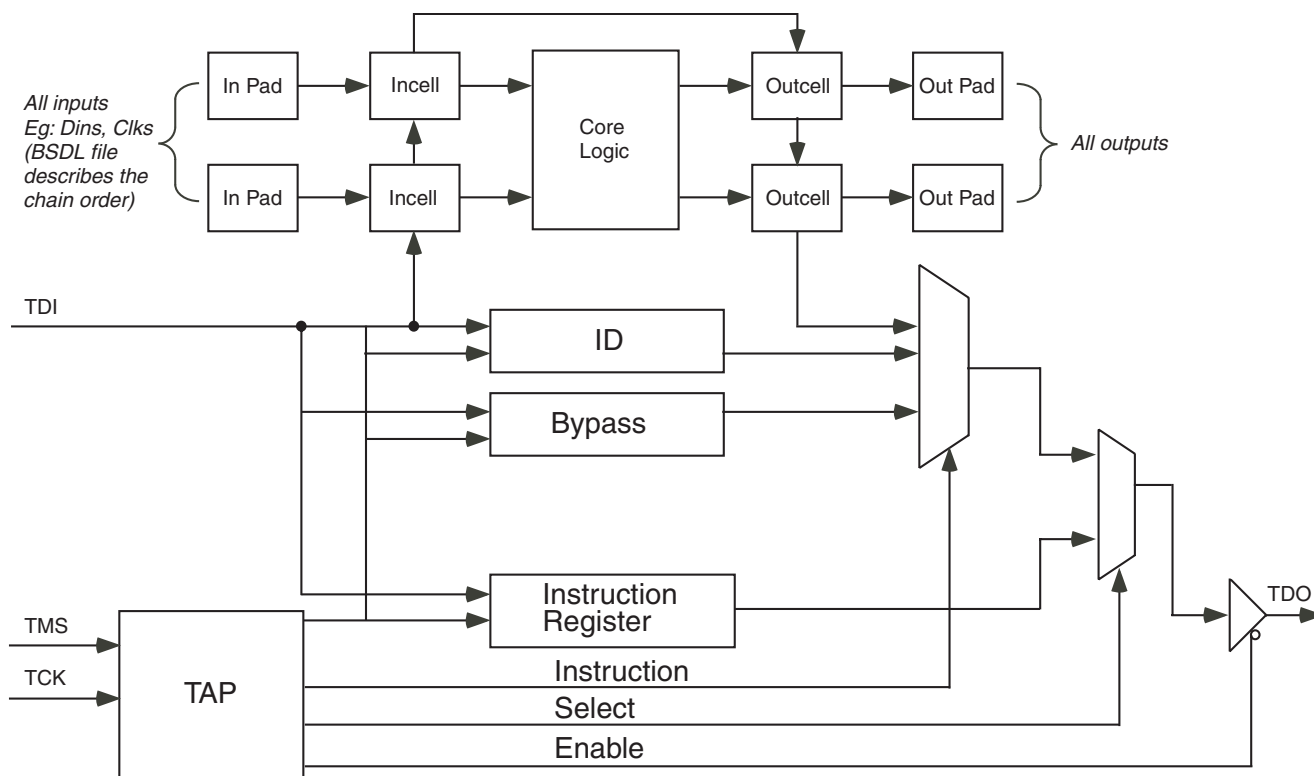
The JTAG test port in this device is fully compliant with the IEEE Standard Test Access Port (IEEE 1149.1) specifications. Four additional pins (TDI, TDO, TMS and TCK) are provided to support the JTAG boundary scan interface. Note that IDT provides appropriate Boundary Scan Description Language program files for these devices.

The Standard JTAG interface consists of seven basic elements:

- Test Access Port (TAP)
- TAP controller
- Instruction Register (IR)
- Data Register Port (DR)
- Bypass Register (BYR)
- ID Code Register

The following sections provide a brief description of each element. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

The Figure below shows the standard Boundary-Scan Architecture



6357 drw46

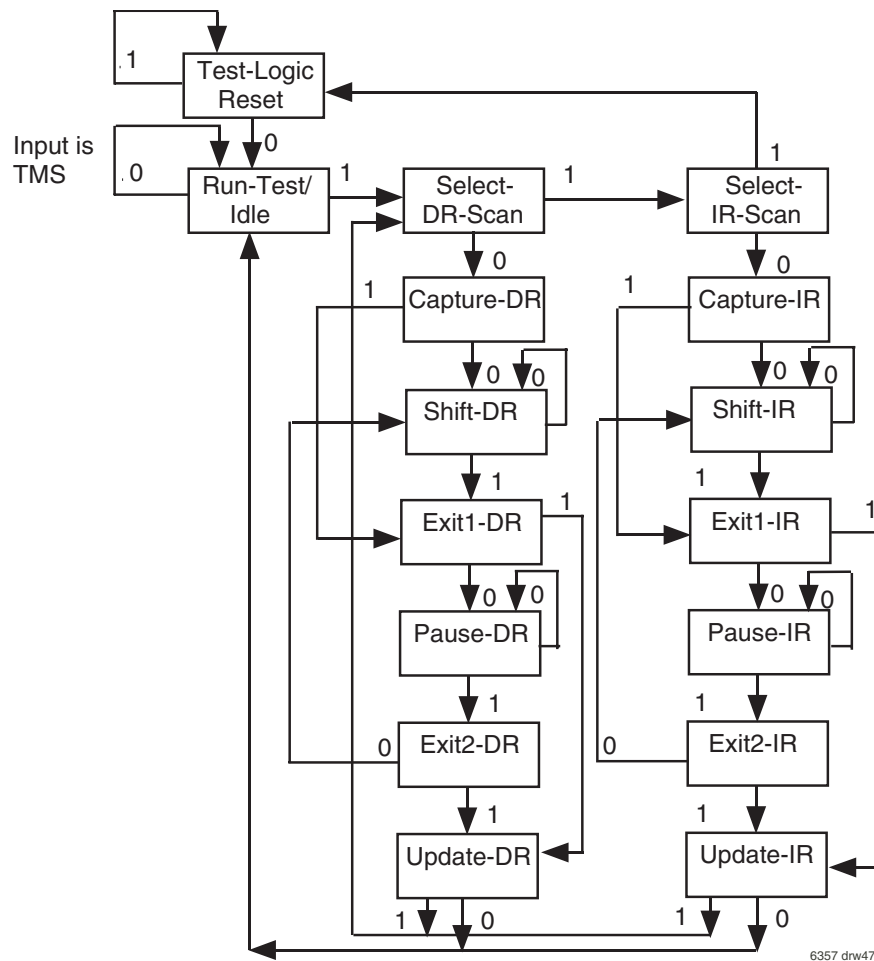
Figure 32. JTAG Architecture

### TEST ACCESS PORT (TAP)

The TAP interface is a general-purpose port that provides access to the internal JTAG state machine. It consists of three input ports (TCLK, TMS, TDI) and one output port (TDO).

### THE TAP CONTROLLER

The TAP controller is a synchronous finite state machine that responds to TMS and TCLK signals to generate clock and control signals to the Instruction and Data Registers for capture and updating of data passed through the TDI serial input.



- NOTES:
- Five consecutive 1's at TMS will reset the TAP.
  - TAP controller resets automatically upon power-up.

Figure 33. TAP Controller State Diagram

Refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1) for the full state diagram

All state transitions within the TAP controller occur at the rising edge of the TCLK pulse. The TMS signal level (0 or 1) determines the state progression that occurs on each TCLK rising edge.

**Test-Logic-Reset** All test logic is disabled in this controller state enabling the normal operation of the IC. The TAP controller state machine is designed in such a way that, no matter what the initial state of the controller is, the Test-Logic-Reset state can be entered by holding TMS at high and pulsing TCK five times.

**Run-Test-Idle** In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it will be executed when the controller enters this state. The test logic in the IC is idle otherwise.

**Select-DR-Scan** This is a controller state where the decision to enter the Data Path or the Select-IR-Scan state is made.

**Select-IR-Scan** This is a controller state where the decision to enter the Instruction Path is made. The Controller can return to the Test-Logic-Reset state otherwise.

**Capture-IR** In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits are always required to be "01".

**Shift-IR** In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register. TDO changes on the falling edge of TCK.

**Exit1-IR** This is a controller state where a decision to enter either the Pause-IR state or Update-IR state is made.

**Pause-IR** This state is provided in order to allow the shifting of instruction register to be temporarily halted.

**Exit2-DR** This is a controller state where a decision to enter either the Shift-IR state or Update-IR state is made.

**Update-IR** In this controller state, the instruction in the instruction register scan chain is latched into the register of the Instruction Register on every falling edge of TCK. This instruction also becomes the current instruction once it is latched.

**Capture-DR** In this controller state, the data is parallel loaded in to the data registers selected by the current instruction on the rising edge of TCK.

**Shift-DR, Exit1-DR, Pause-DR, Exit2-DR and Update-DR** These controller states are similar to the Shift-IR, Exit1-IR, Pause-IR, Exit2-IR and Update-IR states in the Instruction path.

## THE INSTRUCTION REGISTER

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

## TEST DATA REGISTER

The Test Data register contains three test data registers: the Bypass, the Boundary Scan register and Device ID register.

These registers are connected in parallel between a common serial input and a common serial data output.

The following sections provide a brief description of each element. For a complete description, refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

## TEST BYPASS REGISTER

The register is used to allow test data to flow through the device from TDI to TDO. It contains a single stage shift register for a minimum length in the serial path. When the bypass register is selected by an instruction, the shift register stage is set to a logic zero on the rising edge of TCLK when the TAP controller is in the Capture-DR state.

The operation of the bypass register should not have any effect on the operation of the device in response to the BYPASS instruction.

## THE BOUNDARY-SCAN REGISTER

The boundary-scan register (BSR) contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

## THE DEVICE IDENTIFICATION REGISTER

The Device Identification Register is a Read Only 32-bit register used to specify the manufacturer, part number and version of the device to be determined through the TAP in response to the IDCODE instruction.

IDT JEDEC ID number is 0xB3. This translates to 0x33 when the parity is dropped in the 11-bit Manufacturer ID field.

For the IDT72T6360, the Part Number field contains the following values:

Device	Part# Field
IDT72T6360	0437 (hex)

31(MSB)	28 27	12 11	1 0(LSB)
Version (4 bits) 0000	Part Number (16-bit)	Manufacturer ID (11-bit) 0033 (hex)	1

IDT72T6360 JTAG Device Identification Register

## JTAG INSTRUCTION REGISTER

The Instruction register allows an instruction to be serially input into the device when the TAP controller is in the Shift-IR state. The instruction is decoded to perform the following:

- Select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and the selected data register.
- Define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

The Instruction Register is a 4 bit field (i.e. IR3, IR2, IR1, IR0) to decode 16 different possible instructions. Instructions are decoded as follows.

Hex Value	Instruction	Function
0000	EXTEST	Test external pins
0001	SAMPLE/PRELOAD	Select boundary scan register
0002	IDCODE	Selects chip identification register
0003	CLAMP	Fix the output chains to scan chain values
0004	HIGH-IMPEDANCE	Puts all outputs in high-impedance state
000F	BYPASS	Select bypass register
	Private	Several combinations are private (for IDT internal use). Do not use codes other than those identified above.

## JTAG INSTRUCTION REGISTER DECODING

The following sections provide a brief description of each instruction. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

### EXTEST

The required EXTEST instruction places the device into an external boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data off-chip via the boundary outputs and receive test data off-chip via the boundary inputs. As such, the EXTEST instruction is the workhorse of IEEE Std 1149.1, providing for probe-less testing of solder-joint opens/shorts and of logic cluster function.

### SAMPLE/PRELOAD

The required SAMPLE/PRELOAD instruction allows the device to remain in a normal functional mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register can be accessed via a data scan operation, to take a sample of the functional data entering and leaving the device. This instruction is also used to preload test data into the boundary-scan register before loading an EXTEST instruction.

### IDCODE

The optional IDCODE instruction allows the device to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. The device identification register is a 32-bit shift register containing information regarding the device manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the device. Also, access to the device identification register should be immediately available, via a TAP data-scan operation, after power-up of the device or by otherwise moving to the Test-Logic-Reset state.

### CLAMP

The optional CLAMP instruction sets the outputs of an device to logic levels determined by the contents of the boundary-scan register and selects the one-bit bypass register to be connected between TDI and TDO. Before loading this instruction, the contents of the boundary-scan register can be preset with the SAMPLE/PRELOAD instruction. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the outputs.

### HIGH-IMPEDANCE

The optional High-Impedance instruction sets all outputs (including two-state as well as three-state types) of an device to a disabled (high-impedance) state

and selects the one-bit bypass register to be connected between TDI and TDO. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the device outputs.

### BYPASS

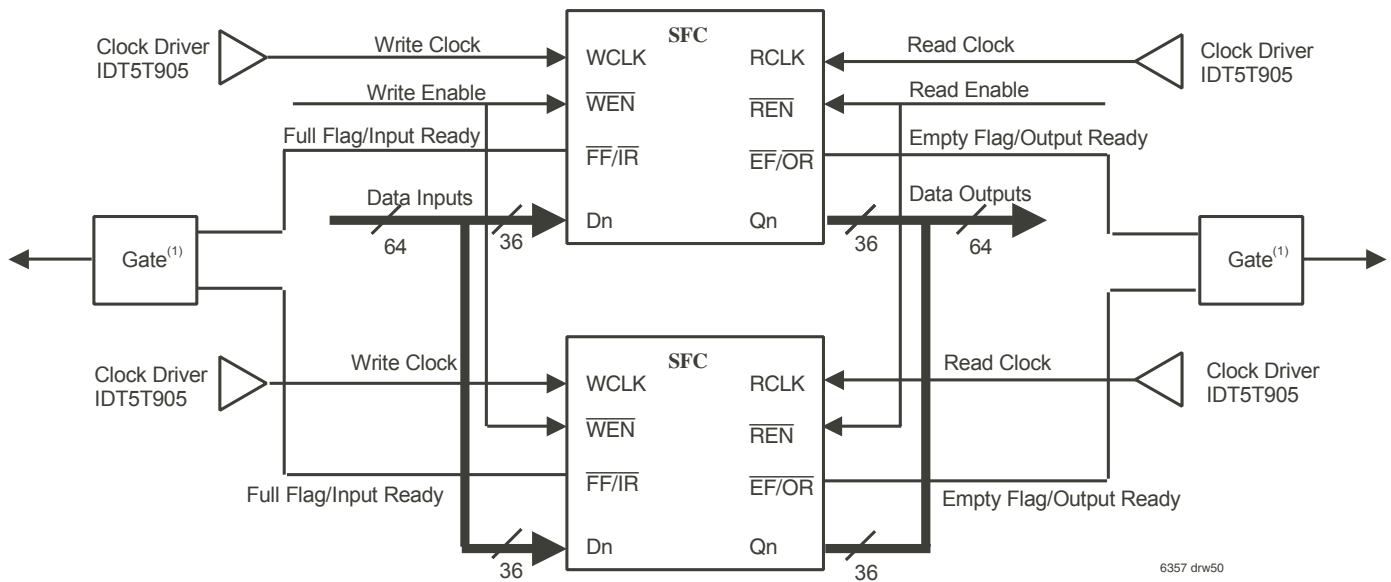
The required BYPASS instruction allows the device to remain in a normal functional mode and selects the one-bit bypass register to be connected between TDI and TDO. The BYPASS instruction allows serial data to be transferred through the IC from TDI to TDO without affecting the operation of the device.



## WIDTH EXPANSION CONFIGURATION

The sequential flow-control (SFC) device can be connected with another SFCs in width expansion to support bus-widths greater than 36-bits. This configuration connects the input and output bus of two devices together to create a wider bus. The read and write clocks for each device are driven with a clock driver. The empty and full flags of both devices are connected to a logic gate (AND/OR) depending on whether IDT Standard mode or FWFT mode is selected. Because of the variation in skew between the read clock and write

clock, it is possible for  $\overline{EF}/\overline{FF}$  deassertion and  $\overline{IR}/\overline{OR}$  assertion to vary from one cycle between the devices. The logic gate connected to the status flags will create a composite flag that will update the status of both SFC devices to represent a more accurate status of the configuration. To minimize the skew between the two write and read clocks, a clock driver (IDT5T905 recommended) is used to drive the input clocks for both SFC devices. Figure 36 illustrates the width expansion configuration.



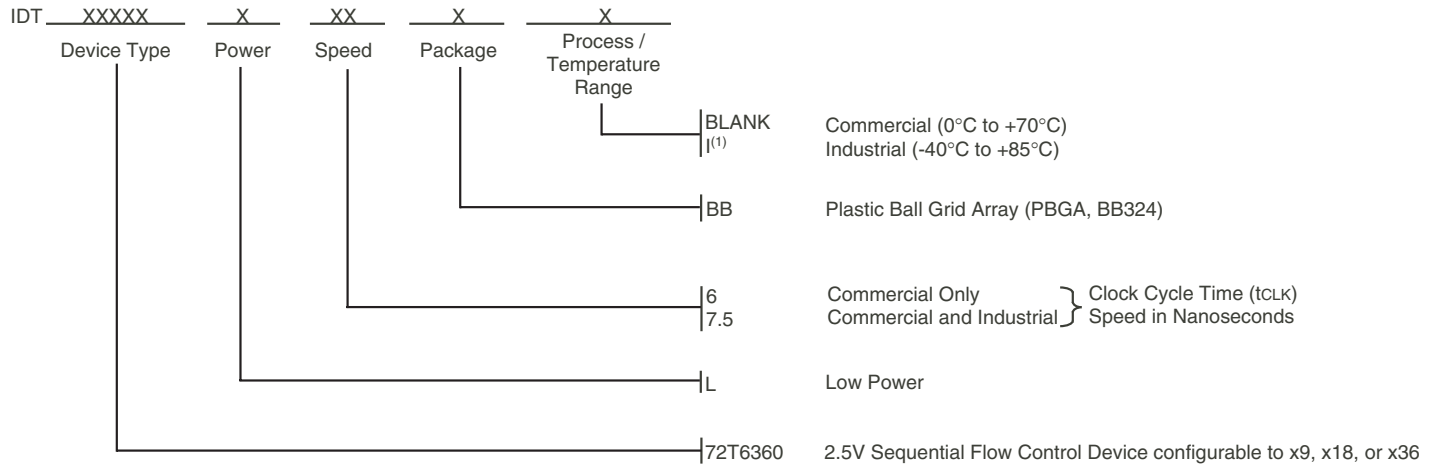
### NOTES:

1. Use an AND gate in IDT Standard mode, an OR gate in FWFT mode.
2. Do not connect any output signals directly together.

Figure 36. Width Expansion Configuration in IDT Standard Mode and FWFT Mode



## ORDERING INFORMATION



6357 drwlast



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