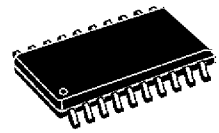
SGS-THOMSON MICROELECTRONICS

L9864

ABS AND ISO/SDL INTERFACE

- THREE HYSTERESIS COMPARATORS WITH LOW INPUT CURRENTS, FIXED THRESHOLD VOLTAGES AND INTEGRATED OUTPUT PULL-UP RESISORS.
- DIAGNOSTIC INTERFACE CIRCUIT WITH SUPPLY VOLTAGE DEPENDENT INPUT THRESHOLDS AND PROTECTED OPEN COLLECTOR OUTPUT
- EXTERNALLY PROGRAMMABLE ISO OR SDL FUNCTION FOR THE DIAGNOSTIC
- INVERTER CONTROL COMPARATORS WITH INTERNAL INPUT PULL-UP RESISTORS
- TWO PRECISION CLAMPING CIRCUITS
- ALL INPUTS AND OUTPUTS PROTECTED AGAINST ESD
- THERMAL SHUTDOWN FUNCTION FOR THE K DIAGNOSTIC OUTPUT



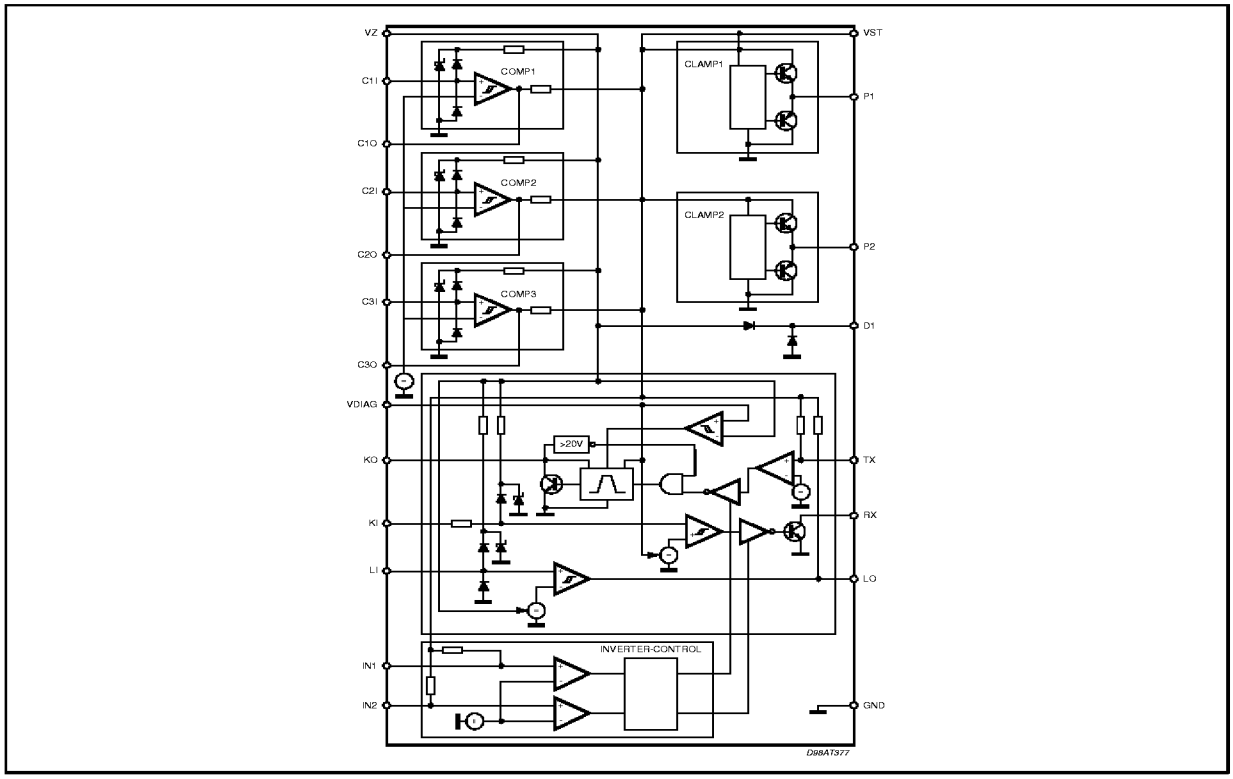
SO20L

ORDERING NUMBER: L9864D

DESCRIPTION

The L9864 is a monolithic integrated circuit containing ABS and a programmable ISO/SDL interface function

BLOCK DIAGRAM

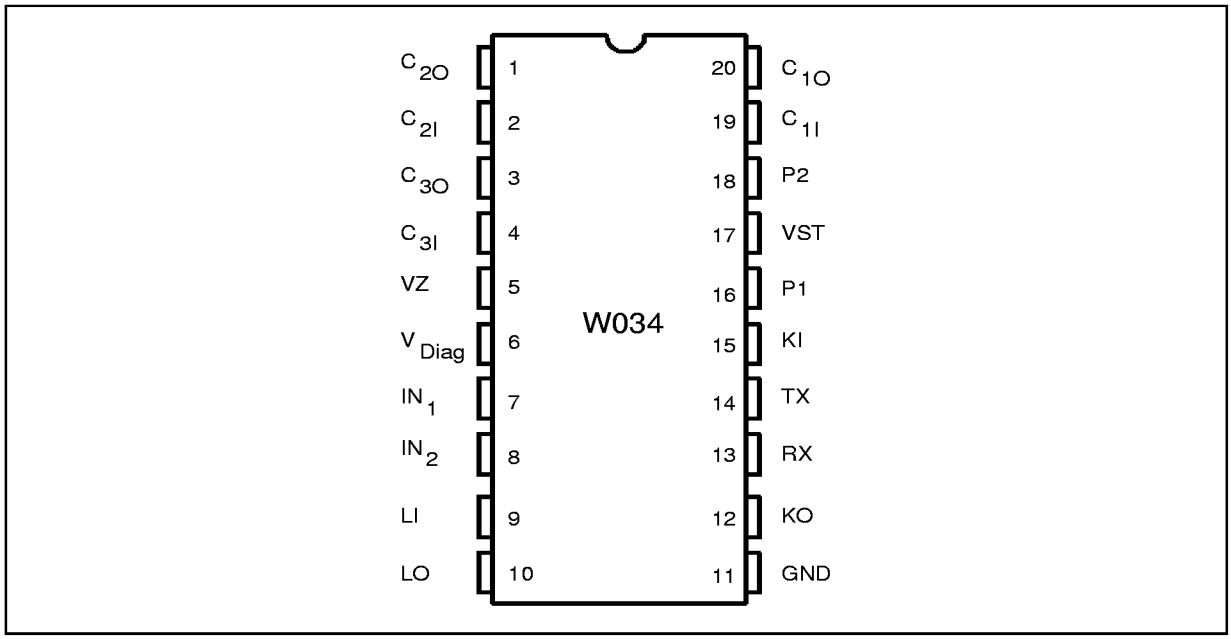


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Value	Unit
V_z, V_{Diag}	Board Voltage	Continuous (DC)	0 to 20	V
		$0 < t_p \leq 5min$; Tj = -40 to80°C	26.5	V
		$t_p \leq 2s$	-1.5	V
		$0 < t_p \leq 200ms$; $f \leq 0.06Hz$; $n \leq 360$ cycles	40	V
		$0 < t_p \leq 50ms$; $f_p \leq 1Hz$; $n \leq 36000$ cycles	40	V
dV_z/dt, dV_{Diag}/dt		Vz = 6 to 16V	10	V/µs
V_{st}	Stabilized Voltage		0 to 6	V
T_{stg}	Storage Temperature	continuous	-55 to 150	°C
T_j	Junction Temperature	continuous $\sum t_p < 100h$ $t_p < 10ms$	-55 to 150 170 180	°C °C °C
$V_{KO, KI}$		positive transient (1)	50	V

Note 1: according to ISO TR 7637/1; the transient will be clamped with external circuitry.

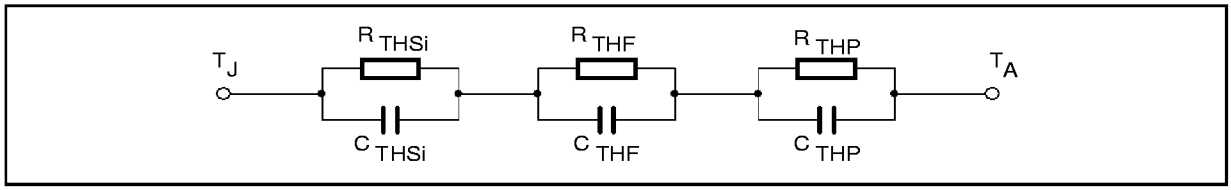
PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance Junction ambient SO20 (mounted on board)	max 80	K/W
T_{jTSD}	Thermal Protection threshold Junction Temperature	150 to 180	°C

Equivalent Circuit Diagram of the Thermal Impedance Junction to Ambient



Si = silicon and die attach
F = frame
P = remaining package mass

$$t_{HD} = \frac{1}{R_{TH} \cdot C_{TH}}$$

The typical values for SO20 package are:

R_{THSI}	=	1.5KW	TTHSI	=	2ms
R_{THF}	=	15KW	T_{THF}	=	20ms
R_{THP}	=	60KW	T_{THP}	=	50s

ELECTRICAL CHARACTERISTICS (Operating Range)
The electrical characteristics are valid within the below defined operating range, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_Z			6	12	16	V
V_{Diag}			4.75		16	V
V_{ST}			4.75	5	5.25	V
T_{amb}	Ambient Temperature	hybrid ass. chip	-40		125	°C
t_B	Useful Life Time	$V_z = V_{ST} = V_{Diag} = 0V$	15			years
t_b	Operating Life Time	$V_z = V_{ST} = V_{Diag}$ nominal values; $T_{amb} = 55°C$	4500			hours
Comparators (Comp 1, Comp 2, Comp 3)						
V_{C1IL}	Input Voltage Low State	V_{C10} = (LOW); $\lvert I_{C1} \rvert \leq 10mA$			2	V
V_{C2IL}		V_{C20} = (LOW); $\lvert I_{C2} \rvert \leq 10mA$			2	V
V_{C3IL}		V_{C30} = (LOW); $\lvert I_{C3} \rvert \leq 10mA$			2	V
V_{C1IH}	Input Voltage	V_{C10} = (HIGH); $\lvert I_{C1} \rvert \leq 10mA$	2.8			V
V_{C2IH}		V_{C20} = (HIGH); $\lvert I_{C2} \rvert \leq 10mA$	2.8			V
V_{C3IH}		V_{C30} = (HIGH); $\lvert I_{C3} \rvert \leq 10mA$	2.8			V
V_{C1Ih}	Input Threshold Level Hysteresis		0.08	0.2	0.4	V
V_{C2Ih}			0.08	0.2	0.4	V
V_{C3Ih}			0.08	0.2	0.4	V
$\lvert I_{C1L} \rvert$ $\lvert I_{C2L} \rvert$ $\lvert I_{C3L} \rvert$	Input Currents	$0 \leq V_{C1I}, V_{C2I}, V_{C3I}, \leq V_z - 0.5V$ $V_z, \leq 16V$			400	nA
		$0 \leq V_{C1I}, V_{C2I}, V_{C3I}, \leq V_z$; $V_z, \leq 16V$			5	µA
V_{C1} V_{C2} V_{C3}	Input Voltage During Clamp	$\lvert I_{C1, 2, 3} \rvert = 10mA$			30	V
		$\lvert I_{C1, 2, 3} \rvert = -10mA$	-1.5			V
V_{C10L}	Output Saturation Voltage	V_{C1I} = (LOW); $\lvert I_{C10} \rvert \leq 3mA$			0.4	V
V_{C20L}		V_{C2I} = (LOW); $\lvert I_{C20} \rvert \leq 3mA$			0.4	V
V_{C30L}		V_{C3I} = (LOW); $\lvert I_{C30} \rvert \leq 3mA$			0.4	V
I_{C10L}	Output Short Circuit	$V_{C10} = V_{C20} = V_{C30} = 6V$; no damage		10		mA
I_{C20L}				10		mA
I_{C30L}				10		mA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{C10H}	Output Voltage High State	$10M\Omega \leq R_{LC10}$	V_{ST}-0.25	V_{ST}-0.1	V_{ST}	V
V_{C20H}		$10M\Omega \leq R_{LC20}$	V_{ST}-0.25	V_{ST}-0.1	V_{ST}	V
V_{C30H}		$10M\Omega \leq R_{LC30}$	V_{ST}-0.25	V_{ST}-0.1	V_{ST}	V
R_A	Comparator Output Pull-Up Resistor	Output Status = (HIGH); $-0.3 \leq V_{C10}, V_{C20}, V_{C30} \leq 25V$	7	10	18	KΩ
$f_{TC1,2,3}$	Transmission Frequency	$C_{L1}, C_{L2}, C_{L3} \leq 20pF$ (external load capacitors)	200			KHz
$t_{1C1,2,3}$	Off Delay Time	$V_{C1l}, V_{C2l}, V_{C3l}, =$ -1 to 16V			1.5	µs
$t_{2C1,2,3}$	On Delay Time	$\lvert I_{C1,2,3} \rvert \leq 10mA$ for the definition of t_1, t_2 see fig.1			1.0	µs
Δt_{1-2}	On Off Delay Time Difference	$\lvert t_{1C}, t_{2C} \rvert_{1,2,3}$			1.0	µs
$\lvert I_{P1DC} \rvert$ $\lvert I_{P2DC} \rvert$	DC Input Currents	$V_{P1} = 0$; $V_{P2} = 0$			10	µs
		$V_{P1,P2} = V_{ST}$			25	µA
		$50mV \leq V_{P1} \leq V_{ST}$ -50mV $50mV \leq V_{P2} \leq V_{ST}$ -50mV			5	µA
		$500mV \leq V_{P1} \leq V_{ST}$ -500mV $500mV \leq V_{P2} \leq V_{ST}$ -500mV			2	µA
V_{P1DC} V_{P2DC}		$I_{P1,2} = 10mA$			V_{ST}+200	V
		$I_{C1,2} = -10mA$	-200			mV
V_{P1TR} V_{P2TR}	Dynamic overshoot (with respect to 0 or VST)	Input pulse specific. Ri = 10KΩ; $V_{P1} = \pm 100V$; $t_r = 10ns$; $t_f = 100ns$; within a max. overshoot time $t_o \leq 20ns$, higher overshoot value is possible. *1	-300		300	mV
V_{KIL}	Input Voltage Low State	Output Status Low $4.75V \leq V_{Diag} \leq 5.25V$ 1)			2.0	V
		$6V \leq V_{Diag} \leq 20V$ 2) $\lvert I_{KI} \rvert \leq 10mA$			$0.4V_{Diag}$	V
		Output Status Low $20V \leq V_{Diag} \lvert I_{KI} \rvert \leq 10mA$			8	V
V_{KIH}	Input Voltage High State	Output Status High $4.75V \leq V_{Diag} \leq 5.25V$ 1)	2.9			V
		$6V \leq V_{Diag} \leq 20V$ 2) $\lvert I_{KI} \rvert \leq 10mA$	$0.6V_{Diag}$			V
		Output Status High $20V \leq V_{Diag}$ 2) $\lvert I_{KI} \rvert \leq 10mA$	12			V
V_{KIh}	Input Threshold Hysteresis		0.08	0.2	0.4	V
V_{KICL}	Input Voltage During Clamp	$I_{KICL} = 10mA$	50			V
		$I_{KICL} = -10mA$	-1.5			V
$\lvert I_{KI} \rvert$	Input Current	$0 \leq V_{KI} \leq 16V$			3	µA
R_{KI}	Equivalent Input Resistor $6V \leq V_{KL} \leq 16V$	$GND \leq V_Z \leq V_{KI}$; $6V \leq V_Z \leq 16V$	200			KΩ
		V_Z = GND	50			KΩ
		V_Z = open	50			KΩ

* 1 Guaranteed by design. Not feasible to check on ATE.

1) according to SDL specification

2) according to ISO specification

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{LIL}	Input Voltage Low State	Output Status = LOW; $\|I_{L1}\| \leq$ 10mA; $6V \leq V_Z \leq 16V$			$0.4V_Z$	V
		Output Status = LOW; $\|I_{L1}\| \leq$ 10mA; $20V \leq V_Z$			8	V
V_{LIH}	Input Voltage High State	Output Status = HIGH; $\|I_{L1}\| \leq$ 10mA; $6V \leq V_Z \leq 20V$	$0.6V_Z$			V
		Output Status = HIGH; $\|I_{L1}\| \leq$ 10mA; $20V \leq V_Z$	12			V
V_{LIh}	Input Threshold hysteresis		0.08	0.2	0.4	V
$\|I_{LI}\|$	Input Current	0V â $V_{LI} \leq$ 16V			3	µA
V_{LI}	Input Voltage During Clamp	ILI = 10mA			30	V
		I_{LI} = -10mA	-1.5			V
R_{LI}	Equivalent Input Resistor 6V â $V_{LI} \leq$ 16V	$GND \leq V_Z \leq V_{LI}$; $6V \leq V_Z \leq 16V$	200			KΩ
		V_Z = GND	50			KΩ
		V_Z = OPEN	50			KΩ
V_{TXL}	Input Voltage Low State		-0.15		1	V
V_{TXH}	Input Voltage High State		2		V_{ST}+0.15	V
R_E	Input Resistors at TX	$0.15V \leq V_{TX} \leq V_{ST}$ +0.15V	14	20	36	KΩ
V_{RXL} V_{LOL}	Output Saturation Voltage	V_{LI}, V_{KI} = (LOW) I_{RX}, I_{LO} = 3mA			0.4	V
I_{RX} I_{LO}	Output Short Circuit Current	V_{RX}, V_{LO} = 6V no damage		10		mA
V_{RXH} V_{LOH}	Output Voltage High State	$10M\Omega \leq R_{LRX}$; $10M\Omega \leq R_{LLO}$	V_{ST}-0.25	V_{ST}-0.1	V_{ST}	V
R_A	Output Pull-up Resistor LO Output	Output Status (HIGH) $-0.3V \leq V_{LO} \leq 25V$	7	10	18	KΩ
V_{KOL}	Output Saturation Voltage	$\|I_{KO}\|$ = 10mA			0.3	V
		$\|I_{KO}\|$ = 30mA @ $V_{Diag} = V_Z$ $\|I_{KO}\|$ = 20mA @ $V_{Diag} = V_{ST}$			0.5	V
I_{KOSC}	Output Short Circuit Current	V_{KO} = 16V no damage		50		mA
$\|I_{KOH}\|$	Output Leakage Current	Output K = (HIGH) $20V < V_{KO} \leq 50V$ (for output K voltage $20V < V_{KO} \leq 50V$ the output may be disabled internally) $0V \leq V_Z \leq 40V$; $0V \leq V_{ST} \leq 6V$			50	µA
R_{KOH}	D.C. Static Output OFF impedance	$0V \leq V_{KO} \leq 20V$ $0V \leq V_Z \leq 40V$ $0V \leq V_{ST} \leq 6V$	200			KΩ
$\|I_{RXH}\|$	Output Leakage Current	Output RX = (HIGH) $0 \leq V_{RX} \leq V_{ST}$			10	µA
f_{LI_LO} f_{KI_RX} f_{TX_KO}	Transmission Frequency	C_{LO}, C_{RX}, $C_{KO} \leq$ 15pF (external loads)	200			KHz
		R_{RX} = 10KΩ to V_{ST}	200			KHz
		$R_{KO} \leq$ 1.5KΩ to $V_{Diag} = V_Z$	10	60		KHz
		$R \leq 910\Omega$ to $V_{Diag} = V_{ST}$; $C_{KOISO} \leq$ 1.3nF	5	12		KHz
C_{KOi}	Internal Output Capacity				20	pF

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$t_{1,LI-LO}$ $t_{1,KI-RX}$ $t_{r,TX-KO/SDL}$ $t_{r,TX-KO/ISO}$	Rise Time	for the definition of t_1, t_2 see fig 2 for SDL: $V_{Diag} = V_{ST} = 5V$ $V_Z = 12V$ T_j 25°C, (1)	 10	1.5 1.5 15 3	 20 5.0	µs µs µs µs
$t_{2,LI-LO}$ $t_{2,KI-RX}$ $t_{r,TX-KO/SDL}$ $t_{r,TX-KO/ISO}$	Fall Time	for ISO: $V_{Diag} = V_Z = 12V$	 10	1.5 1.5 15 3	 20 5.0	µs µs µs µs
$V_{ext\ KO}$	External KO Negative Clamp Voltage	$R_{LKO} = 75\Omega$; $V_{KO} \geq V_{KO\ sub\text{-}diode}$ @ $I_{KO} = -100\mu A$, $V_Z = 0V$; $t_j = 25°C$	-1.5			V
Inverter Matrix / Static Input Signal						
$V_{IN1,2L}$	Input Voltage Low		-0.15		1	V
$V_{IN1,2H}$	Input Voltage High		2		V_{ST}+0.15	V
$R_{IN1,2}$	Input Resistor at IN1, IN2 Input	$-0.15 \leq V_{IN1,2} \leq V_{ST}+0.15V$	14	20	36	KΩ
Current Consumption						
I_{ST}	Supply Current	$V_{ST} \leq 5.25V$; $C_{I1,2,3}$, T_X, K_I = (LOW) IN1, IN2 = (LOW) $0V \leq V_{P1,2} \leq V_{ST}$			6	mA
I_Z	Supply Current	$VZ \leq 16V$			10	mA
I_{Diag}	Supply Current	$4.75V \leq V_{Diag} \leq 16V$			4	mA
V_{CCR}	Reverse Supply	$R_{ext} \leq 10M\Omega$ @ V_{CC} all inputs open $V_Z = V_{Diag} = 4.3V$			0.2	V
Diode (only on chip available)						
V_{CL}	Clamping Voltage	I_F, = 10mA, T_j = 25°C			1.0	V
T_K	Clamping Voltage Temp. Coefficient		-25		-1.0	mV/K
V_{BR}	Reverse Breakdown Voltage	$I_R = 100\mu A$; $T_j = 125°C$	50			V
V_{BRSub}	Substrate Breakdown Voltage	$I_{Sub} = 100\mu A$; $T_j = 125°C$	50			V

1)According to GM Serial specification XDE-5024 a line disturbance lower than 20µV for any frequencies higher than 530kHz is realized by means of controlling the leading and the falling edge and by shaping the transition points of the trapezoidal waveform of the output signal.

Control Function Truth Table

IN1	IN2	DIAGNOSTIC STATUS	
L	L	RX = $\overline{KI}$	KO = $\overline{TX}$
L	H	RX = $\overline{KI}$	KO = TX
H	L	RX = KI	KO = $\overline{TX}$
H	H	RX = KI	KO = TX

Figure 1. Transient Characteristic Comparators

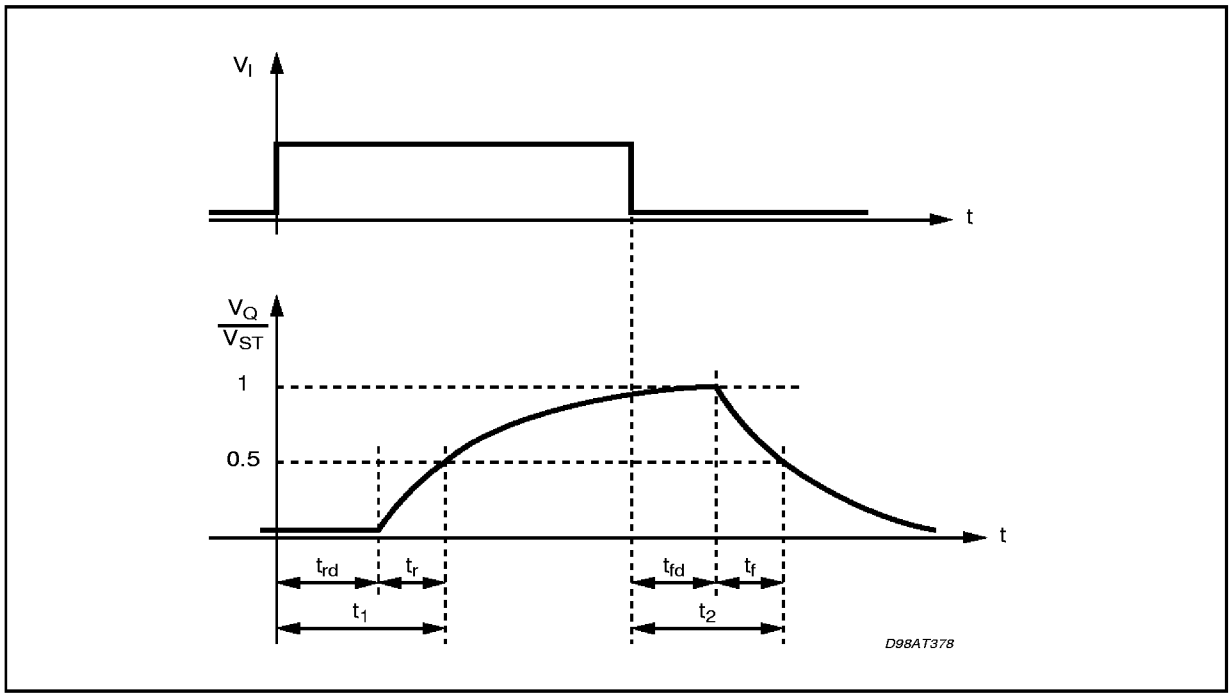
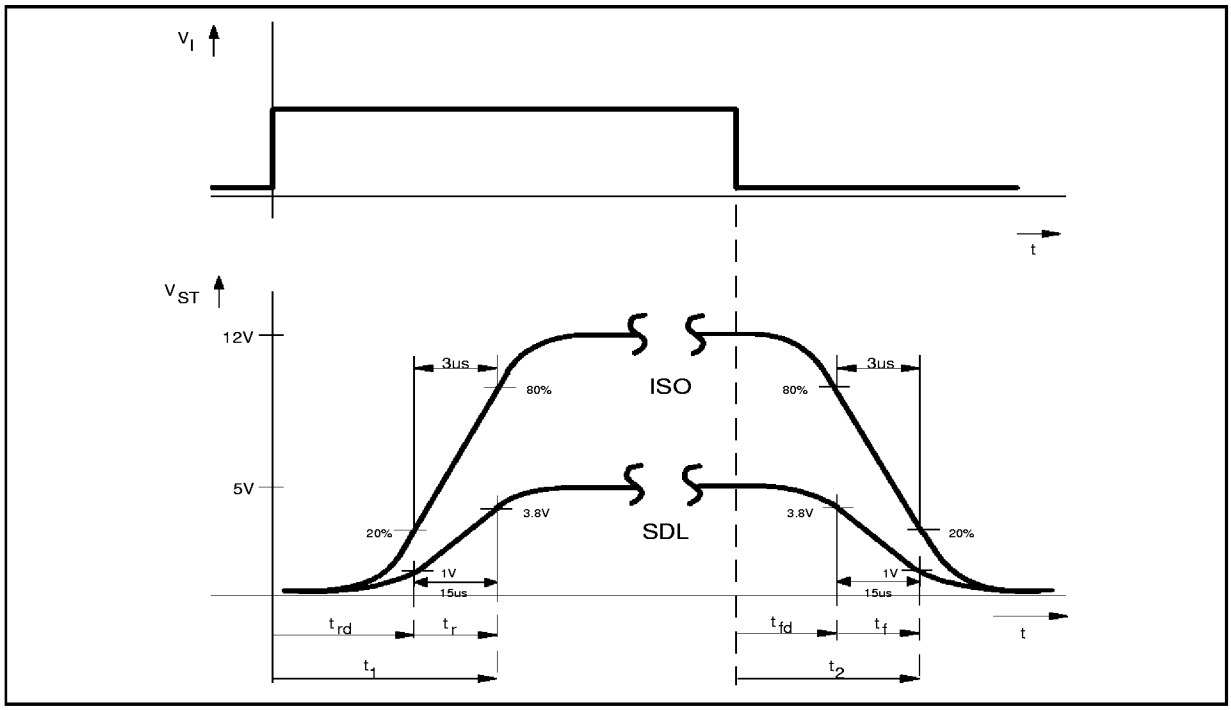
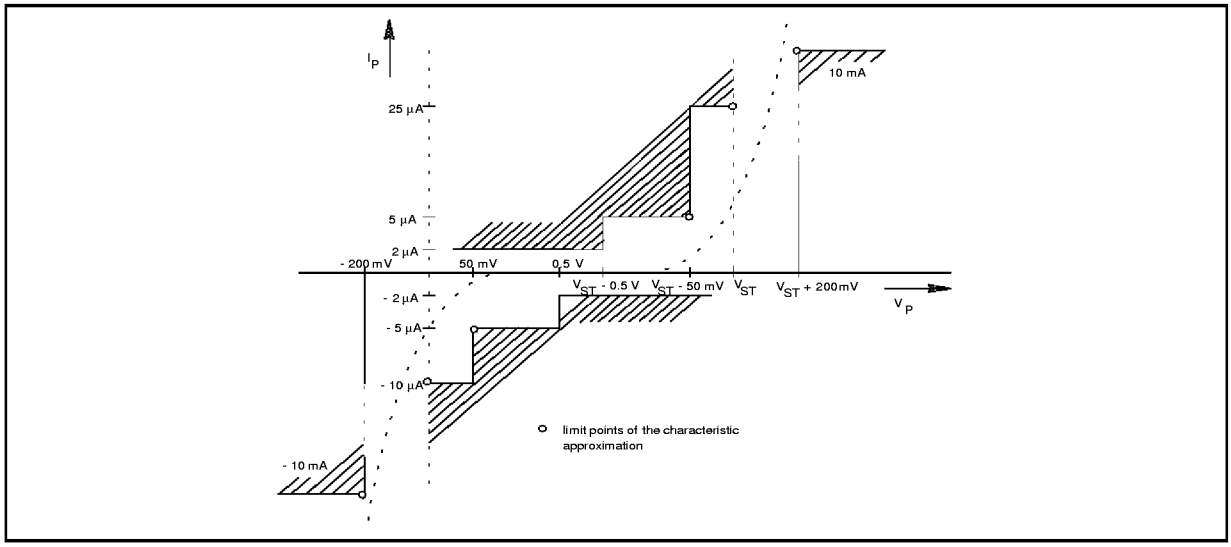


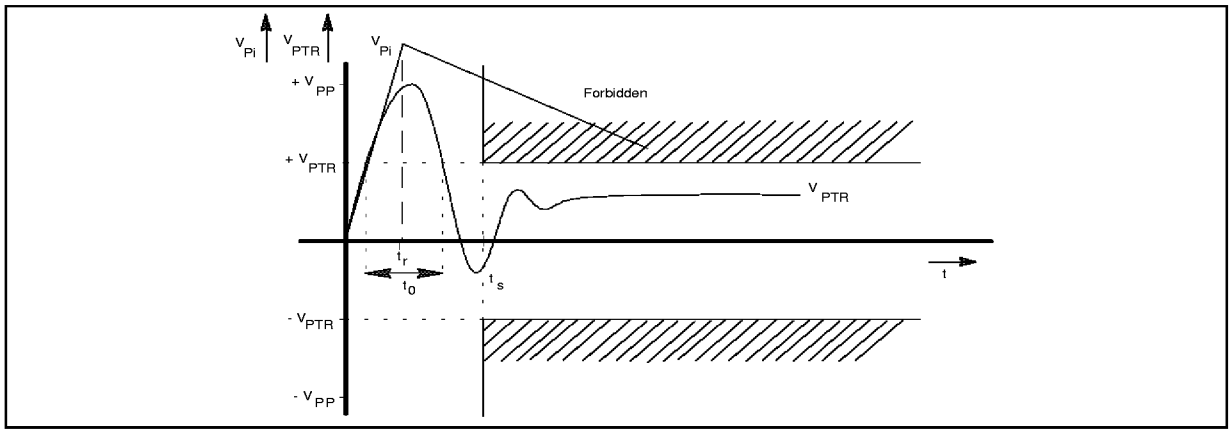
Figure 2.



DC Input Characteristics



Dynamic Input Characteristics



FUNCTIONAL DESCRIPTION

The thermal shut down function switches OFF the K output if the chip temperature increases above the thermal shut down threshold.

If the voltage applied to the KO output will be higher than the K disable threshold the output KO will be switched OFF.

To programm the ISO or SDL mode the pin V_{Diag} must be connected to V_Z or V_{ST}.

APPLICATION NOTES

Because of stability the external network as shown in the application circuit diagram at the protection pins P1, P2 is recommended.

The stray capacitor CPi should be kept as small as possible (CPi ≤ 5pF).

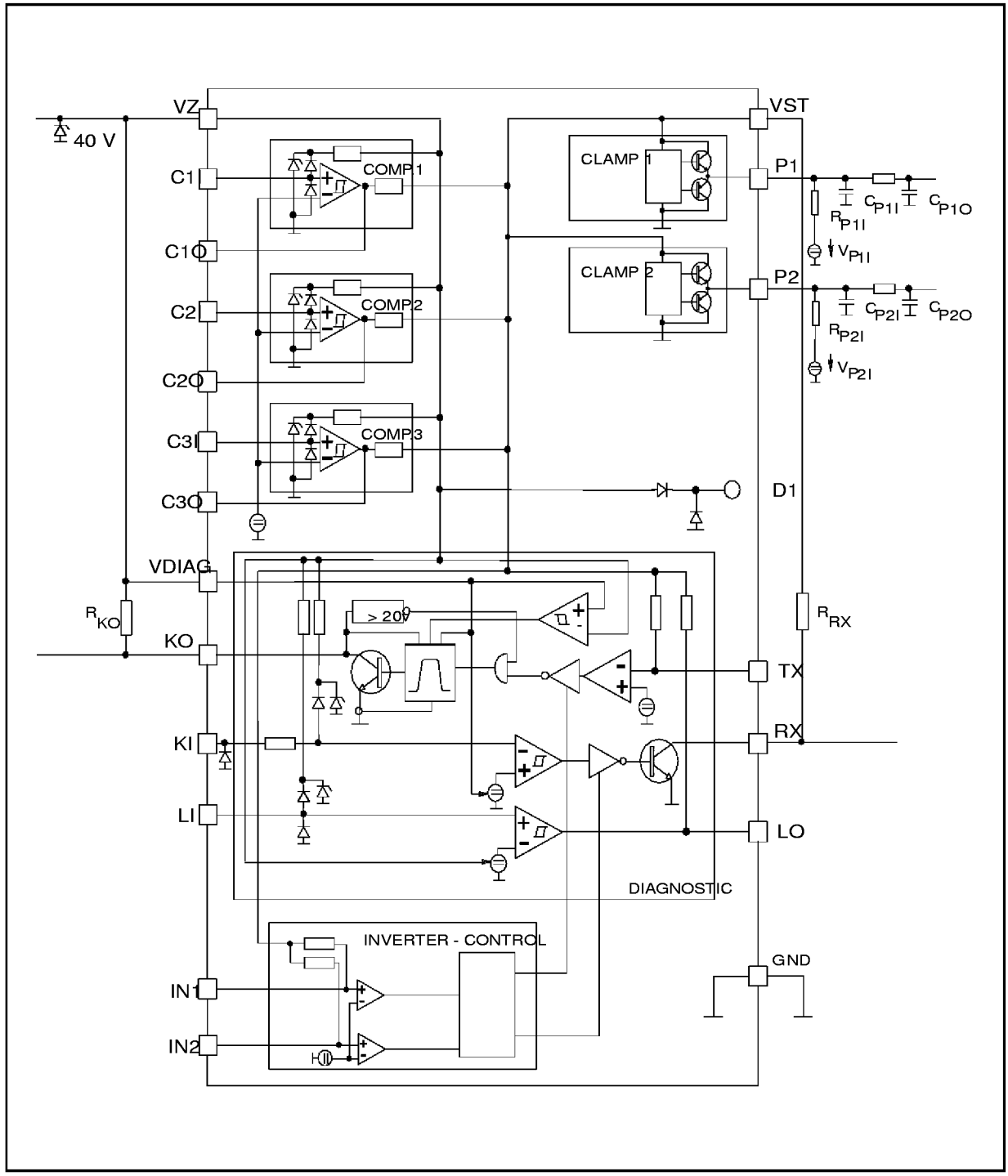
The input current must be limited via the resistor RPi. For 10 mA input current is calculated to :

$$R_{Pi} = \frac{V_{Pi}max}{10mA}$$

The low pass filter R_{PO}, C_{PO} reduces low voltage high frequency interference during the non clamping range and avoids any oscillation for high voltage spikes.

Recommended values (R_{PO} = 10KΩ, C_{PO} = 0.1nF ... 1nF).

ISO and SDL Application Circuit



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)