Description

The μPD42601 silicon file is an economical mass storage device specifically designed to replace magnetic disk drives in silicon disk, solid-state recording, and system backup applications in a variety of computer systems. Organized as 1,048,576 words by 1 bit, the μPD42601 provides a battery backup feature for enhanced system performance and a substantial savings in power consumption.

The device is capable of executing standard access or page-mode write and read cycles. Refreshing is accomplished by means of $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $\overline{RAS}$-only refresh cycles, self-refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during a 32-ms period.

The μPD42601 is uniquely suitable for battery backup systems because it requires a very low power supply current for extended periods of self-refresh operation. If ambient temperature is limited to 50 °C (max), as little as 30 μA (max) is required to maintain all data.

The μPD42601 is available in high-density 20-pin plastic ZIP or 26/20-pin plastic SOJ packaging.

Features

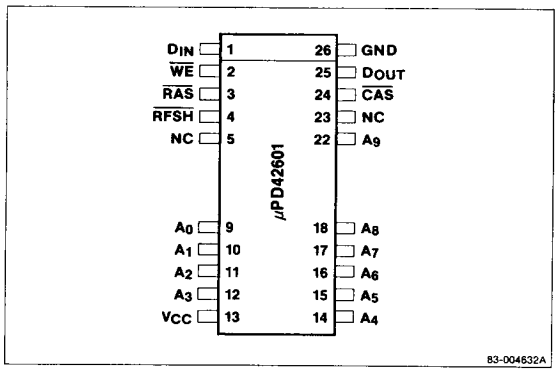
- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ CMOS technology
- ☐ Low operating power: 12 mA maximum
- ☐ 30 μA maximum self-refresh current at 0 to 50 °C
- ☐ Read or write cycle time: 1000 ns minimum
- ☐ Page-mode cycle time: 200 ns minimum
- ☐ $\overline{CAS}$ before $\overline{RAS}$ refreshing
- ☐ 512 refresh cycles during 32-ms period
- ☐ Automatic self-refreshing by $\overline{RAS}$ input cycling

Ordering Information

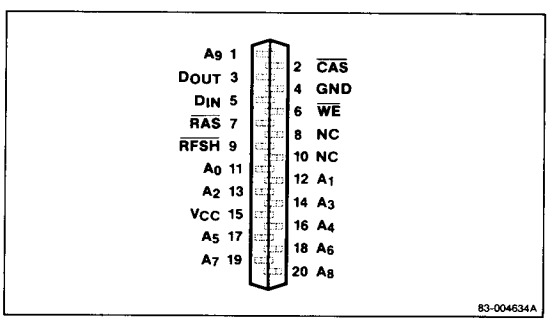
Part Number	Page-Mode Cycle (min)	Self-Refresh Current (max, 50 °C)	Package
μPD42601LA-60	200 ns	120 μA	26/20-pin plastic SOJ
LA-60L	200 ns	30 μA	
μPD42601V-60	200 ns	120 μA	20-pin plastic ZIP
V-60L	200 ns	30 μA	

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



Pin Identification

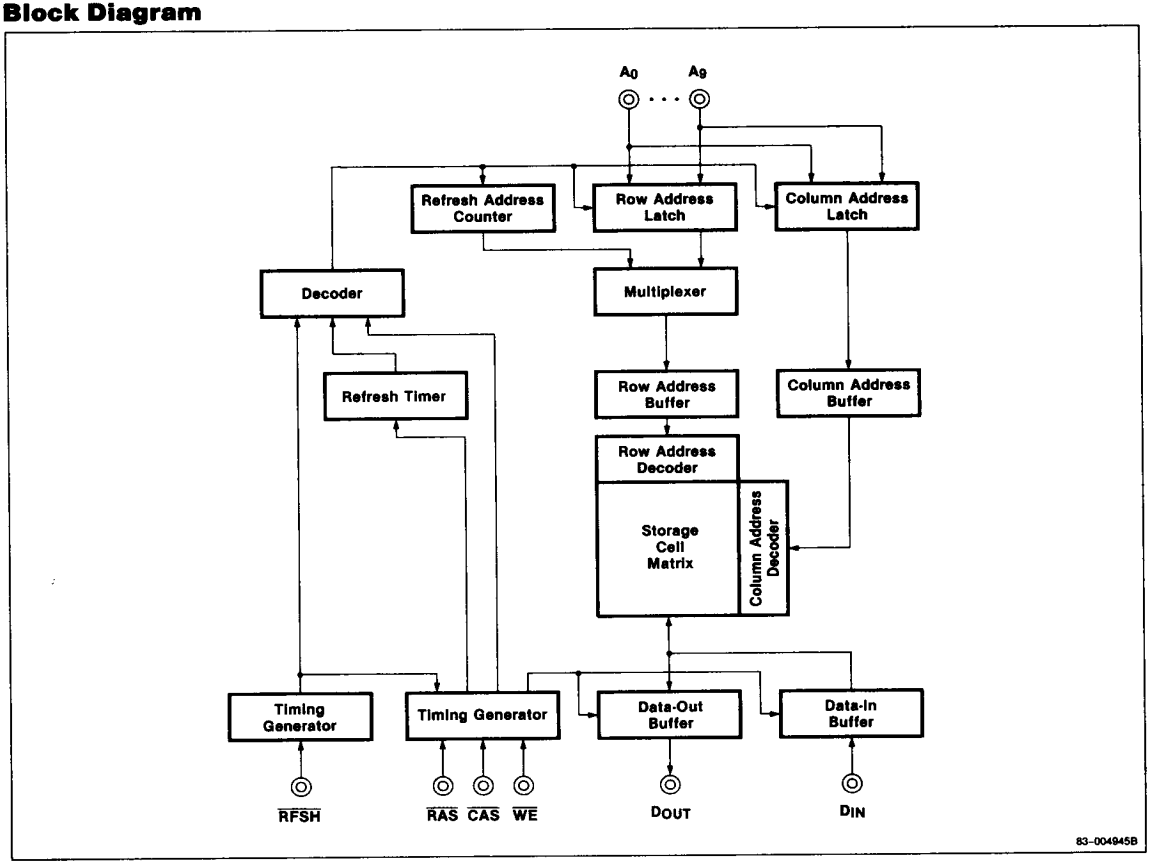
Name	Function
A_0 - A_8	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{RFSH}$	Self-refresh control
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W
Supply voltage, V_{CC}	−1.0 to +7.0 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



Operation

Write and Read Operation

The μPD42601 is capable of standard write and read operation as well as page-mode operation. The ten row address bits are set up on pins A_0 through A_9 and latched onto the chip by $\overline{RAS}$. Subsequently, ten column address bits are set up on pins A_0 through A_9 and latched onto the chip by $\overline{CAS}$. An appropriate write or read cycle is executed according to the logical level of $\overline{WE}$: a high $\overline{WE}$ initiates a read cycle and low $\overline{WE}$ initiates a write cycle.

Page-mode operation may be executed by pulsing $\overline{CAS}$ repeatedly while maintaining a low $\overline{RAS}$. The first word is accessed in the same manner as in standard write and read operation, with row addresses latched onto the chip by $\overline{RAS}$ and column addresses latched by $\overline{CAS}$. Subsequent column addresses are accessed for each $\overline{CAS}$ cycle, repeated during a period up to the maximum $\overline{RAS}$ pulse width.

Refresh Operation

$\overline{CAS}$ before $\overline{RAS}$ Refreshing. This cycle may be initiated by bringing $\overline{CAS}$ low before $\overline{RAS}$ and holding it low after $\overline{RAS}$ falls. A built-in address counter makes external addressing unnecessary.

$\overline{RAS}$-Only Refreshing. $\overline{RAS}$-only refreshing is executed by holding $\overline{CAS}$ high as the row addresses are latched onto the chip by $\overline{RAS}$. Using this cycle, all storage cells are refreshed by the 512 address combinations of A_0 through A_8 during a 32-ms period.

Self-Refreshing. A self-refresh cycle is initiated for the addresses generated by the internal counter whenever $\overline{RFSH}$ is active low and the $\overline{RAS}$ input is cycling (see figure 1). Since the minimum required $\overline{RAS}$ cycling frequency depends on ambient temperature, power consumption will also vary with temperature as shown in the AC and DC Characteristics. For extended periods of self-refresh operation, a low supply current is required; e.g., if ambient temperature is limited to 50°C (max), as little as 30 μA (max) is required to maintain all data.

18j

Recommended DC Operating Conditions

$T_A = 0$ to +70°C; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V

Capacitance

$T_A = 25$°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$
Output capacitance	C_D	7	pF	D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Operating current, average	I_{CC1}			12	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; I_O = 0 mA; t_{RC} = t_{RC} (min)
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{RFSH}$ = V_{IH}
				0.5	mA	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{RFSH}$ ≥ V_{CC} − 0.4; A_0-A_9, D_{IN} and $\overline{WE}$ ≥ V_{CC} − 0.4 or ≤ 0.4 V
Operating current, $\overline{RAS}$-only refresh, average	I_{CC3}			10	mA	t_{RC} = t_{RC} (min); I_O = 0 mA
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh, average	I_{CC4}			10	mA	t_{RC} = t_{RC} (min); I_O = 0 mA
Operating current, self-refresh mode, average	I_{CC5}			30	μA	$\overline{RAS}$ cycling at 50 kHz (Notes 1, 2, 3, 4)
				60	μA	$\overline{RAS}$ cycling at 100 kHz (Notes 1, 2, 3, 4)
				120	μA	$\overline{RAS}$ cycling at 200 kHz (Notes 1, 2, 3)
Operating current, page mode, average	I_{CC6}			12	mA	t_{PC} = t_{PC} (min); I_O = 0 mA
Input leakage current	I_{IL}	−1		1	μA	V_{IN} = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_{OL}	−1		1	μA	D_{OUT} disabled; V_{OUT} = 0 to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_O = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_O = −5 mA

Notes:

(1) When t_{FAS} ≤ 2.5 ms, I_{CC5} does not depend on the $\overline{RAS}$ clock; I_{CC5} (max) = 500 μA. When t_{FAS} ≥ 2.5 ms, I_{CC5} (max) = 500 μA in the first 2.5 ms after $\overline{RFSH}$ falls (it does not depend on the $\overline{RAS}$ clock). Subsequently, I_{CC5} is 120 μA for the μPD42601 or is as shown in the following table for the μPD42601-L.

Operating Temperature [T_A]	Clock Frequency [min]	Self-Refresh Current [max]
0 to 50°C	50 kHz	30 μA at 50 kHz
0 to 60°C	100 kHz	60 μA at 100 kHz
0 to 70°C	200 kHz	120 μA at 200 kHz

(2) t_{RCF} depends on operating temperature as reflected in the table below (see figures 2 and 3).

Operating Temperature [T_A]	t_{RCF} [max] μPD42601-L	μPD42601
0 to 50°C	20 μs	5 μs
0 to 60°C	10 μs	5 μs
0 to 70°C	5 μs	5 μs

(3) Average power supply current required for self refreshing is measured according to the following conditions: $\overline{RAS}$ is cycling at 50, 100 or 200 kHz; V_{IH} ≥ V_{CC} − 0.4 V; V_{IL} ≤ 0.4 V; t_T ≤ 50 ns; A_0 to A_9, D_{IN}, $\overline{WE}$ and $\overline{CAS}$ = V_{CC} to GND; RFSH = V_{IL}. When $\overline{RFSH}$ = V_{IL} (≤ 0.4 V), the $\overline{RAS}$ input must be cycled at or exceeding the minimum frequency requirements.

(4) This specification applies to the μPD42601-L only. For the non-L version, I_{CC5} is 120 μA, maximum, at all T_A.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Random read or write cycle time	t_{RC}	1000		ns	(Note 5)
Page-mode cycle time	t_{PC}	200		ns	(Notes 5, 15)
Access time from $\overline{RAS}$	t_{RAC}		600	ns	(Notes 6, 7)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		100	ns	(Notes 6, 8)
Output buffer turnoff delay	t_{OFF}	0	100	ns	(Note 9)
Transition time (rise and fall)	t_T	3	50	ns	(Notes 3, 4)
$\overline{RAS}$ precharge time	t_{RP}	390		ns	
$\overline{RAS}$ pulse width	t_{RAS}	600	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	100	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	600		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	150	500	ns	(Note 10)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	30		ns	(Note 11)
$\overline{CAS}$ precharge time (non-page cycle)	t_{CPN}	90		ns	
$\overline{CAS}$ precharge time (page cycle)	t_{CP}	90		ns	(Note 15)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Row address setup time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	90		ns	
Column address setup time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	90		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	590		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	75		ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	(Note 12)
Write command hold time	t_{WCH}	90		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	590		ns	
Write command pulse width	t_{WP}	90		ns	
Data-in setup time	t_{DS}	0		ns	(Note 14)
Data-in hold time	t_{DH}	90		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	590		ns	
Write command setup time	t_{WCS}	0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	30		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	105		ns	
Refresh period	t_{REF}		32	ms	Addresses A_0-A_8
Self-Refresh Cycle					
$\overline{RFSH}$ pulse width	t_{FAS}	810		ns	(Note 13)
$\overline{RAS}$ to $\overline{RFSH}$ delay time	t_{RFD}	100		ns	
$\overline{RAS}$ setup time to $\overline{RFSH}$	t_{FRS}	200		ns	
$\overline{RAS}$ cycle time in self-refresh mode	t_{RCF}	1000		ns	(Note 16)
$\overline{RAS}$ precharge time in self-refresh mode	t_{RPF}	390		ns	
$\overline{RAS}$ pulse width in self-refresh mode	t_{RSF}	600		ns	
$\overline{RFSH}$ to $\overline{RAS}$ delay time	t_{FRD}	100		ns	
$\overline{RAS}$ hold time in self-refresh mode	t_{FRH}	200		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up (V_{CC} = +5.0 V ±10%), followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. $\overline{RAS}$, $\overline{CAS}$, and $\overline{RFSH}$ must equal V_{IH} during the initial pause.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(6) Load = 2 TTL loads and 100 pF (V_{OH} = 2.4 V, V_{OL} = 0.4 V).

(7) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(8) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(9) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(10) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) When $t_{FAS} \leq 2.5$ ms, I_{CC5} does not depend on the $\overline{RAS}$ clock; I_{CC5} (max) = 500 μA. When $t_{FAS} \geq 2.5$ ms, I_{CC5} (max) = 500 μA for the first 2.5 ms after $\overline{RFSH}$ falls (it does not depend on the $\overline{RAS}$ clock). Subsequently, I_{CC5} is 120 μA for the μPD42601 or is as shown in the following table for the μPD42601-L.

Operating Temperature [T_A]	Clock Frequency [min]	Self-Refresh Current [max]
0 to 50°C	50 kHz	30 μA at 50 kHz
0 to 60°C	100 kHz	60 μA at 100 kHz
0 to 70°C	200 kHz	120 μA at 200 kHz

Notes [cont]:

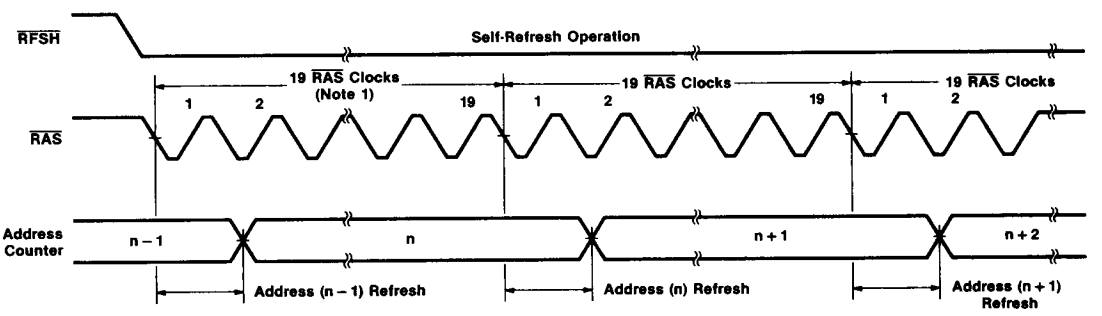
(14) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles.

(15) This parameter is applicable to page-mode operation.

(16) t_{RCF} depends on operating temperature as reflected in the table below (see figures 2 and 3).

Operating Temperature [T_A]	t_{RCF} [max]	
	μPD42601-L	μPD42601
0 to 50°C	20 μs	5 μs
0 to 60°C	10 μs	5 μs
0 to 70°C	5 μs	5 μs

Figure 1. Internal Address Generation in Self-Refresh Operation



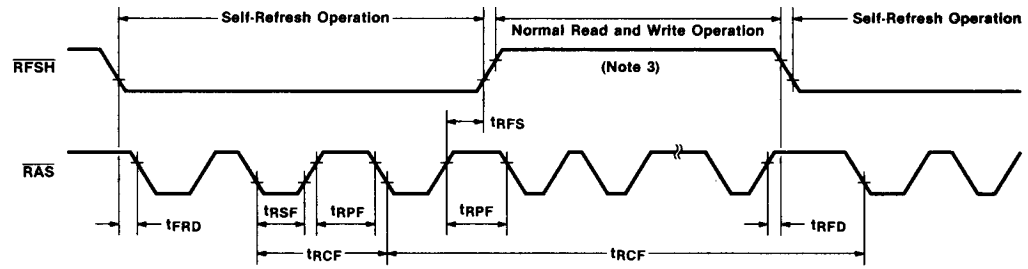
Notes:

(1) One internal address is refreshed every 19 $\overline{RAS}$ pulses.

(2) The self-refresh mode is intended primarily for long periods of refresh-only operation.

83-004503B

Figure 2. Special Requirement for t_{RCF} Near Periods of Limited Standard Refresh Cycles



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50 °C	20 μs	5 μs
60 °C	10 μs	5 μs
70 °C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] In this period of normal read/write operation, there are no CBR refresh cycles or less than 512 $\overline{RAS}$-only refresh cycles.

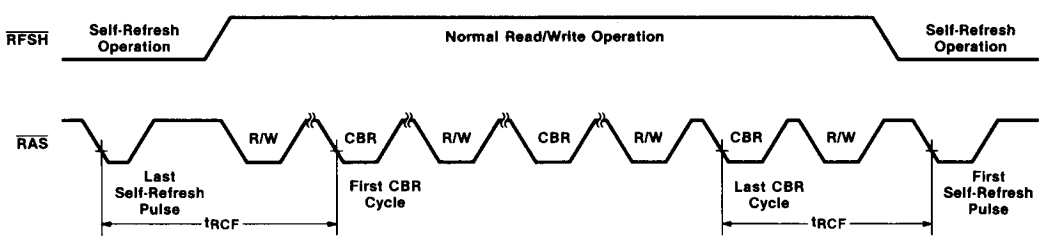
[4] The time delay between the last self-refresh pulse in one self-refresh cycle, and the first self-refresh pulse in the next cycle, is defined by t_{RCF} [max] when the intervening period of read and write operation meets the conditions in Note 3.

[5] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

83-004502B

18j

Figure 3. Timing Restrictions for Entering and Exiting Self-Refresh Operation



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50 °C	20 μs	5 μs
60 °C	10 μs	5 μs
70 °C	5 μs	5 μs

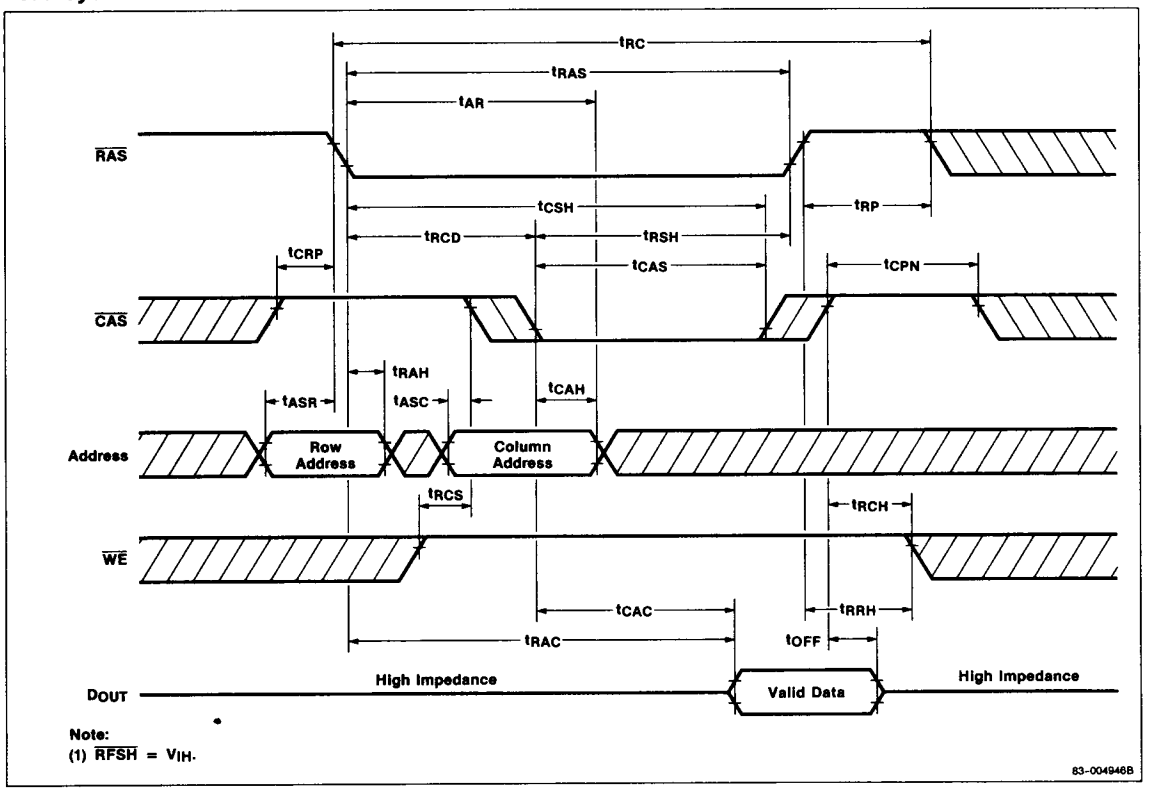
[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

83-004501B

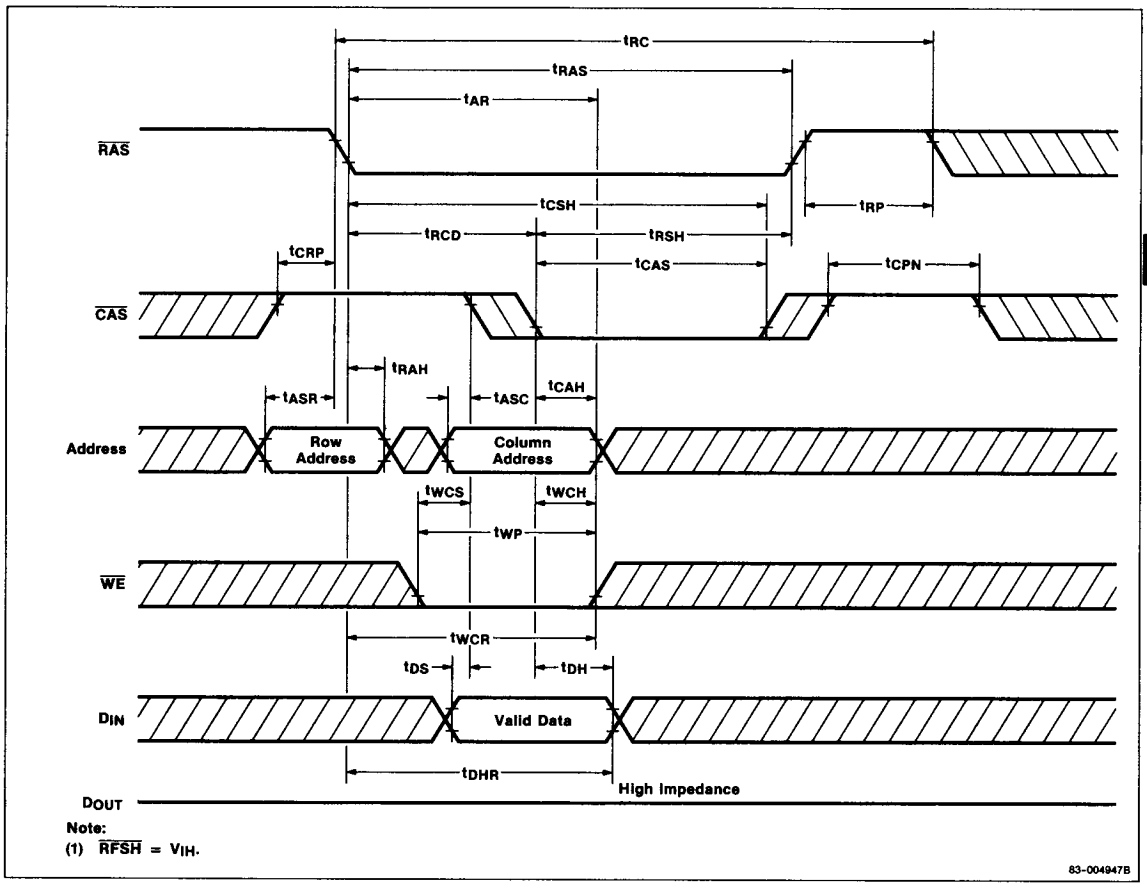
Timing Waveforms

Read Cycle



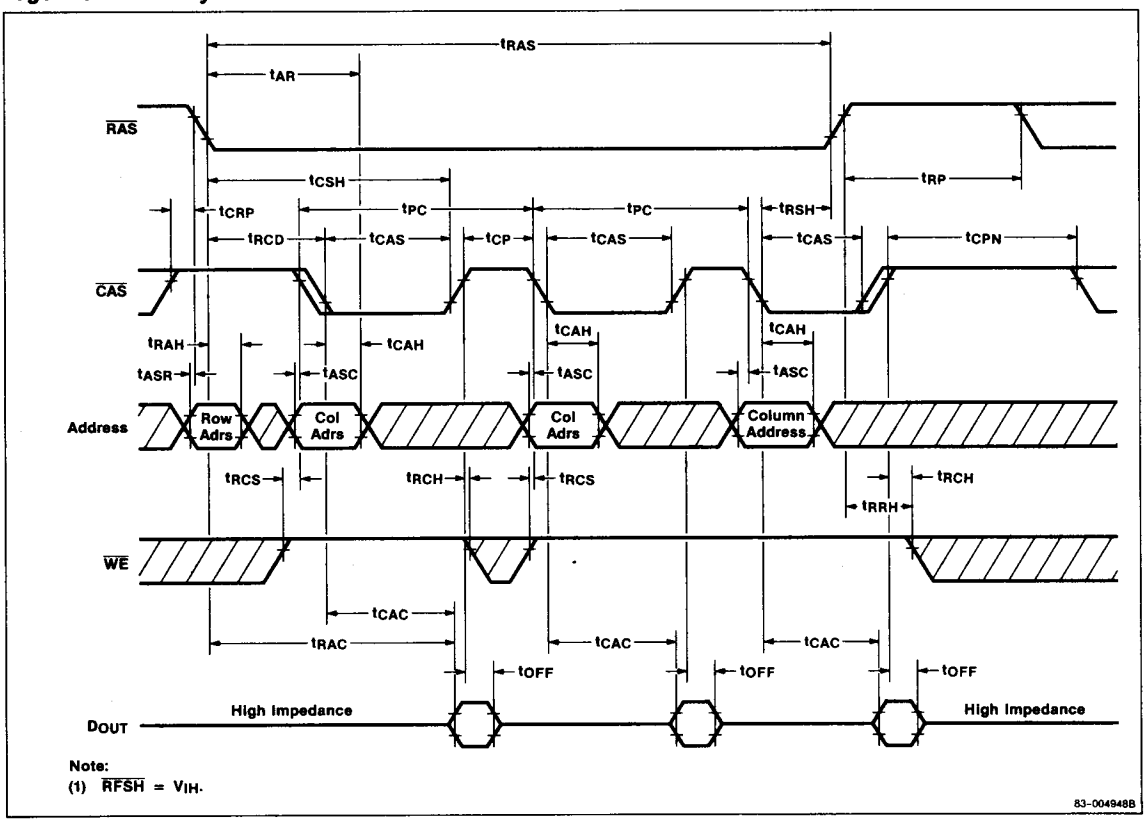
Timing Waveforms (cont)

Write Cycle (Early Write)



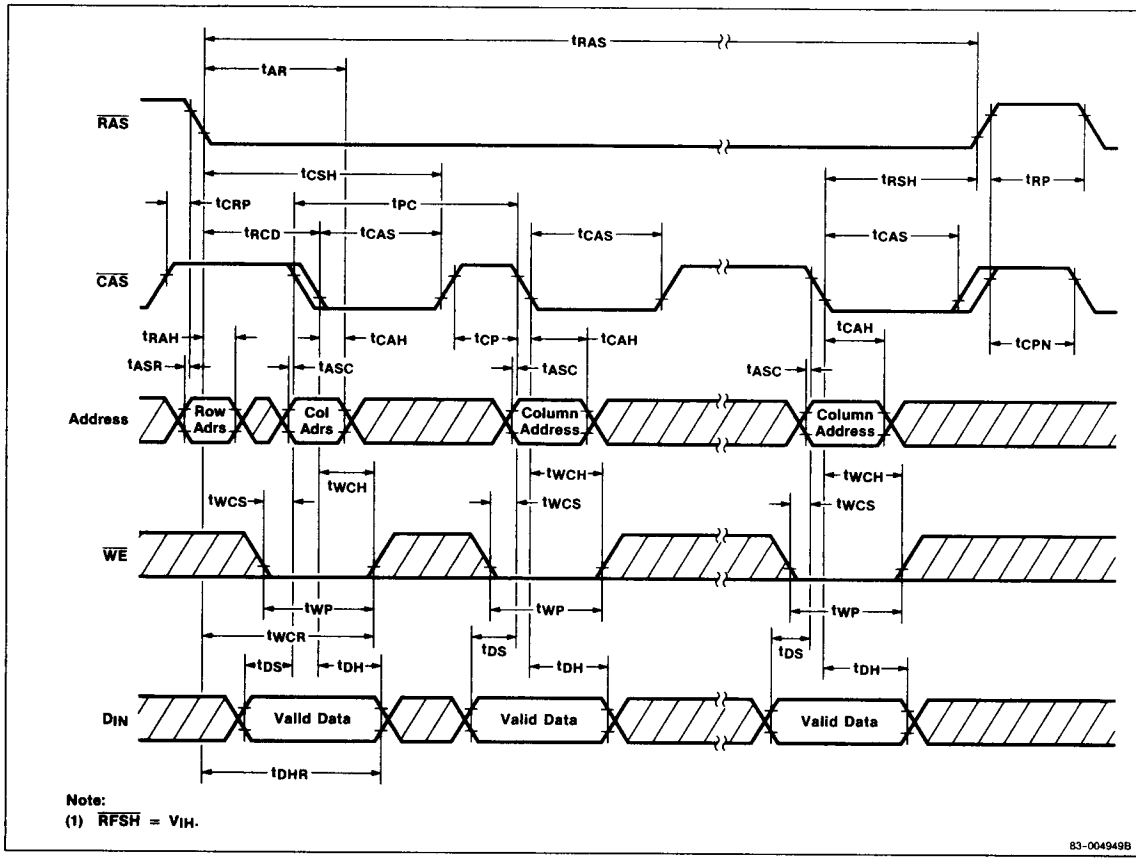
Timing Waveforms (cont)

Page-Mode Read Cycle



Timing Waveforms (cont)

Page-Mode Write Cycle (Early Write)



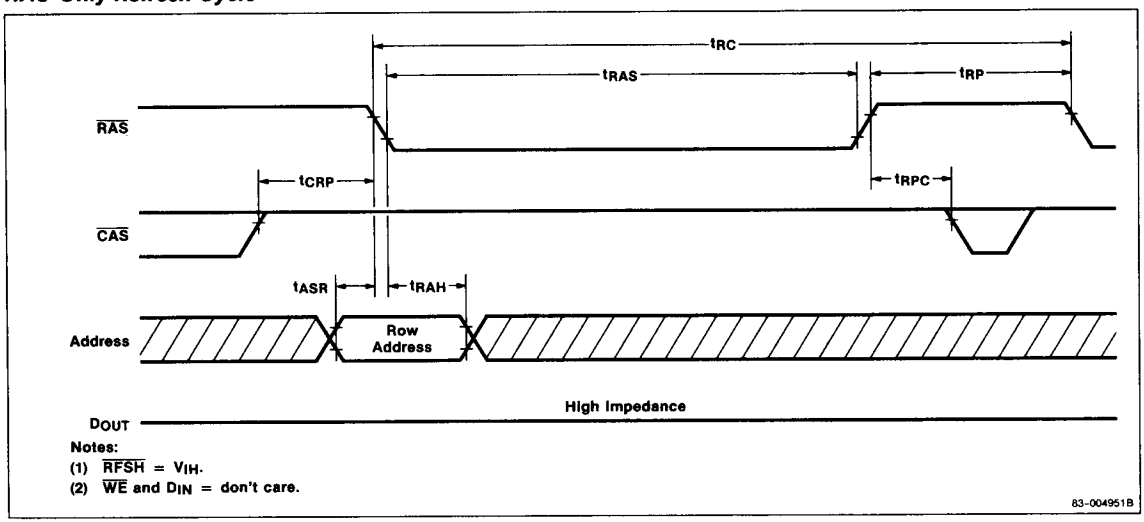
Note:
(1) $\overline{RFSH}$ = V_{IH}.

83-004949B

18j

Timing Waveforms (cont)

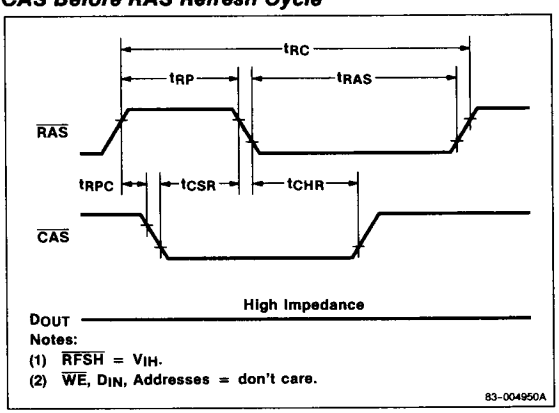
$\overline{RAS}$-Only Refresh Cycle



Notes:
(1) $\overline{RFSH}$ = V_{IH}.
(2) $\overline{WE}$ and D_{IN} = don't care.

83-004951B

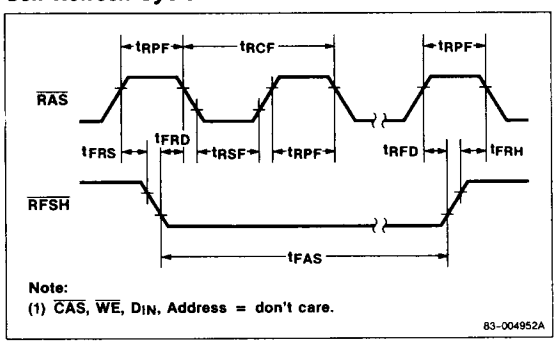
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Notes:
(1) $\overline{RFSH}$ = V_{IH}.
(2) $\overline{WE}$, D_{IN}, Addresses = don't care.

83-004950A

Self-Refresh Cycle



Note:
(1) $\overline{CAS}$, $\overline{WE}$, D_{IN}, Address = don't care.

83-004952A