

MOS INTEGRATED CIRCUIT μ PD431000A

1M-BIT CMOS STATIC RAM 128K-WORD BY 8-BIT

Description

The μ PD431000A is a high speed, low power, and 1,048,576 bits (131,072 words by 8 bits) CMOS static RAM.

The μ PD431000A has two chip enable pins (/CE1, CE2) to extend the capacity. And battery backup is available. In addition to this, A and B versions are low voltage operations.

The μ PD431000A is packed in 32-pin plastic DIP, 32-pin plastic SOP and 32-pin plastic TSOP (I) (8 × 13.4 mm) and (8 × 20 mm).

Features

- 131,072 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Low voltage operation (A version: Vcc = 3.0 to 5.5 V, B version: Vcc = 2.7 to 5.5 V)
- Operating ambient temperature: T_A = 0 to 70 °C
- Low Vcc data retention: 2.0 V (MIN.)
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

| Part number | Access time | Operating supply | Operating ambient | | Supply curre | nt |
|-----------------|--------------------|------------------|-------------------|------------------------|-------------------------|--|
| | ns (MAX.) | voltage V | temperature °C | At operating mA (MAX.) | At standby μA (MAX.) | At data retention μ A (MAX.) Note1 |
| μPD431000A-xxL | 70, 85 | 4.5 to 5.5 | 0 to 70 | 70 | 100 | 15 |
| μPD431000A-xxLL | | | | | 20 | 3 |
| μPD431000A-Axx | 70 Note2, 100 | 3.0 to 5.5 | | 35 Note3 | 13 Note5 | |
| μPD431000A-Bxx | 70 Note2, 120, 150 | 2.7 to 5.5 | | 30 Note4 | 11 Note6 | |

Notes 1. TA \leq 40 °C

- **2.** Vcc = 4.5 to 5.5 V
- **3.** 70 mA (Vcc > 3.6 V)
- 4. 70 mA (Vcc > 3.3 V)
- **5.** 20 μ A (Vcc > 3.6 V)
- **6.** 20 μ A (Vcc > 3.3 V)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.



Ordering Information

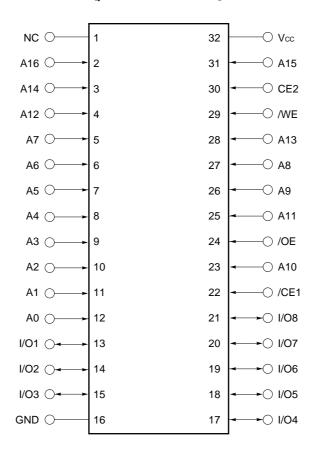
| Part number | Package | Access time ns (MAX.) | Operating supply voltage | Operating ambient temperature °C | Remark |
|-----------------------|------------------------|-----------------------|--------------------------|----------------------------------|------------|
| μPD431000ACZ-70L | 32-PIN PLASTIC DIP | 70 | 4.5 to 5.5 | 0 to 70 | L version |
| μPD431000ACZ-85L | (15.24mm (600)) | 85 | | | |
| μPD431000ACZ-70LL | | 70 | | | LL version |
| μPD431000ACZ-85LL | | 85 | | | |
| μPD431000AGW-70L | 32-PIN PLASTIC SOP | 70 | 4.5 to 5.5 | | L version |
| μPD431000AGW-85L | (13.34 mm (525)) | 85 | | | |
| μPD431000AGW-70LL | | 70 | | | LL version |
| μPD431000AGW-85LL | | 85 | | | |
| μPD431000AGW-A10 | | 100 | 3.0 to 5.5 | | A version |
| μPD431000AGW-B12 | | 120 | 2.7 to 5.5 | | B version |
| μPD431000AGW-B15 | | 150 | | | |
| μPD431000AGZ-85L-KJH | 32-PIN PLASTIC TSOP(I) | 85 | 4.5 to 5.5 | | L version |
| μPD431000AGZ-70LL-KJH | (8x20) (Normal bent) | 70 | | | LL version |
| μPD431000AGZ-85LL-KJH | | 85 | | | |
| μPD431000AGZ-B15-KJH |] | 150 | 2.7 to 5.5 | | B version |
| μPD431000AGZ-70LL-KKH | 32-PIN PLASTIC TSOP(I) | 70 | 4.5 to 5.5 | | LL version |
| μPD431000AGZ-B15-KKH | (8x20) (Reverse bent) | 150 | 2.7 to 5.5 | | B version |
| μPD431000AGU-B12-9JH | 32-PIN PLASTIC TSOP(I) | 120 | 2.7 to 5.5 | | B version |
| μPD431000AGU-B15-9JH | (8x13.4) (Normal bent) | 150 | | | |



Pin Configurations (Marking Side)

/xxx indicates active low signal.

32-PIN PLASTIC DIP (15.24 mm (600)) [μPD431000ACZ-xxL] [μPD431000ACZ-xxLL]



A0 - A16 : Address inputs

I/O1 - I/O8 : Data inputs / outputs

/CE1, CE2 : Chip Enable 1, 2

/WE : Write Enable
/OE : Output Enable
Vcc : Power supply

GND : Ground

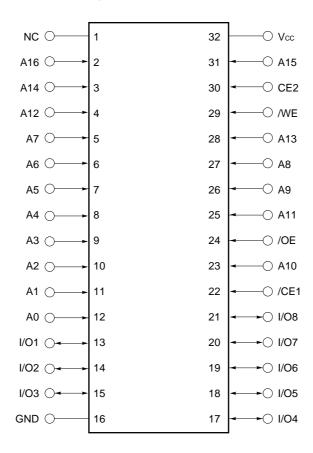
NC : No connection

Remark Refer to Package Drawings for the 1-pin index mark.

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32-PIN PLASTIC SOP (13.34 mm (525))

[μPD431000AGW-xxL]
[μPD431000AGW-xxLL]
[μPD431000AGW-Axx]
[μPD431000AGW-Bxx]



A0 - A16 : Address inputs

I/O1 - I/O8 : Data inputs / outputs

/CE1, CE2 : Chip Enable 1, 2

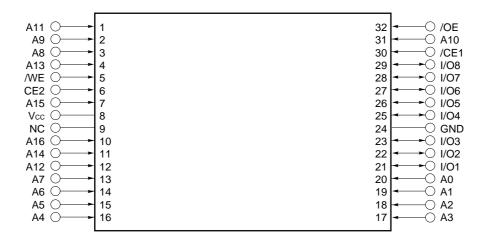
/WE : Write Enable
/OE : Output Enable
Vcc : Power supply

GND : Ground

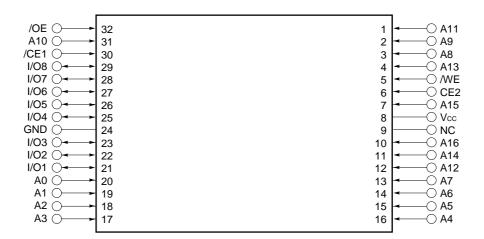
NC : No connection

Remark Refer to Package Drawings for the 1-pin index mark.

32-PIN PLASTIC TSOP(I) (8x20) (Normal bent) [μPD431000AGZ-xxL-KJH] [μPD431000AGZ-xxLL-KJH]



32-PIN PLASTIC TSOP(I) (8x20) (Reverse bent) [μPD431000AGZ-xxLL-KKH] [μPD431000AGZ-Bxx-KKH]



A0 - A16 : Address inputs

I/O1 - I/O8 : Data inputs / outputs

/CE1, CE2 : Chip Enable 1, 2

/WE : Write Enable

/OE : Output Enable

Vcc : Power supply

GND : Ground

NC : No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.

32-PIN PLASTIC TSOP(I) (8x13.4) (Normal bent) [μPD431000AGU-Bxx-9JH]



A0 - A16 : Address inputs

I/O1 - I/O8 : Data inputs / outputs

/CE1, CE2 : Chip Enable 1, 2
/WE : Write Enable
/OE : Output Enable
Vcc : Power supply

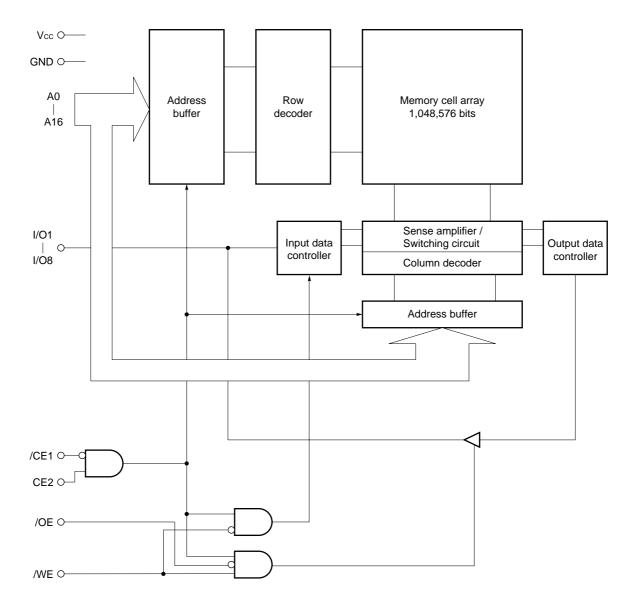
GND : Ground

NC : No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.



★ Block Diagram



Truth Table

| /CE1 | CE2 | /OE | /WE | Mode | I/O | Supply current |
|------|-----|-----|-----|----------------|----------------|----------------|
| Н | × | × | × | Not selected | High impedance | İsb |
| × | L | × | × | | | |
| L | Н | Н | Н | Output disable | | ICCA |
| L | Н | L | Н | Read | D оит | |
| L | Н | × | L | Write | Din | |

Remark \times : VIH or VIL



Electrical Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|-------------------------------|------------------|-----------|------------------------|------|
| Supply voltage | Vcc | | -0.5 Note to +7.0 | V |
| Input / Output voltage | VT | | -0.5 Note to Vcc + 0.5 | ٧ |
| Operating ambient temperature | TA | | 0 to 70 | °C |
| Storage temperature | T _{stg} | | -55 to +125 | °C |

Note -3.0 V (MIN.) (Pulse width: 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

| Parameter | Symbol | Condition | μPD431000A-xxL | | μPD431000A-Axx | | μPD431000A-Bxx | | Unit |
|-------------------------------|--------|-----------|----------------|-----------------|----------------|---------|----------------|---------|------|
| | | | μPD4310 | μPD431000A-xxLL | | | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Supply voltage | Vcc | | 4.5 | 5.5 | 3.0 | 5.5 | 2.7 | 5.5 | V |
| High level input voltage | VIH | | 2.2 | Vcc+0.5 | 2.2 | Vcc+0.5 | 2.2 | Vcc+0.5 | V |
| Low level input voltage | VIL | | -0.3 Note | +0.8 | -0.3 Note | +0.5 | -0.3 Note | +0.5 | V |
| Operating ambient temperature | TA | | 0 | 70 | 0 | 70 | 0 | 70 | °C |

Note -3.0 V (MIN.) (Pulse width: 30 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|----------------------------|--------|-------------------------|------|------|------|------|
| Input capacitance | Cin | Vin = 0 V | | | 6 | pF |
| Input / Output capacitance | Cı/o | V ₁ /O = 0 V | | | 10 | pF |

Remarks 1. Vin: Input voltage

 $V_{I/O}$: Input / Output voltage

2. These parameters are not 100% tested.



DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

| Parameter | Symbol | Test condit | tion | μPD4 | 431000 | A-xxL | μPD4 | 31000 <i>F</i> | \-xxLL | μPD4 | 131000 | A-Axx | Unit |
|-----------------------|------------------|---|-----------------|------|--------|-------|------|----------------|--------|---------|--------|-------|------|
| | | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| Input leakage current | lu | V _{IN} = 0 V to V _{CC} | | -1.0 | | +1.0 | -1.0 | | +1.0 | -1.0 | | +1.0 | μΑ |
| I/O leakage | Іьо | $V_{I/O} = 0 V \text{ to } V_{CC},$ | | -1.0 | | +1.0 | -1.0 | | +1.0 | -1.0 | | +1.0 | μΑ |
| current | | /CE1 = V _{IH} or CE2 = V | VIL | | | | | | | | | | |
| | | or /WE = V _{IL} or /OE = | VIH | | | | | | | | | | |
| Operating | ICCA1 | /CE1 = VIL, CE2 = VII | ١, | | 40 | 70 | | 40 | 70 | | 40 | 70 | mA |
| supply current | | I ₁ /O = 0 mA | | | | | | | | | | | |
| | | Minimum cycle time | Vcc ≤ 3.6 V | | | _ | | | _ | | | 35 | |
| | ICCA2 | /CE1 = V _I L, CE2 = V _I ⊦ | H, II/O = 0 mA, | | | 15 | | | 15 | | | 15 | |
| | | Cycle time = ∞ | Vcc ≤ 3.6 V | | | _ | | | _ | | | 8 | |
| | Іссаз | /CE1 ≤ 0.2 V, CE2 ≥ | Vcc – 0.2 V, | | | 10 | | | 10 | | | 10 | |
| | | Cycle time = 1 μ s, Ivo | o = 0 mA, | | | | | | | | | | |
| | | $V_{IL} \le 0.2 \text{ V}, \text{ V}_{IH} \ge V_{CC}$ | – 0.2 V | | | | | | | | | | |
| | | | Vcc ≤ 3.6 V | | | _ | | | _ | | | 8 | |
| Standby | IsB | /CE1 = VIH or CE2 = V | VIL | | | 3 | | | 3 | | | 3 | mA |
| supply current | | | Vcc ≤ 3.6 V | | | _ | | | _ | | | 2 | |
| | I _{SB1} | /CE1 ≥ Vcc – 0.2 V, | | | 2 | 100 | | 1 | 20 | | 1 | 20 | μΑ |
| | | CE2 ≥ Vcc - 0.2 V | Vcc ≤ 3.6 V | | | _ | | | _ | | 0.5 | 13 | |
| | I _{SB2} | CE2 ≤ 0.2 V | | | 2 | 100 | | 1 | 20 | | 1 | 20 | |
| | | | Vcc ≤ 3.6 V | | _ | _ | | _ | _ | | 0.5 | 13 | |
| High level | V _{OH1} | Iон = −1.0 mA, Vcc ≥ | 4.5 V | 2.4 | | | 2.4 | | | 2.4 | | | V |
| output voltage | | Iон = −0.5 mA | | _ | | | _ | | | 2.4 | | | |
| | V _{OH2} | Iон = −0.02 mA | | _ | | | _ | | | Vcc-0.1 | | | |
| Low level | V _{OL1} | IoL = 2.1 mA, Vcc ≥ 4 | .5 V | | | 0.4 | | | 0.4 | | | 0.4 | V |
| output voltage | | IoL = 1.0 mA | | | | _ | | | _ | | | 0.4 | |
| | V _{OL2} | IoL = 0.02 mA | | | | _ | | | _ | | | 0.1 | |

Remarks 1. VIN: Input voltage

Vi/o: Input / Output voltage

2. These DC characteristics are in common regardless product classification.

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DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

| Parameter | Symbol | Test condition | | μ | PD431000A | -Bxx | Unit |
|---------------------------|------------------|---|-----------------|---------|-----------|------|------|
| | | | | MIN. | TYP. | MAX. | |
| Input leakage current | lu | VIN = 0 V to Vcc | | -1.0 | | +1.0 | μΑ |
| I/O leakage current | Іго | V _{I/O} = 0 V to V _{CC} , /CE1 = V _{IH} or CE2 = V | / _{IL} | -1.0 | | +1.0 | μΑ |
| | | or /WE = V _{IL} or /OE = V _{IH} | | | | | |
| Operating supply current | ICCA1 | /CE1 = VIL, CE2 = VIH, II/O = 0 mA | | | 40 | 70 | mA |
| | | Minimum cycle time | Vcc ≤ 3.3 V | | | 30 | |
| | ICCA2 | /CE1 = VIL, CE2 = VIH, II/O = 0 mA, | | | | 15 | |
| | | Cycle time = ∞ | Vcc ≤ 3.3 V | | | 7 | |
| | Іссаз | /CE1 ≤ 0.2 V, CE2 ≥ Vcc − 0.2 V, | | | | 10 | |
| | | Cycle time = 1 μ s, I ν o = 0 mA, | | | | | |
| | | $V_{IL} \le 0.2 \text{ V}, V_{IH} \ge V_{CC} - 0.2 \text{ V}$ | Vcc ≤ 3.3 V | | | 7 | |
| Standby supply current | IsB | /CE1 = Vih or CE2 = Vil | | | | 3 | mA |
| | | | Vcc ≤ 3.3 V | | | 2 | |
| | I _{SB1} | /CE1 ≥ Vcc - 0.2 V, CE2 ≥ Vcc - 0.2 V | | | 1 | 20 | μΑ |
| | | | Vcc ≤ 3.3 V | | 0.5 | 11 | |
| | I _{SB2} | CE2 ≤ 0.2 V | | | 1 | 20 | |
| | | | Vcc ≤ 3.3 V | | 0.5 | 11 | |
| High level output voltage | V _{OH1} | Iон = −1.0 mA, Vcc ≥ 4.5 V | | 2.4 | | | V |
| | | Іон = -0.5 mA | | 2.4 | | | |
| | V _{OH2} | $I_{OH} = -0.02 \text{ mA}$ | | Vcc-0.1 | | | |
| Low level output voltage | V _{OL1} | IoL = 2.1 mA, Vcc ≥ 4.5 V | | | | 0.4 | V |
| | | IoL = 1.0 mA | | | | 0.4 | |
| | V _{OL2} | IoL = 0.02 mA | | | | 0.1 | |

Remarks 1. VIN: Input voltage

Vi/o: Input / Output voltage

2. These DC characteristics are in common regardless product classification.

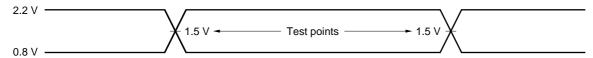


AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

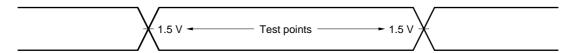
AC Test Conditions

[μ PD431000A-70L, μ PD431000A-85L, μ PD431000A-70LL, μ PD431000A-85LL]

Input Waveform (Rise and Fall Time ≤ 5 ns)



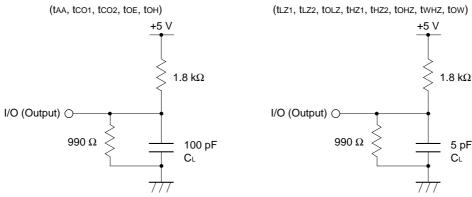
Output Waveform



Output Load

AC characteristics should be measured with the following output load conditions.

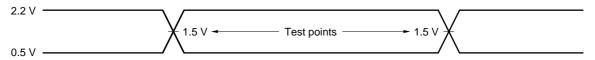
Figure 1 Figure 2



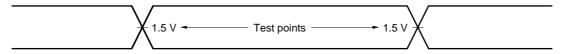
Remark CL includes capacitance of the probe and jig, and stray capacitance.

[μ PD431000A-A10, μ PD431000A-B12, μ PD431000A-B15]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

AC characteristics should be measured with the following output load conditions.

| Part number | Output | load condition |
|-----------------------------|---------------------------|---|
| | taa, tco1, tco2, toe, toh | tlz1, tlz2, tOLZ, tHZ1, tHZ2, tOHZ, tWHZ, tOW |
| μPD431000A-A10, 431000A-B12 | 1TTL + 50 pF | 1TTL + 5 pF |
| μPD431000A-B15 | 1TTL + 100 pF | 1TTL + 5 pF |



Read Cycle (1/2)

| Parameter | Symbol | | Vcc≥ | 4.5 V | | Vcc ≥ 3.0 V | | Unit | Condition |
|----------------------------------|------------------|---------|-----------------|-------|---------------|-------------|----------|------|-----------|
| | | μPD431 | μPD431000A-70 μ | | μPD431000A-85 | | 000A-A10 | | |
| | | μPD4310 | 000A-Axx | | | | | | |
| | | μPD4310 | 000A-Bxx | | | | | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Read cycle time | t rc | 70 | | 85 | | 100 | | ns | |
| Address access time | t AA | | 70 | | 85 | | 100 | ns | Note |
| /CE1 access time | tco1 | | 70 | | 85 | | 100 | ns | |
| CE2 access time | tco2 | | 70 | | 85 | | 100 | ns | |
| /OE to output valid | toe | | 35 | | 45 | | 50 | ns | |
| Output hold from address change | tон | 10 | | 10 | | 10 | | ns | |
| /CE1 to output in low impedance | t LZ1 | 10 | | 10 | | 10 | | ns | |
| CE2 to output in low impedance | tLZ2 | 10 | | 10 | | 10 | | ns | |
| /OE to output in low impedance | tolz | 5 | | 5 | | 5 | | ns | |
| /CE1 to output in high impedance | t HZ1 | | 25 | | 30 | | 35 | ns | |
| CE2 to output in high impedance | t _{HZ2} | | 25 | | 30 | | 35 | ns | |
| /OE to output in high impedance | tонz | | 25 | | 30 | | 35 | ns | |

Note See the output load.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (2/2)

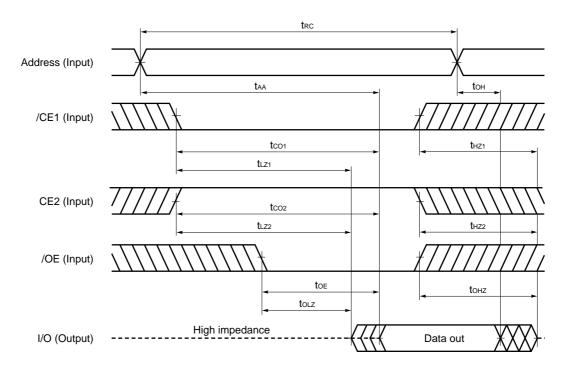
| Parameter | Symbol | | Vcc≥ | 2.7 V | | Unit | Condition |
|----------------------------------|------------------|--------|----------|--------|----------|------|-----------|
| | | μPD431 | 000A-B12 | μPD431 | 000A-B15 | | |
| | | MIN. | MAX. | MIN. | MAX. | | |
| Read cycle time | trc | 120 | | 150 | | ns | |
| Address access time | taa | | 120 | | 150 | ns | Note |
| /CE1 access time | tco1 | | 120 | | 150 | ns | |
| CE2 access time | tc02 | | 120 | | 150 | ns | |
| /OE to output valid | toe | | 60 | | 70 | ns | |
| Output hold from address change | tон | 10 | | 10 | | ns | |
| /CE1 to output in low impedance | t _{LZ1} | 10 | | 10 | | ns | |
| CE2 to output in low impedance | tLZ2 | 10 | | 10 | | ns | |
| /OE to output in low impedance | tolz | 5 | | 5 | | ns | |
| /CE1 to output in high impedance | t _{HZ1} | | 40 | | 50 | ns | |
| CE2 to output in high impedance | t HZ2 | | 40 | | 50 | ns | |
| /OE to output in high impedance | tонz | | 40 | | 50 | ns | |

Note See the output load.

Remark These AC characteristics are in common regardless of package types.



Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.



Write Cycle (1/2)

| Parameter | Symbol | | Vcc≥ | 4.5 V | | Vcc ≥ | 3.0 V | Unit | Condition |
|---------------------------------|--------|---------|---------------|-------|---------------|-------|----------|------|-----------|
| ` | | μPD431 | μPD431000A-70 | | μPD431000A-85 | | 000A-A10 | | |
| | | μPD4310 | 000A-Axx | | | | | | |
| | | μPD4310 | 000A-Bxx | | | | | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Write cycle time | twc | 70 | | 85 | | 100 | | ns | |
| /CE1 to end of write | tcw1 | 55 | | 70 | | 80 | | ns | |
| CE2 to end of write | tcw2 | 55 | | 70 | | 80 | | ns | |
| Address valid to end of write | taw | 55 | | 70 | | 80 | | ns | |
| Address setup time | tas | 0 | | 0 | | 0 | | ns | |
| Write pulse width | twp | 50 | | 60 | | 60 | | ns | |
| Write recovery time | twr | 5 | | 5 | | 0 | | ns | |
| Data valid to end of write | tow | 35 | | 35 | | 60 | | ns | |
| Data hold time | tон | 0 | | 0 | | 0 | | ns | |
| /WE to output in high impedance | twнz | | 25 | | 30 | | 35 | ns | Note |
| Output active from end of write | tow | 5 | | 5 | | 5 | | ns | |

Note See the output load.

Remark These AC characteristics are in common regardless package types.

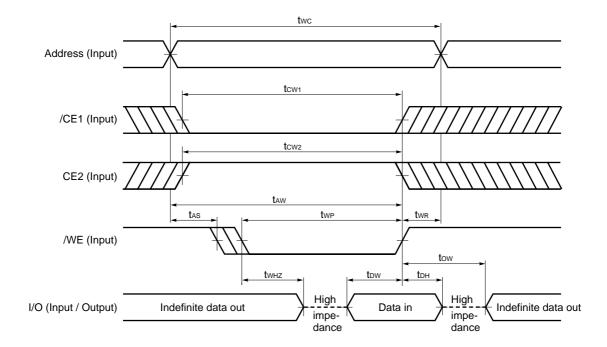
Write Cycle (2/2)

| Parameter | Symbol | Vcc ≥ 2.7 V | | | Unit | Condition | |
|---------------------------------|--------------|-------------|----------|----------------|------|-----------|------|
| | | μPD4310 | 000A-B12 | μPD431000A-B15 | | | |
| | | MIN. | MAX. | MIN. | MAX. | | |
| Write cycle time | twc | 120 | | 150 | | ns | |
| /CE1 to end of write | tcw1 | 100 | | 120 | | ns | |
| CE2 to end of write | tcw2 | 100 | | 120 | | ns | |
| Address valid to end of write | taw | 100 | | 120 | | ns | |
| Address setup time | t AS | 0 | | 0 | | ns | |
| Write pulse width | twp | 85 | | 100 | | ns | |
| Write recovery time | twr | 0 | | 0 | | ns | |
| Data valid to end of write | tow | 60 | | 80 | | ns | |
| Data hold time | tон | 0 | | 0 | | ns | |
| /WE to output in high impedance | t wnz | | 40 | | 50 | ns | Note |
| Output active from end of write | tow | 5 | | 5 | | ns | |

Note See the output load.

Remark These AC characteristics are in common regardless of package types.

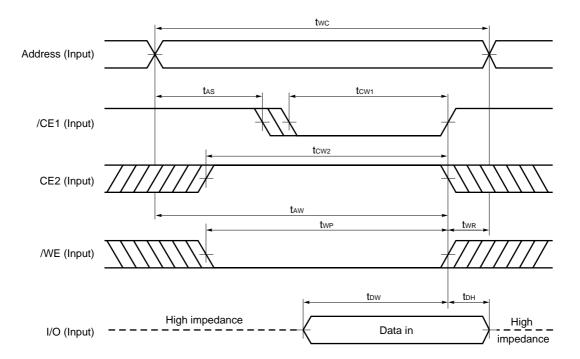
Write Cycle Timing Chart 1 (/WE Controlled)



- Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 - 2. Do not input data to the I/O pins while they are in the output state.
- Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.
 - 2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.
 - 3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

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Write Cycle Timing Chart 2 (/CE1 Controlled)

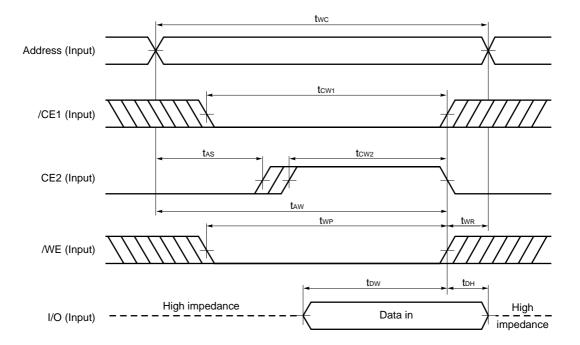


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Low Vcc Data Retention Characteristics (T_A = 0 to 70 °C)

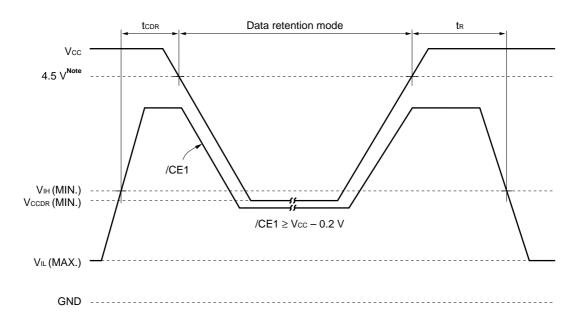
| Parameter | Symbol | Test Condition | μΡΕ | 0431000A | -xxL | μPD | 431000A- | ·xxLL | Unit |
|-------------------|------------|----------------------------------|------|----------|----------|----------|----------|----------|------|
| | | | | | | μ PC | 431000A | -Axx | |
| | | | | | | μΡΕ | 431000A | -Bxx | |
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| Data retention | Vccdr1 | /CE1 ≥ Vcc - 0.2 V, | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| supply voltage | | CE2 ≥ Vcc - 0.2 V | | | | | | | |
| | Vccdr2 | CE2 ≤ 0.2 V | 2.0 | | 5.5 | 2.0 | | 5.5 | |
| Data retention | ICCDR1 | Vcc = 3.0 V, /CE1 ≥ Vcc – 0.2 V, | | 1 | 50 Note1 | | 0.5 | 10 Note2 | μΑ |
| supply current | | CE2 ≥ Vcc – 0.2 V | | | | | | | |
| | Iccdr2 | Vcc = 3.0 V, CE2 ≤ 0.2 V | | 1 | 50 Note1 | | 0.5 | 10 Note2 | |
| Chip deselection | tcdr | | 0 | | | 0 | | | ns |
| to data retention | | | | | | | | | |
| mode | | | | | | | | | |
| Operation | t R | | 5 | | | 5 | | | ms |
| recovery time | | | | | | | | | |

Notes 1. 15 μ A (TA \leq 40 $^{\circ}$ C)

2. $3 \mu A (T_A \le 40 \, ^{\circ}C)$

Data Retention Timing Chart

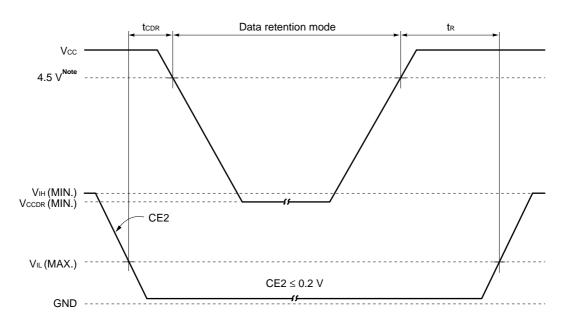
(1) /CE1 Controlled



Note A version: 3.0 V, B version: 2.7 V

Remark On the data retention mode by controlling /CE1, the input level of CE2 must be CE2 \geq Vcc - 0.2 V or CE2 \leq 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

(2) CE2 Controlled

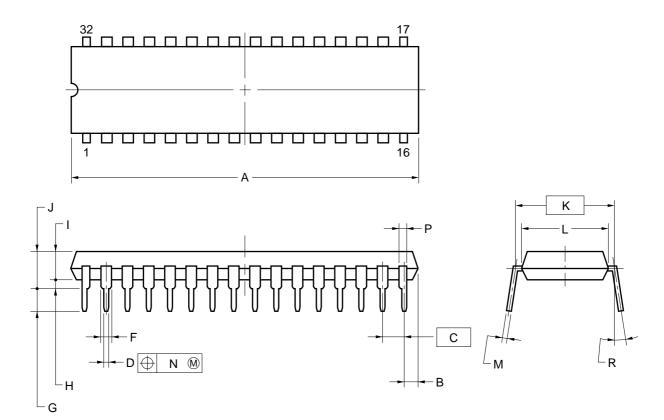


Note A version: 3.0 V, B version: 2.7 V

Remark On the data retention mode by controlling CE2, the other pins (/CE1, Address, I/O, /WE, /OE) can be in high impedance state.

★ Package Drawings

32-PIN PLASTIC DIP (15.24mm(600))



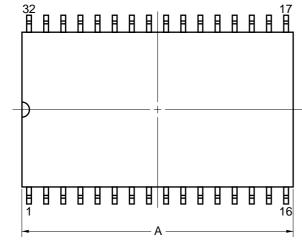
NOTES

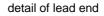
- 1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.
- 2. Item "K" to center of leads when formed parallel.

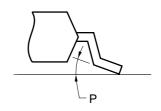
| ITEM | MILLIMETERS |
|------|------------------------|
| Α | 40.64 MAX. |
| В | 1.27 MAX. |
| С | 2.54 (T.P.) |
| D | 0.50±0.10 |
| F | 1.1 MIN. |
| G | 3.2±0.3 |
| Н | 0.51 MIN. |
| ı | 4.31 MAX. |
| J | 5.08 MAX. |
| K | 15.24 (T.P.) |
| L | 13.2 |
| М | $0.25^{+0.10}_{-0.05}$ |
| N | 0.25 |
| Р | 0.9 MIN. |
| R | 0 - 15° |
| | |

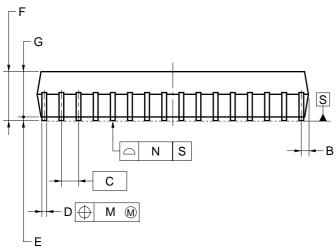
P32C-100-600A-2

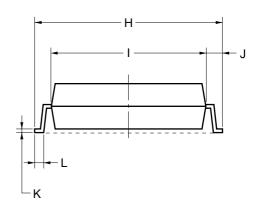
32-PIN PLASTIC SOP (13.34 mm (525))











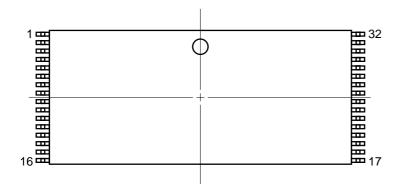
NOTE

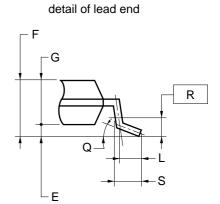
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

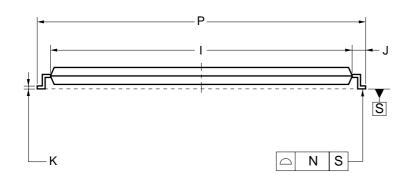
| ITEM | MILLIMETERS |
|------|--------------------------|
| Α | 20.61 MAX. |
| В | 0.78 MAX. |
| С | 1.27 (T.P.) |
| D | $0.40^{+0.10}_{-0.05}$ |
| Е | 0.15±0.05 |
| F | 2.95 MAX. |
| G | 2.7 |
| Н | 14.1±0.3 |
| 1 | 11.3 |
| J | 1.4±0.2 |
| К | $0.20^{+0.10}_{-0.05}$ |
| L | 0.8±0.2 |
| М | 0.12 |
| N | 0.10 |
| P | 3° ^{+7°} -3° |
| | |

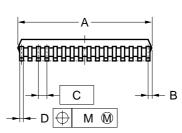
P32GW-50-525A-1

32-PIN PLASTIC TSOP(I) (8x20)









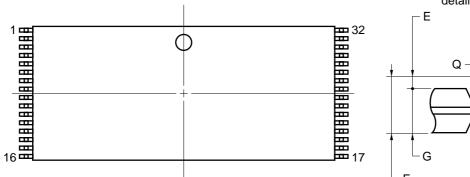
NOTES

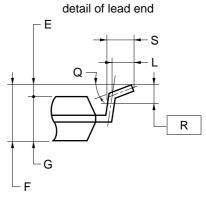
- Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash : $8.3 \ \text{mm} \ \text{MAX.}$)

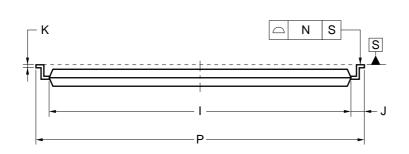
| ITEM | MILLIMETERS |
|------|-------------|
| A | 8.0±0.1 |
| В | 0.45 MAX. |
| С | 0.5 (T.P.) |
| D | 0.22±0.05 |
| Е | 0.1±0.05 |
| F | 1.2 MAX. |
| G | 0.97±0.08 |
| - 1 | 18.4±0.1 |
| J | 0.8±0.2 |
| K | 0.145±0.05 |
| L | 0.5 |
| М | 0.10 |
| N | 0.10 |
| P | 20.0±0.2 |
| Q | 3°+5° |
| R | 0.25 |
| S | 0.60±0.15 |

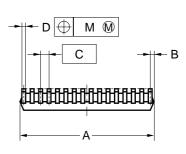
S32GZ-50-KJH1-2

32-PIN PLASTIC TSOP(I) (8x20)









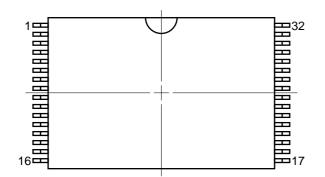
NOTES

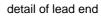
- 1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash: 8.3 mm MAX.)

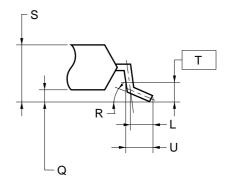
| ITEM | MILLIMETERS |
|------|--------------------|
| Α | 8.0±0.1 |
| В | 0.45 MAX. |
| С | 0.5 (T.P.) |
| D | 0.22±0.05 |
| Е | 0.1±0.05 |
| F | 1.2 MAX. |
| G | 0.97±0.08 |
| ı | 18.4±0.1 |
| J | 0.8±0.2 |
| K | 0.145±0.05 |
| L | 0.5 |
| М | 0.10 |
| N | 0.10 |
| Р | 20.0±0.2 |
| Q | 3°+5° |
| R | 0.25 |
| S | 0.60±0.15 |
| | 20007 50 1/1/114 0 |

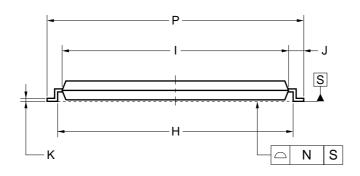
S32GZ-50-KKH1-2

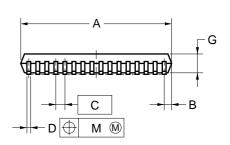
32-PIN PLASTIC TSOP(I) (8x13.4)











NOTES

- Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

| ITEM | MILLIMETERS |
|------|---------------------------|
| Α | 8.0±0.1 |
| В | 0.45 MAX. |
| С | 0.5 (T.P.) |
| D | 0.22±0.05 |
| G | 1.0±0.05 |
| Н | 12.4±0.2 |
| I | 11.8±0.1 |
| J | 0.8±0.2 |
| K | $0.145^{+0.025}_{-0.015}$ |
| L | 0.5 |
| М | 0.08 |
| N | 0.08 |
| Р | 13.4±0.2 |
| Q | 0.1±0.05 |
| R | 3°+5° -3° |
| S | 1.2 MAX. |
| Т | 0.25 |
| U | 0.6±0.15 |
| | |

P32GU-50-9JH-2



Recommended Soldering Conditions

The following conditions must be met when soldering conditions of the μ PD431000A.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μPD431000AGW-xxLL : 32-PIN PLASTIC SOP (13.34 mm (525)) μPD431000AGW-xxLL : 32-PIN PLASTIC SOP (13.34 mm (525)) μPD431000AGW-Axx : 32-PIN PLASTIC SOP (13.34 mm (525)) μPD431000AGW-Bxx : 32-PIN PLASTIC SOP (13.34 mm (525)) μPD431000AGZ-xxL-KJH : 32-PIN PLASTIC TSOP(I) (8x20) (Normal bent) μPD431000AGZ-xxLL-KJH : 32-PIN PLASTIC TSOP(I) (8x20) (Normal bent) μPD431000AGZ-xxLL-KKH : 32-PIN PLASTIC TSOP(I) (8x20) (Reverse bent) μPD431000AGZ-Bxx-KJH : 32-PIN PLASTIC TSOP(I) (8x20) (Normal bent) μPD431000AGZ-Bxx-KKH : 32-PIN PLASTIC TSOP(I) (8x20) (Reverse bent) μPD431000AGZ-Bxx-KKH : 32-PIN PLASTIC TSOP(I) (8x20) (Reverse bent) μPD431000AGU-Bxx-9JH : 32-PIN PLASTIC TSOP(I) (8x13.4) (Normal bent)

Please consult with our sales offices.

Types of Through Hole Mount Device

 μ PD431000ACZ-xxL: 32-PIN PLASTIC DIP (15.24 mm (600)) μ PD431000ACZ-xxLL: 32-PIN PLASTIC DIP (15.24 mm (600))

| Soldering process | Soldering conditions | | |
|--------------------------------|--|--|--|
| Wave soldering (Only to leads) | Solder temperature: 260 °C or below, Flow time: 10 seconds or below | | |
| Partial heating method | Pin temperature : 300 °C or below, Time: 3 seconds or below (Per one lead) | | |

Caution Do not jet molten solder on the surface of package.

Data Sheet M11657EJAV0DS 25

NEC μ PD431000A

[MEMO]

NOTES FOR CMOS DEVICES -

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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M8E 00.4