

HD74SSTV16859

1:2 13-bit SSTL_2 Registered Buffer

REJ03D0832-0900
(Previous: ADE-205-337H)
Rev.9.00
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Description

The HD74SSTV16859 is a 1:2 13-bit registered buffer designed for 2.3 V to 2.7 V V_{CC} operation and LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input.

Data flow from D to QA, QB is controlled by differential clock pins ($\overline{\text{CLK}}$, CLK) and the $\overline{\text{RESET}}$. Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ($\overline{\text{CLK}}$) must be used to maintain noise margins. When $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

Features

- Supports LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input
- Differential SSTL_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74SSTV16859TEL	TSSOP-64 pin	PTSP0064KA-A (TTP-64DV)	T	EL (1,000 pcs / Reel)

Function Table

Inputs				Outputs	
$\overline{\text{RESET}}$	$\overline{\text{CLK}}$	CLK	D	QA	QB
L	X	X	X	L	L
H	↓	↑	H	H	H
H	↓	↑	L	L	L
H	L or H	H or L	X	Q ₀ ^{*1}	Q ₀ ^{*1}

H : High level

L : Low level

X : Immaterial

↑ : Low to high transition

↓ : High to low transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement

Q12A	1	64	V _{DDQ}
Q11A	2	63	GND
Q10A	3	62	D12
Q09A	4	61	D11
Q08A	5	60	V _{CC}
V _{DDQ}	6	59	V _{DDQ}
GND	7	58	GND
Q07A	8	57	D10
Q06A	9	56	D9
Q05A	10	55	D8
Q04A	11	54	GND
Q03A	12	53	D7
Q02A	13	52	D6
Q01A	14	51	RESET
GND	15	50	GND
Q00A	16	49	CLK
Q12B	17	48	CLK
V _{DDQ}	18	47	V _{DDQ}
Q11B	19	46	V _{CC}
Q10B	20	45	V _{REF}
Q09B	21	44	D5
Q08B	22	43	GND
Q07B	23	42	D4
Q06B	24	41	D3
Q05B	25	40	D2
GND	26	39	GND
V _{DDQ}	27	38	V _{DDQ}
Q04B	28	37	V _{CC}
Q03B	29	36	D1
Q02B	30	35	D0
Q01B	31	34	GND
Q00B	32	33	V _{DDQ}

(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC} or V_{DDQ}	-0.5 to 3.6	V	
Input voltage ^{*1}	V_I	-0.5 to $V_{DDQ}+0.5$	V	
Output voltage ^{*1}	V_O	-0.5 to $V_{DDQ}+0.5$	V	
Input clamp current	I_{IK}	±50	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{DDQ}
V_{CC} , V_{DDQ} or GND current / pin	I_{CC} , I_{DDQ} or I_{GND}	±100	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air)	P_T	1	W	TSSOP
Storage temperature	T_{stg}	-65 to +150	°C	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

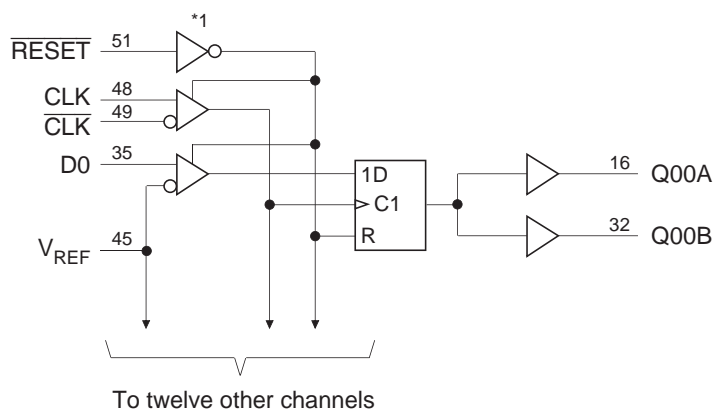
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	V_{DDQ}	2.5	2.7	V	
Output supply voltage	V_{DDQ}	2.3	2.5	2.7	V	
Reference voltage	V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination voltage	V_{TT}	$V_{REF}-40$ mV	V_{REF}	$V_{REF}+40$ mV	V	
Input voltage	V_I	0	—	V_{CC}	V	
AC high level input voltage	V_{IH}	$V_{REF}+310$ mV	—	—	V	D
AC low level input voltage	V_{IL}	—	—	$V_{REF}-310$ mV	V	D
DC high level input voltage	V_{IH}	$V_{REF}+150$ mV	—	—	V	D
DC low level input voltage	V_{IL}	—	—	$V_{REF}-150$ mV	V	D
High level input voltage	V_{IH}	1.7	—	$V_{DDQ}+0.3$	V	RESET
Low level input voltage	V_{IL}	-0.3	—	0.7	V	RESET
Differential input voltage	(Common mode range)	V_{CMR}	0.97	1.53	V	CLK, $\overline{\text{CLK}}$
	(Minimum peak to peak input)	V_{PP}	360	—	mV	CLK, $\overline{\text{CLK}}$
High level output current	I_{OH}	—	—	-20	mA	
Low level output current	I_{OL}	—	—	20	mA	
Operating temperature	T_a	0	—	70	°C	

Note: The RESET input of the device must be held at V_{DDQ} or GND to ensure proper device operation. The differential inputs must not be floating, unless RESET is low.

Logic Diagram



Note: 1. $\overline{\text{RESET}}$ input gate is connected to V_{DDQ} .

Electrical Characteristics

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input diode voltage	V_{IK}	2.3	—	—	-1.2	V	$I_{IN} = -18 \text{ mA}$
Output voltage	V_{OH}	2.3 to 2.7	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100 \mu\text{A}$
		2.3	1.95	—	V_{DDQ}		$I_{OH} = -16 \text{ mA}$
	V_{OL}	2.3 to 2.7	—	—	0.2		$I_{OL} = 100 \mu\text{A}$
		2.3	0	—	0.35		$I_{OL} = 16 \text{ mA}$
Input current (All inputs)	I_{IN}	2.7	—	—	± 5	μA	$V_{IN} = 2.7 \text{ V}$ or 0
Quiescent supply current	I_{CC}^{*2}	2.7	—	—	45	mA	$V_{IN} = V_{IH(AC)}$ or $V_{IL(AC)}$, $I_O = 0$
Standby current	$I_{CC(stdy)}$	2.7	—	—	10	μA	$\overline{\text{RESET}} = \text{GND}$
Dynamic operating clock only	I_{CCD}^{*2}	2.7	—	—	90	$\mu\text{A}/$ clock MHz	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle
Dynamic operating per each data input	I_{CCD}^{*2}	2.7	—	—	20	$\mu\text{A}/$ clock MHz/ data input	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.
Output high ^{*3}	r_{OH}	2.3 to 2.7	7	—	22 ^{*4}	Ω	$I_{OH} = -20 \text{ mA}$
Output low ^{*3}	r_{OL}	2.3 to 2.7	7	—	22 ^{*4}	Ω	$I_{OL} = 20 \text{ mA}$
$ r_{OH} - r_{OL} $ each separate bit ^{*3}	$r_{O(\Delta)}$	2.5	—	—	4	Ω	$I_O = 20 \text{ mA}$, $T_a = 25^\circ\text{C}$
Input capacitance	Data inputs	C_{IN}	2.5 ^{*1}	—	3.5	pF	$V_I = V_{REF} \pm 310 \text{ mV}$
	CLK and $\overline{\text{CLK}}$			—	3.5		$V_{CMR} = 1.25 \text{ V}$, $V_{PP} = 360 \text{ mV}$
	$\overline{\text{RESET}}$			3.0	—		$V_I = V_{CC}$ or GND

Notes: 1. All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_a = 25^\circ\text{C}$.

2. Total $I_{CC} (\text{max}) = I_{CC} + \{I_{CCD} (\text{clock}) \times f(\text{clock})\} + \{I_{CCD} (\text{Data}) \times 1/2f(\text{clock}) \times 13\}$

3. This is effective in the case that it did terminate by resistance.

4. See figure. 1, 2

Switching Characteristics

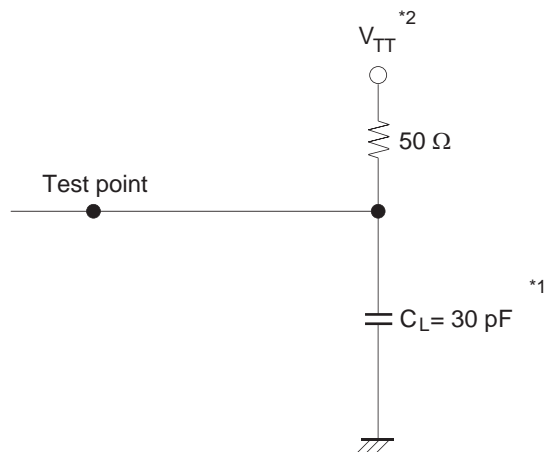
Item		Symbol	$V_{CC} = 2.5 \pm 0.2 \text{ V}$		Unit	Test Condition
			Min	Max		
Clock frequency ^{*1}		f_{clock}	—	200	MHz	
Setup time	Fast slew rate ^{*4, 6}	t_{su}	0.75	—	ns	Data before $\text{CLK}\uparrow$, $\text{CLK}\downarrow$
	Slow slew rate ^{*5, 6}		0.9	—		
Hold time	Fast slew rate ^{*4, 6}	t_{h}	0.75	—	ns	Data after $\text{CLK}\uparrow$, $\text{CLK}\downarrow$
	Slow slew rate ^{*5, 6}		0.9	—		
Differential inputs active time		t_{act}	22	—	ns	Data inputs must be low after RESET high.
Differential inputs inactive time		t_{inact}	22	—	ns	Data and clock inputs must be held at valid levels (not floating) after RESET low.
Pulse width		t_{w}	2.5	—	ns	CLK , CLK "H" or "L"
Output slew ^{*3}		t_{SL}	1	4	volt/ns	

($C_L = 30 \text{ pF}$, $R_L = 50 \Omega$, $V_{\text{REF}} = V_{\text{TT}} = V_{\text{DDQ}} \times 0.5$)

Item	Symbol	$V_{CC} = 2.5 \pm 0.2 \text{ V}$			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max			
Maximum clock frequency	f_{max}	200	—	—	MHz		
Propagation delay time ^{*2}	$t_{\text{PLH}}, t_{\text{PHL}}$	1.1	—	2.8	ns	CLK , CLK	QA, QB
	t_{PHL}	—	—	5.0		RESET	QA, QB

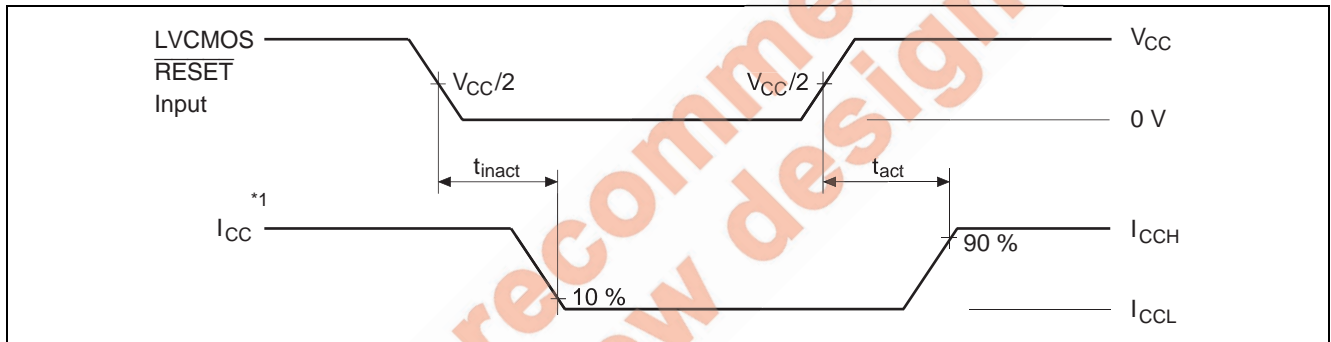
- Notes:
1. Although the clock is differential, all timing is relative to CLK going high and CLK going low.
 2. This timing relationship is specified into test load (see waveforms – 3, 4) with all of the outputs switching.
 3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
 4. For data signal input slew rate $\geq 1 \text{ V/ns}$.
 5. For data signal input slew rate $\geq 0.5 \text{ V/ns}$ and $< 1 \text{ V/ns}$.
 6. CLK , CLK signals input slew rates are $\geq 1 \text{ V/ns}$.

Test Circuit

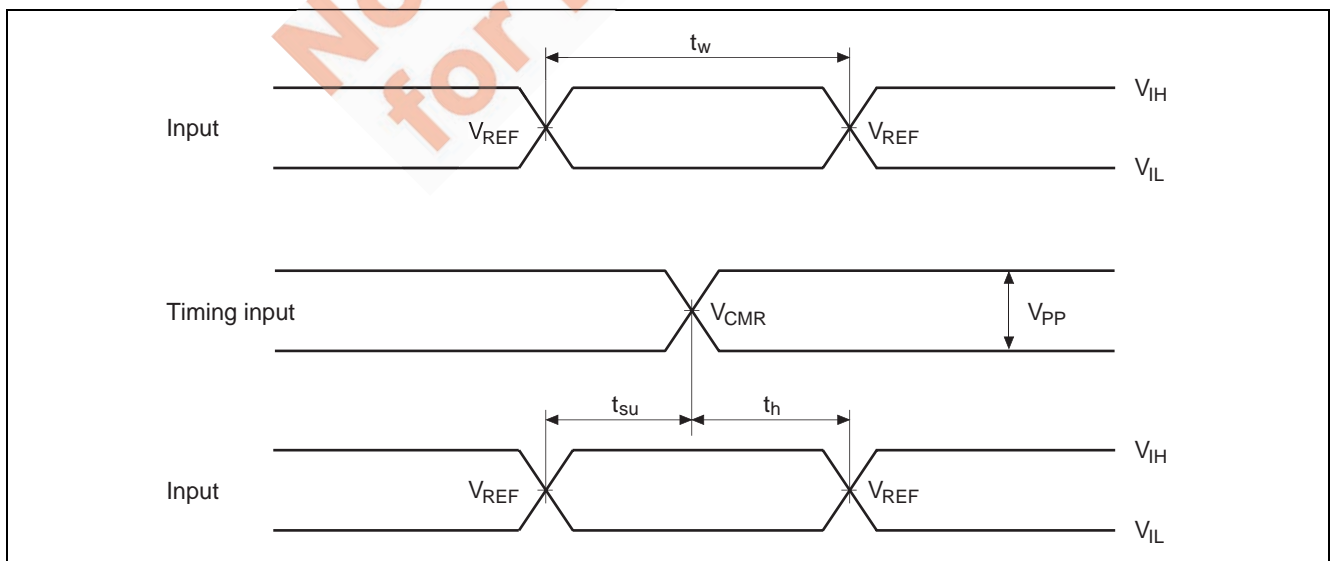


- Notes:
1. C_L includes probe and jig capacitance.
 2. $V_{TT} = V_{REF} = V_{DDQ} \times 0.5$

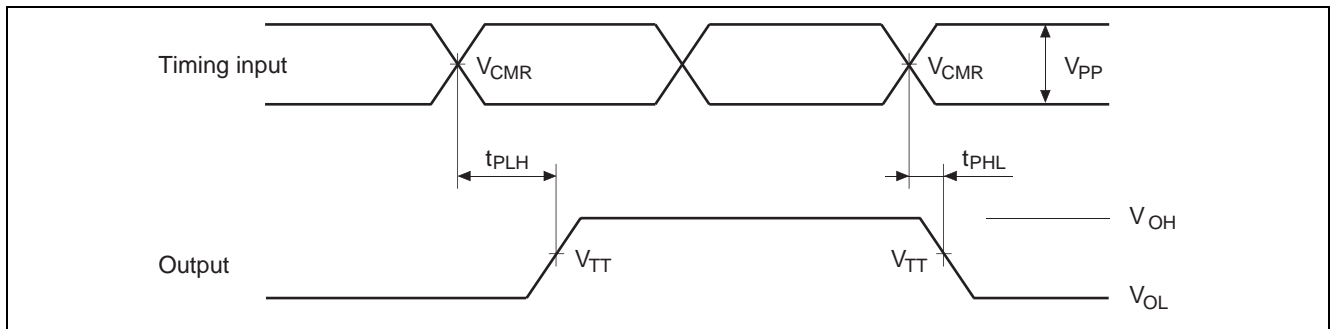
Waveforms – 1



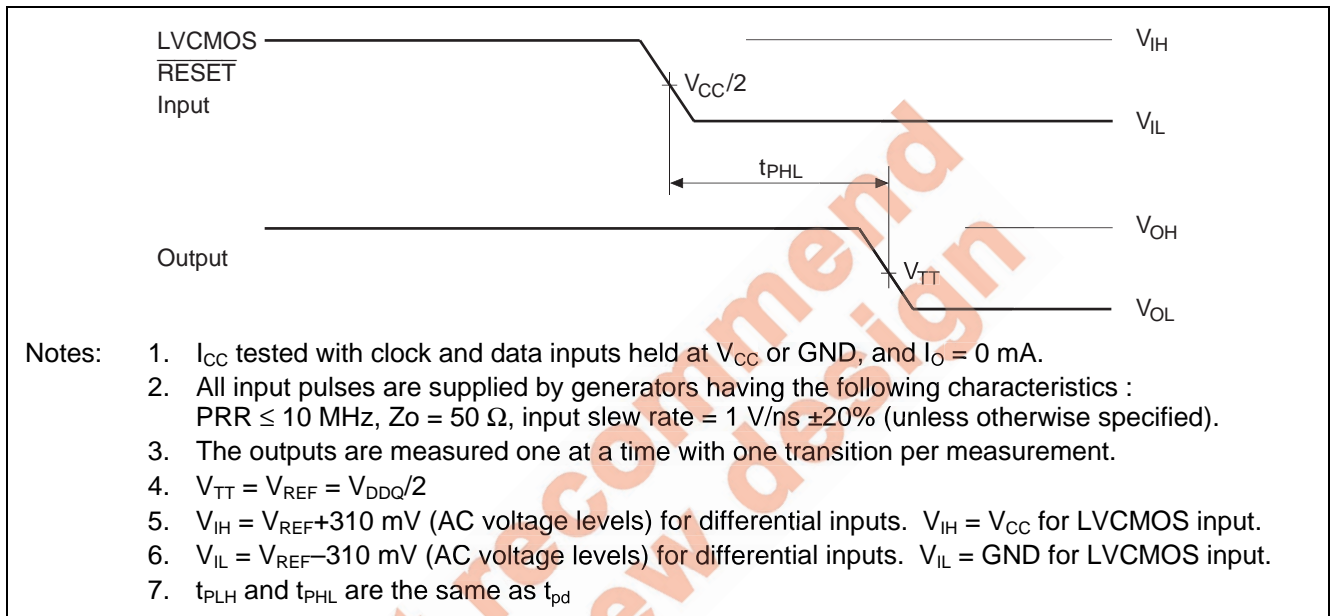
Waveforms – 2



Waveforms – 3



Waveforms – 4



Application Data

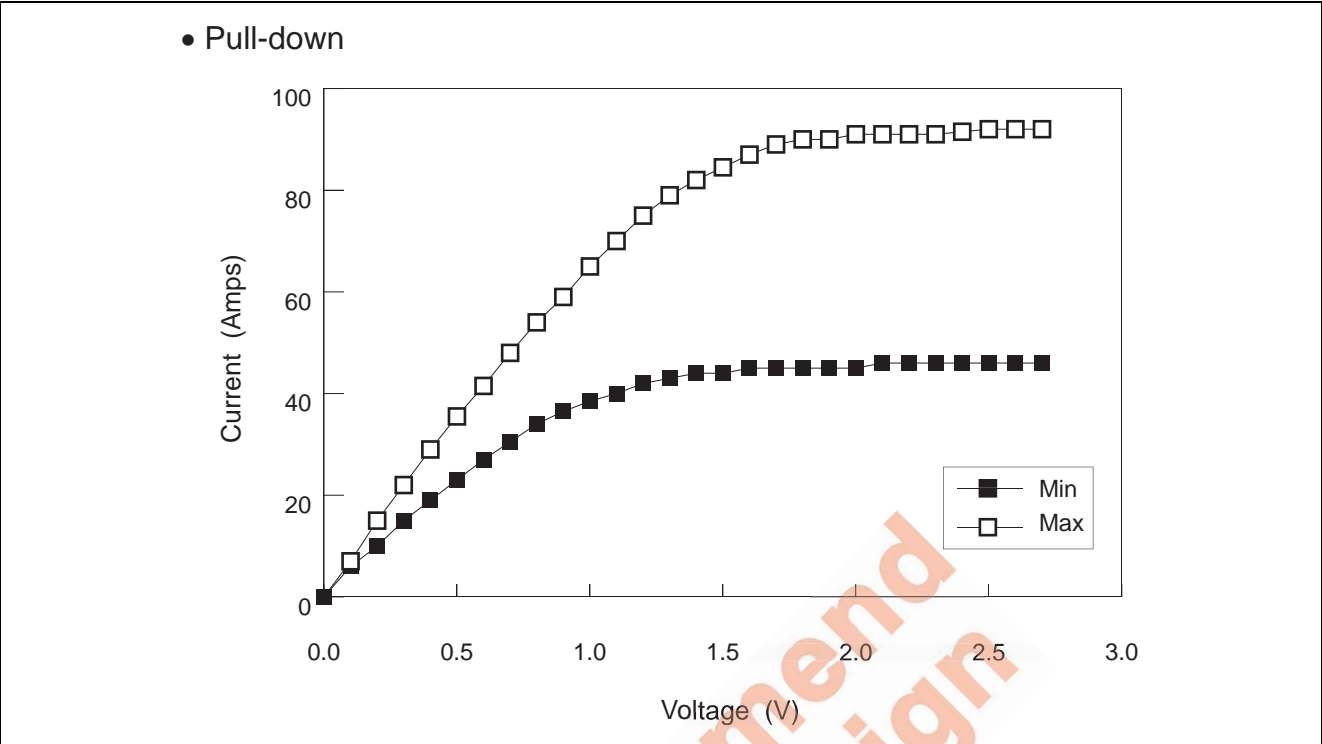


Figure 1

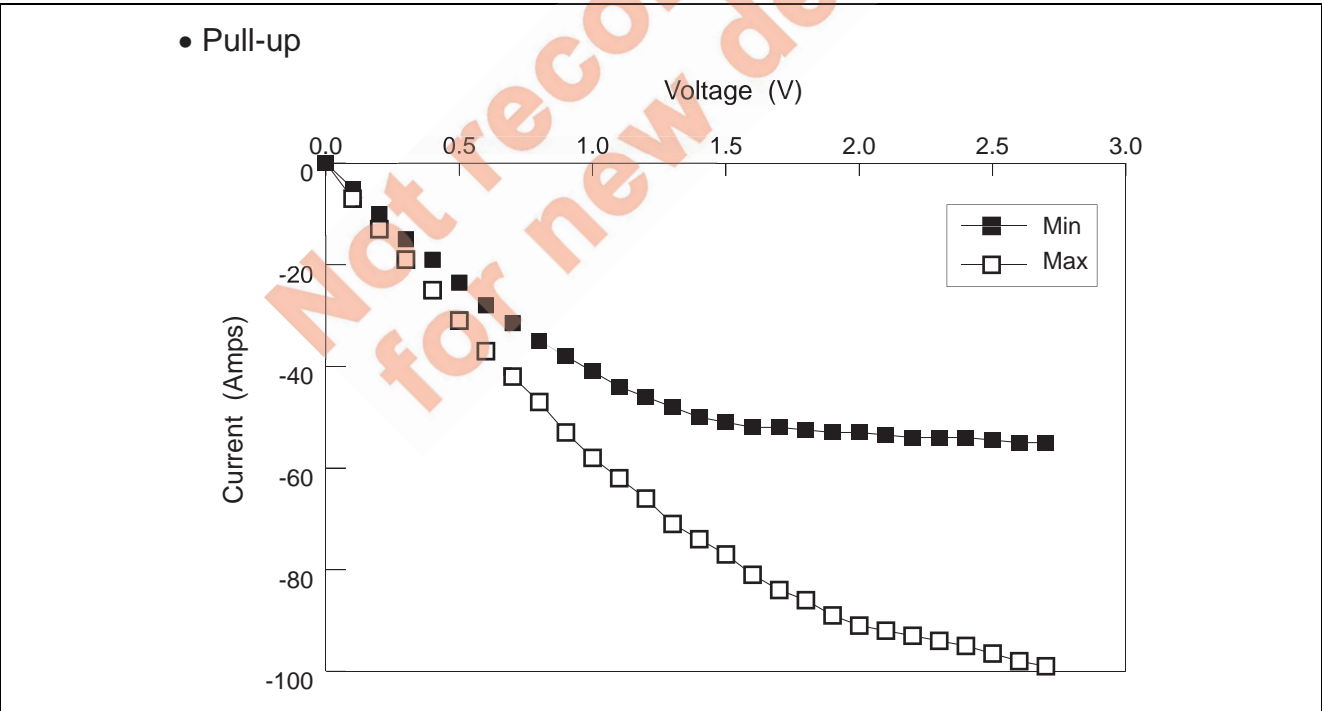
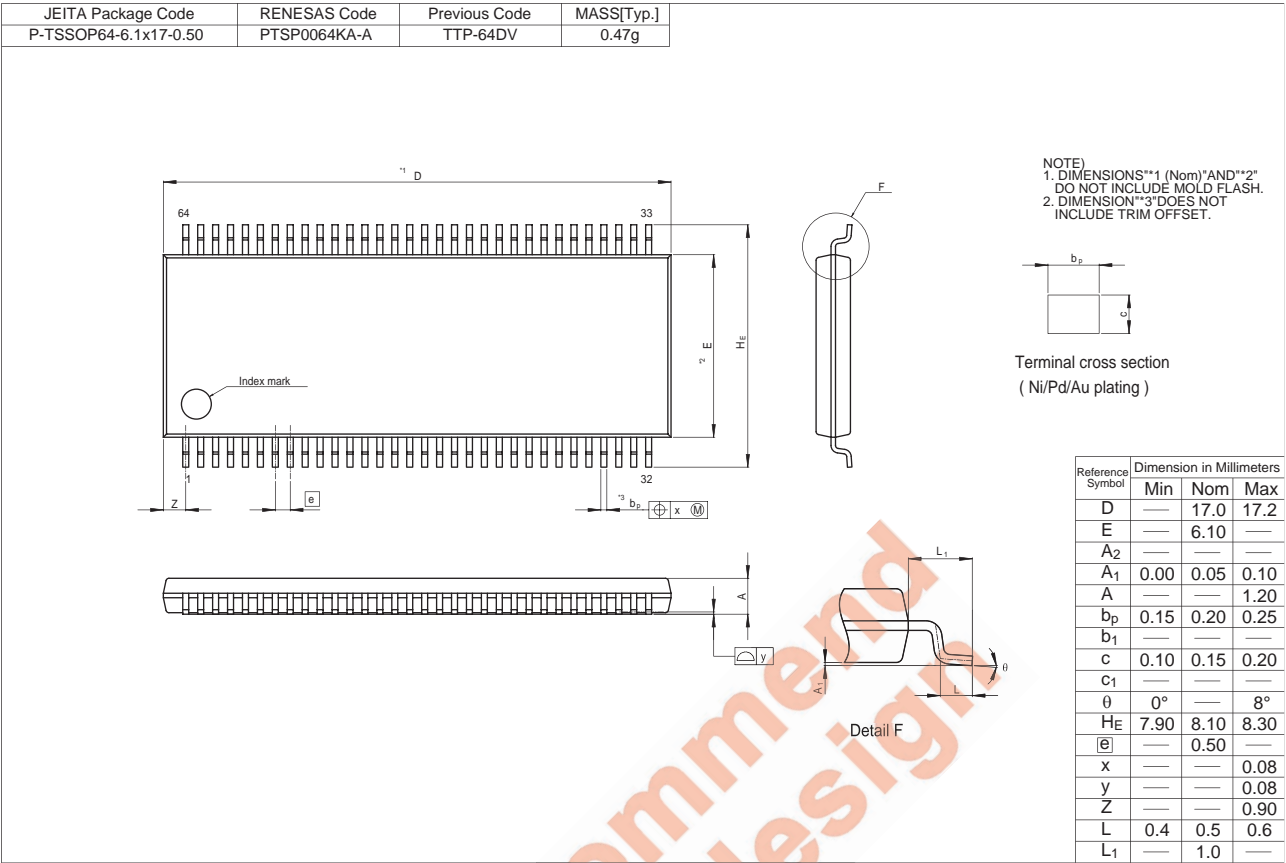


Figure 2

Curve Data

Voltage (V)	Pull-down		Pull-up	
	I (mA)	I (mA)	I (mA)	I (mA)
	Min	Max	Min	Max
0.0	0	0	0	0
0.1	6	7	-5	-7
0.2	10	15	-10	-13
0.3	15	22	-15	-19
0.4	19	29	-19	-25
0.5	23	35.5	-23.5	-31
0.6	27	41.5	-28	-37
0.7	30.5	48	-31.5	-42
0.8	34	54	-35	-47
0.9	36.5	59	-38	-53
1.0	38.5	65	-41	-58
1.1	40	70	-44	-62
1.2	42	75	-46	-66
1.3	43	79	-48	-71
1.4	44	82	-50	-74
1.5	44	84.5	-51	-77
1.6	45	87	-52	-81
1.7	45	89	-52	-84
1.8	45	90	-52.5	-86
1.9	45	90	-53	-89
2.0	45	91	-53	-91
2.1	46	91	-53.5	-92
2.2	46	91	-54	-93
2.3	46	91	-54	-94
2.4	46	91.5	-54	-95
2.5	46	92	-54.5	-96.5
2.6	46	92	-55	-98
2.7	46	92	-55	-99

Package Dimensions



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