

# Schmitt-Trigger Inverter/ CMOS Logic Level Shifter with LSTTL-Compatible Inputs

**L74VHC1GT14**

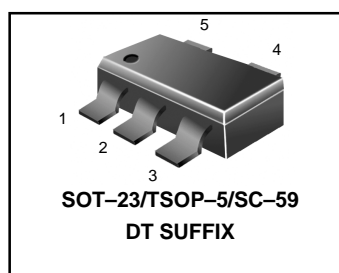
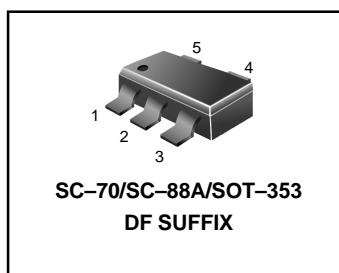
The L74VHC1GT14 is a single gate CMOS Schmitt-trigger inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

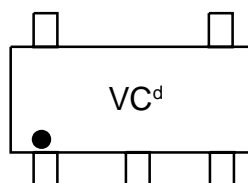
The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The L74VHC1GT14 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the L74VHC1GT14 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when  $V_{CC} = 0$  V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc. The LMC74VHC1GT14 can be used to enhance noise immunity or to square up slowly changing waveforms.

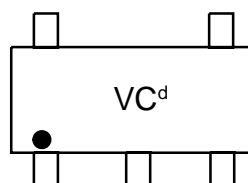
- High Speed:  $t_{PD} = 4.5$  ns (Typ) at  $V_{CC} = 5$  V
- Low Power Dissipation:  $I_{CC} = 2$  mA (Max) at  $T_A = 25^\circ\text{C}$
- TTL-Compatible Inputs:  $V_{IL} = 0.8$  V;  $V_{IH} = 2.0$  V
- CMOS-Compatible Outputs:  $V_{OH} > 0.8 V_{CC}$ ;  
 $V_{OL} < 0.1 V_{CC}$  @ Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 100; Equivalent Gates = 25



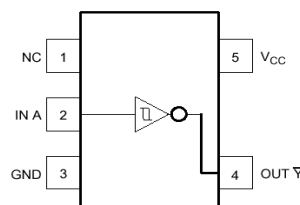
### MARKING DIAGRAMS



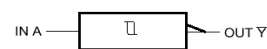
Pin 1  
d = Date Code



Pin 1  
d = Date Code



**Figure 1. Pinout (Top View)**



**Figure 2. Logic Symbol**

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT $\bar{Y}$
5	$V_{CC}$

FUNCTION TABLE	
Inputs	Output
A	$\bar{Y}$
L	H
H	L

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

### L74VHC1GT14

#### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	- 0.5 to + 7.0	V
$V_{IN}$	DC Input Voltage	- 0.5 to + 7.0	V
$V_{OUT}$	DC Output Voltage	$V_{CC}=0$ High or Low State	- 0.5 to + 7.0 -0.5 to $V_{CC} + 0.5$
$I_{IK}$	Input Diode Current	-20	mA
$I_{OK}$	Output Diode Current	$V_{OUT} < GND; V_{OUT} > V_{CC}$	+20 mA
$I_{OUT}$	DC Output Current, per Pin	+ 25	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND	+50	mA
$P_D$	Power dissipation in still air	SC-88A, TSOP-5	200 mW
$\theta_{JA}$	Thermal resistance	SC-88A, TSOP-5	333 °C/W
$T_L$	Lead Temperature, 1 mm from Case for 10 s	260	°C
$T_J$	Junction Temperature Under Bias	+ 150	°C
$T_{stg}$	Storage temperature	-65 to +150	°C
$V_{ESD}$	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 > 200 N/A V
$I_{LATCH-UP}$	Latch-Up Performance	Above $V_{CC}$ and Below GND at 125°C (Note 5)	± 500 mA

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22-A114-A
3. Tested to EIA/JESD22-A115-A
4. Tested to JESD22-C101-A
5. Tested to EIA/JESD78

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	3.0	5.5	V
$V_{IN}$	DC Input Voltage	0.0	5.5	V
$V_{OUT}$	DC Output Voltage	$V_{CC} = 0$ High Low State	0.0 $V_{CC}$	V
$T_A$	Operating Temperature Range	- 55	+ 125	°C
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 3.3 \pm 0.3 V$ $V_{CC} = 5.0 \pm 0.5 V$	0 0	100 20 ns/V

#### DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

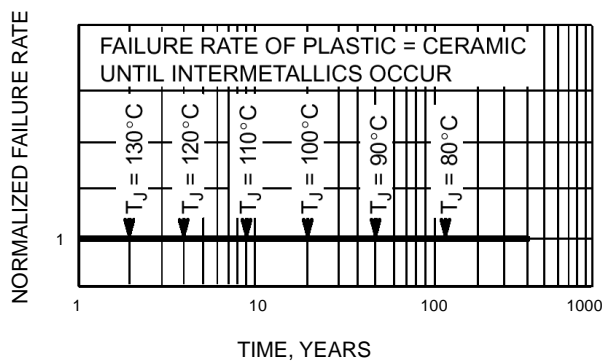


Figure 3. Failure Rate vs. Time Junction Temperature

**L74VHC1GT14**
**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>T+</sub>	Positive Threshold Voltage		3.0	1.20	1.40	1.60		1.6		1.60	V
			4.5	1.58	1.74	2.00		2.0		2.0	
			5.5	1.79	1.94	2.10		2.0		2.0	
V <sub>T-</sub>	Negative Threshold Voltage		3.0	0.35	0.76	0.93	0.35		0.35		V
			4.5	0.5	1.01	1.18	0.5		0.5		
			5.5	0.6	1.13	1.29	0.6		0.6		
V <sub>H</sub>	Hysteresis Voltage		3.0	0.30	0.64	1.20	0.30	1.20	0.30	1.20	
			4.5	0.40	0.73	1.40	0.40	1.40	0.40	1.40	
			5.5	0.50	0.81	1.60	0.50	1.60	0.50	1.60	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> ≤ V <sub>T-</sub> - Min I <sub>OH</sub> = -50 μA	2.0	1.9	2.0		1.9		1.9		V
			3.0	2.9	3.0		2.9		2.9		
			4.5	4.4	4.5		4.4		4.4		
		I <sub>OH</sub> = -4 mA	3.0	2.58			2.48		2.34		
		I <sub>OH</sub> = -8 mA	4.5	3.94			3.80		3.66		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> ≥ V <sub>T+</sub> + Min <sub>L</sub> I <sub>OL</sub> = 50 μA	2.0		0.0	0.1		0.1		0.1	V
			3.0		0.0	0.1		0.1		0.1	
			4.5		0.0	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	3.0			0.36		0.44		0.52	
		I <sub>OL</sub> = 8 mA	4.5			0.36		0.44		0.52	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			2.0		20		40	μA
I <sub>CCT</sub>	Quiescent Supply Current	Input: V <sub>IN</sub> = 3.4 V	5.5			1.35		1.50		1.65	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0.0			0.5		5.0		10	μA

**AC ELECTRICAL CHARACTERISTICS** C<sub>load</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to $\bar{Y}$	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		7.0	12.8	1.0	15.0	1.0	17.0	ns
				8.4	16.3	1.0	18.5	1.0	20.5	
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		4.5	8.6	1.0	10.0	1.0	11.5	
				5.8	10.6	1.0	12.0	1.0	13.5	
C <sub>IN</sub>	Maximum Input Capacitance			5	10		10		10	pF
			<b>Typical @ 25°C, V<sub>CC</sub> = 5.0 V</b>							
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)		10						pF	

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

### L74VHC1GT14

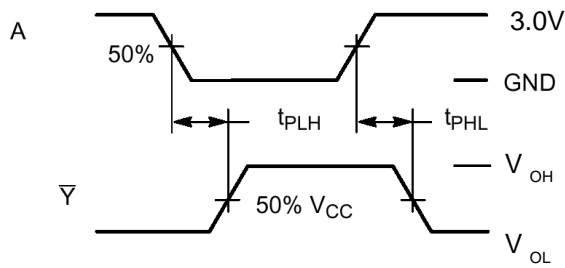
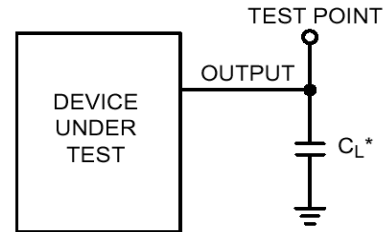


Figure 4. Switching Waveforms



\*Includes all probe and jig capacitance

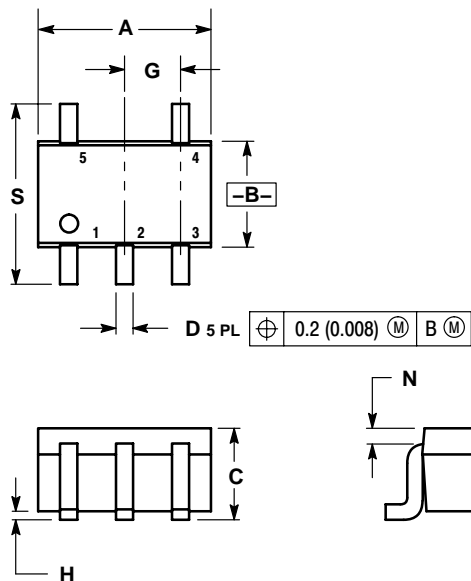
Figure 5. Test Circuit

#### DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
L74VHC1GT14DFT1	L	74	VHC1G	T14	DF	T1	SC-70/SC-88A/ SOT-353	178 mm (7 in) 3000 Unit
L74VHC1GT14DFT2	L	74	VHC1G	T14	DF	T2	SC-70/SC-88A/ SOT-353	178 mm (7 in) 3000 Unit
L74VHC1GT14DTT1	L	74	VHC1G	T14	DT	T1	SOT-23/TSOPS/ SC-59	178 mm (7 in) 3000 Unit

### L74VHC1GT14

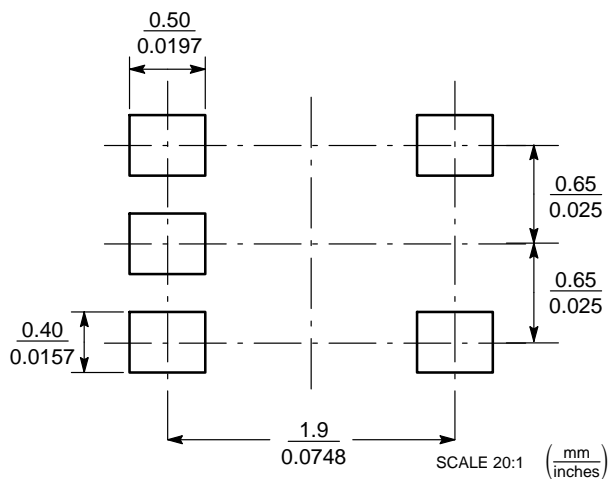
#### PACKAGE DIMENSIONS SC70-5/SC-88A/SOT-353 DF SUFFIX



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
  4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

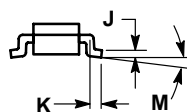
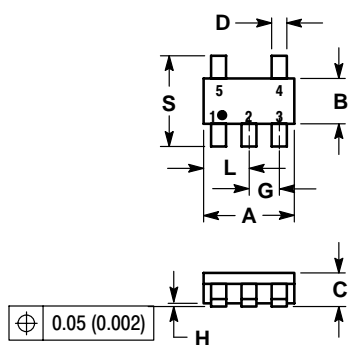
#### SOLDERING FOOTPRINT\*



## L74VHC1GT14

### PACKAGE DIMENSIONS

SOT23-5/TSOP-5/SC59-5  
DT SUFFIX



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0	10	0	10
S	2.50	3.00	0.0985	0.1181

### SOLDERING FOOTPRINT\*

