NEC

MOS INTEGRATED CIRCUIT

μPD42S4280, 424280

4 M-BIT DYNAMIC RAM
256 K-WORD BY 18-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

DESCRIPTION

The μPD42S4280, 424280 are 262 144 words by 18 bits dynamic CMOS RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

Besides, the μPD42S4280 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 44-pin plastic TSOP and 40-pin plastic SOJ.

FEATURES

- 262 144 words by 18 bits organization
- Single +5.0 V ± 10 % power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S4280-70, 424280-70	1 045.0 mW	70 ns	130 ns	45 ns
μPD42S4280-80, 424280-80	962.5 mW	80 ns	150 ns	50 ns

- The μPD42S4280 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S4280	512 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh	1.1 mW (CMOS level input)
μPD424280	512 cycles/ 8 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh	5.5 mW (CMOS level input)

- Multiplexed address inputs ..... Row address: A0 to A8, Column address: A0 to A8

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The mark ★ shows revised points.

★ ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μPD42S4280G5-70-7JF	70 ns	44-pin Plastic TSOP	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{RAS}$ only refresh $\overline{CAS}$ before $\overline{RAS}$ refresh hidden refresh
μPD42S4280G5-80-7JF	80 ns		
μPD42S4280G5-70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD42S4280G5-80-7KF	80 ns		
μPD42S4280LE-70	70 ns	40-pin Plastic SOJ	
μPD42S4280LE-80	80 ns		
μPD424280G5-70-7JF	70 ns	44-pin Plastic TSOP	$\overline{RAS}$ only refresh $\overline{CAS}$ before $\overline{RAS}$ refresh hidden refresh
μPD424280G5-80-7JF	80 ns		
μPD424280G5-70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD424280G5-80-7KF	80 ns		
μPD424280LE-70	70 ns	40-pin Plastic SOJ	
μPD424280LE-80	80 ns		

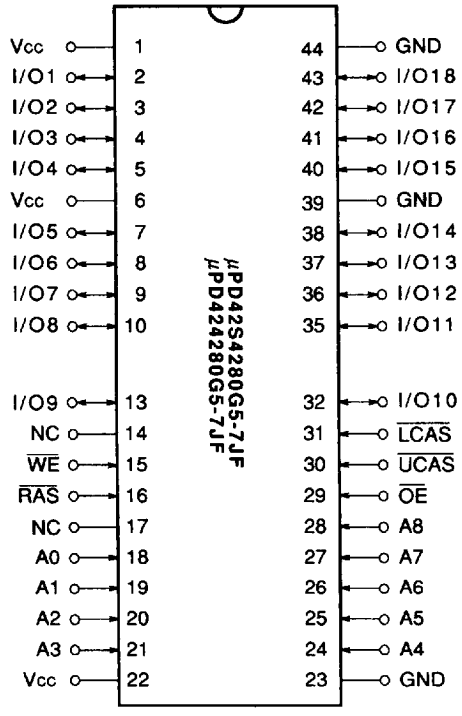
QUALITY GRADE

STANDARD

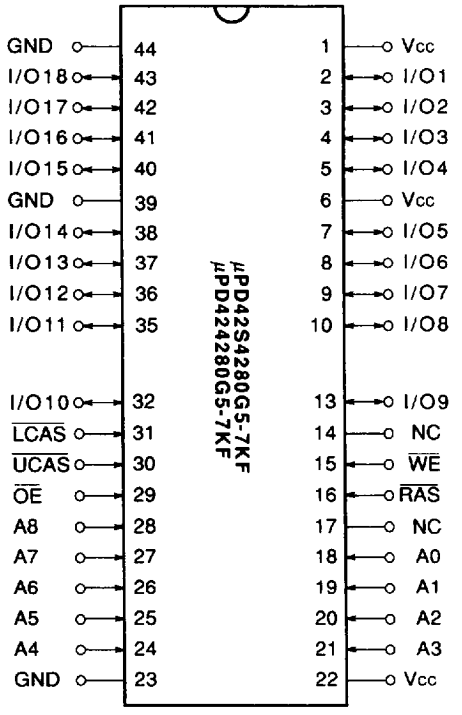
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS ★

44-pin Plastic TSOP
(Marking Side)

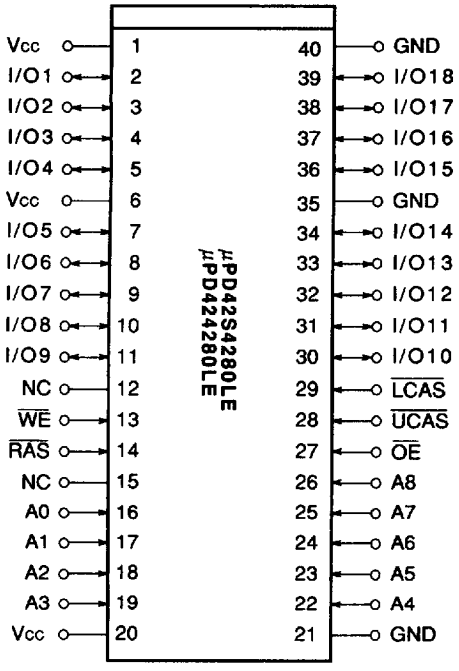


44-pin Plastic TSOP (Reverse bent)
(Marking Side)



A0 to A8	: Address Inputs
I/O1 to I/O18	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{UCAS}$	: Column Address Strobe (upper)
$\overline{LCAS}$	: Column Address Strobe (lower)
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power Supply (+5.0 V ± 10 %)
GND	: Ground
NC	: No Connection

40-pin Plastic SOJ
(Top View)



A0 to A8	: Address Inputs
I/O1 to I/O18	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{UCAS}$	: Column Address Strobe (upper)
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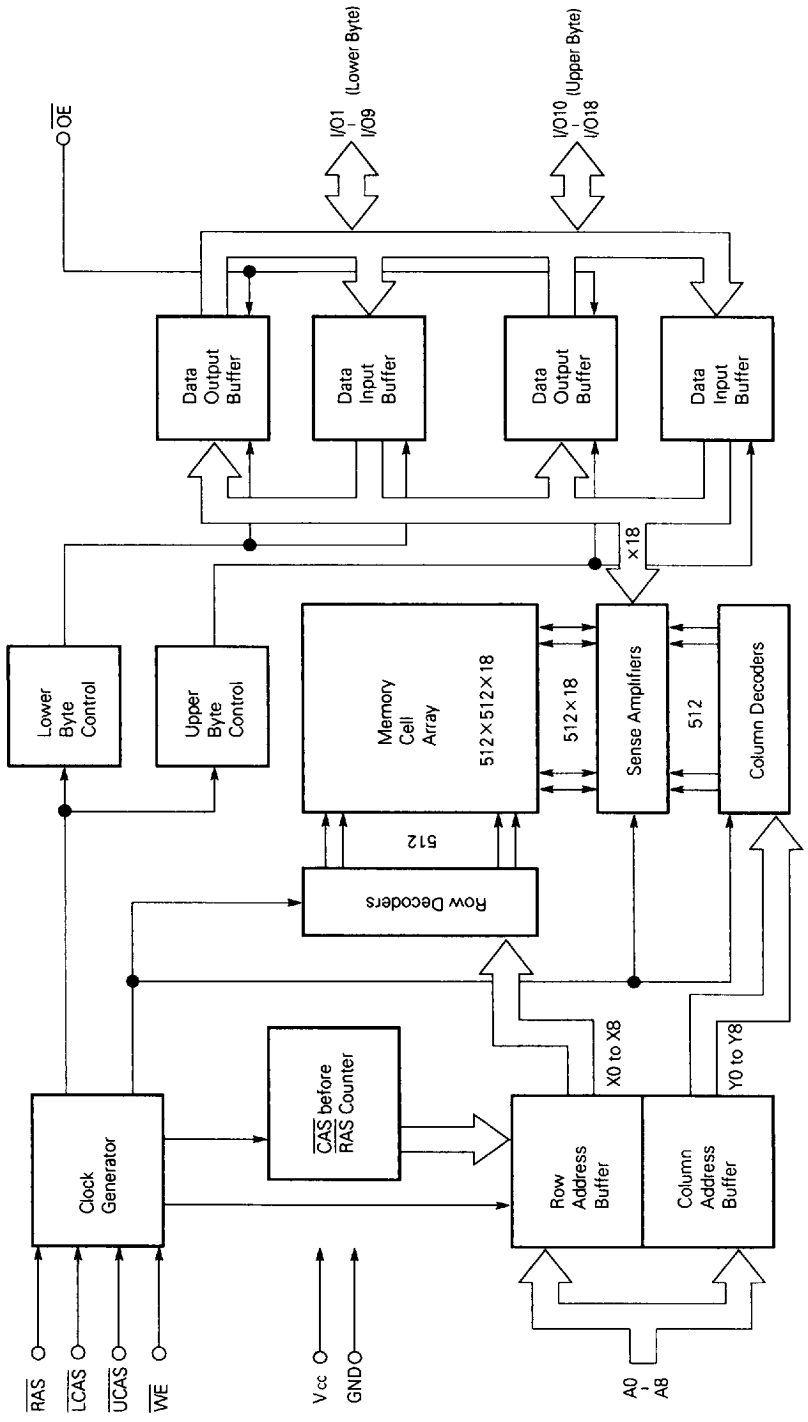
Vcc	: Power Supply (+5.0 V ± 10 %)
GND	: Ground
NC	: No Connection

BLOCK DIAGRAM



★ INPUT/OUTPUT PIN FUNCTIONS

The μPD42S4280, 424280 have input pins $\overline{RAS}$, $\overline{CAS}$ [Note], $\overline{WE}$, $\overline{OE}$, A0 to A8 and input/output pins I/O1 to I/O18.

Pin name	Input/ output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address (A0 to A8) and selecting a corresponding word line. It refreshes memory cell array of one line (9 216-bit) selected by the row address (A0 to A8). It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address (A0 to A8) and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address input)	Input	9-bit address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word (18-bit) is selected from 262 144-word by 18-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O18 (Data input/output)	Input/ output	18-bit data bus. I/O1 to I/O18 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

ELECTRICAL SPECIFICATIONS NOTE 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Voltage on Any Pin Relative to GND	V_T		−1.0 to +7.0	V
Supply Voltage	V_{CC}		−1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1.3	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS NOTE 2, 3

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low Level Input Voltage	V_{IL}		−1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

CAPACITANCE (T_a = +25 °C, f = 1 MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_{I1}	A0 to A8			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	C_D	I/O1 to I/O18			7	pF

★ **DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)**

PARAMETER		SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTE
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		190	mA	4, 5
				t_{RAC} = 80 ns		175		
Standby current	μPD42S4280	I_{CC2}	$V_{IH(MIN)} \leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		2	mA	
			V_{CC}–0.2 V $\leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.2		
	μPD424280		$V_{IH(MIN)} \leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		2		
			V_{CC}–0.2 V $\leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		1		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling, $V_{IH(MIN)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		190	mA	4, 5
				t_{RAC} = 80 ns		175		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX)}$ $\overline{CAS}$ Cycling, $t_{PC} = t_{PC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		170	mA	4, 5
				t_{RAC} = 80 ns		160		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		190	mA	4, 5
				t_{RAC} = 80 ns		175		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (512 cycles/128 ms, only for μPD42S4280)		I_{CC6}	Standby : V_{CC}–0.2 V $\leqq \overline{RAS}$ $\overline{CAS}$ before $\overline{RAS}$ refresh : 512 cycles/128 ms $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX)}$ $\overline{WE}$, $\overline{OE}$: V_{IH} Address input : V_{IH} or V_{IL} Output : Hi-Z	$t_{RAS} \leqq$ 200 ns		200	μA	4, 5
				$t_{RAS} \leqq 1$ μs		300		
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S4280)		I_{CC7}	I_O = 0 mA $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX)}$			150	μA	
Input leakage current		$I_{I(L)}$	V_I = 0 to 5.5 V all other pins except for testing pin = 0 V		–10	+10	μA	
Output leakage current		$I_{O(L)}$	Output is disabled (Hi-Z) V_O = 0 to 5.5 V		–10	+10	μA	
High level output voltage		V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = 2.1 mA			0.4	V	

AC CHARACTERISTICS ★

(Recommended Operating Conditions unless otherwise noted) NOTE 6, 7 (1/2)

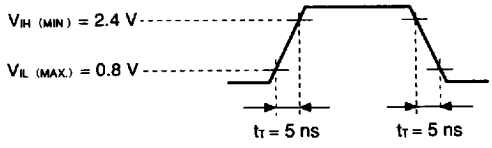
PARAMETER	SYMBOL	t_{RAC} = 70 ns		t_{RAC} = 80 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	130		150		ns	8
Read Modify Write Cycle Time	t_{RWC}	175		200		ns	8
Fast Page Mode Cycle Time	t_{PC}	45		50		ns	8
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	90		105		ns	8
Access Time from $\overline{RAS}$	t_{RAC}		70		80	ns	9, 10
Access Time from $\overline{CAS}$	t_{CAC}		20		20	ns	9, 10
Access Time from Column Address	t_{AA}		35		40	ns	9, 10
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45	ns	10
$\overline{CAS}$ to Output Data Setup Time	t_{CLZ}	0		0		ns	10
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	t_{OFF}	0	15	0	20	ns	11
Transition Time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10 000	80	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	70	125 000	80	125 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		20		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70		80		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10 000	20	10 000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	ns	9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		ns	12
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		ns	
Row Address Setup Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		ns	
Column Address Setup Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		ns	14
Write Command Pulse Width	t_{WP}	15		15		ns	14
Write Command Lead Time Referenced to $\overline{RAS}$	t_{RWL}	20		25		ns	
Write Command Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		20		ns	
Data-in Setup Time	t_{DS}	0		0		ns	15
Data-in Hold Time	t_{DH}	15		20		ns	15

(2/2)

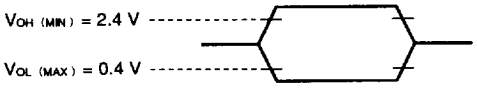
PARAMETER		SYMBOL	tRAC = 70 ns		tRAC = 80 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Refresh Time	μPD42S4280	tREF		128		128	ms	17
	μPD424280			8		8	ms	
Write Command Setup Time		tWCS	0		0		ns	16
$\overline{CAS}$ to $\overline{WE}$ Delay Time		tCWD	40		45		ns	16
$\overline{RAS}$ to $\overline{WE}$ Delay Time		tRWD	90		105		ns	16
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)		tCPWD	60		70		ns	16
Column Address Delay Time Referenced to $\overline{WE}$		tAWD	55		65		ns	16
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		tCSR	10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		tCHR	15		15		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time		tRPC	10		10		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time		tOES	0		0		ns	
Access Time from $\overline{OE}$		tOEA		20		20	ns	
$\overline{OE}$ Data Delay Time		tOED	15		20		ns	
Output Buffer Turn-off Delay Time ($\overline{OE}$)		tOEZ	0	15	0	20	ns	11
$\overline{OE}$ Output Data Setup Time		tOLZ	0		0		ns	
$\overline{OE}$ Hold Time		tOEH	0		0		ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$ Precharge		tRHCP	40		45		ns	
Masked Byte Write Hold Time referenced to $\overline{RAS}$		tMRH	0		0		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tRASS	100		100		μs	17
$\overline{CAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tCASS	500		500		μs	17
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tRPS	130		150		ns	17
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tCHS	−50		−50		ns	17

NOTES ★

1. $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
2. All voltages are referenced to GND.
3. An initial pause of 100 μs is required after power up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
4. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on t_{RC} and t_{PC}. Specified values are obtained with outputs open.
5. Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
6. AC measurements assume t_T = 5 ns.
7. AC Characteristics test condition
   (1) Input timing specification



   (2) Output timing specification

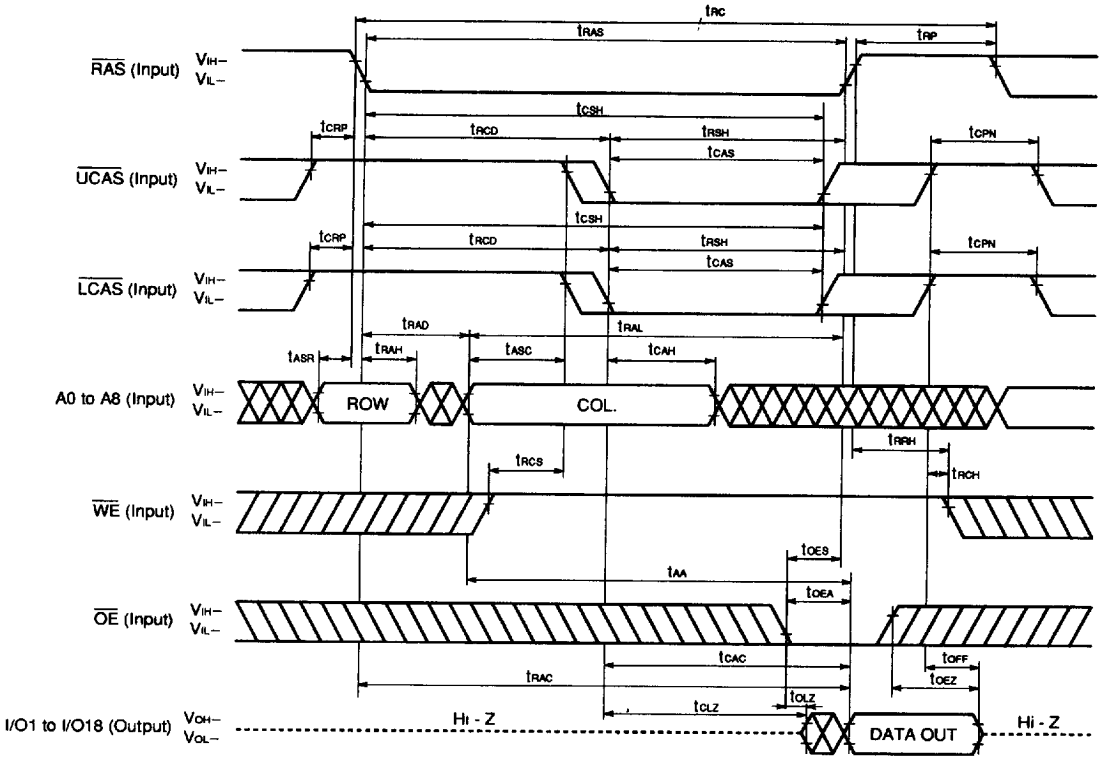


8. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70 °C) is assured.
9. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

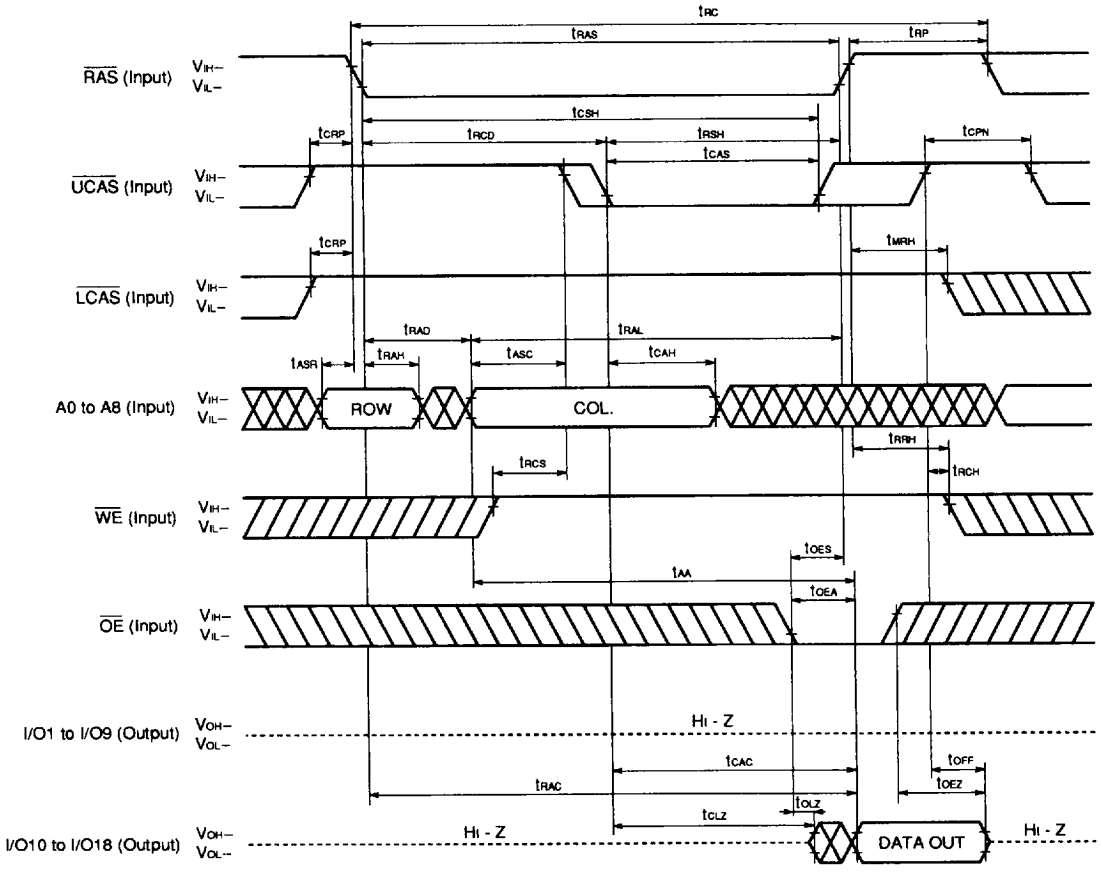
CONDITION	ACCESS TIME
$t_{RAD} \leq t_{RAD\ (MAX)}$ and $t_{RCD} \leq t_{RCD\ (MAX)}$	$t_{RAC\ (MAX)}$
$t_{RAD\ (MAX.)} \leq t_{RAD}$ and $t_{RCD} \leq t_{RCD\ (MAX)}$	$t_{AA\ (MAX.)}$
$t_{RCD\ (MAX.)} \leq t_{RCD}$	$t_{CAC\ (MAX.)}$

   $t_{RAD\ (MAX)}$ and $t_{RCD\ (MAX)}$ indicate the point which the access time changes and are not the limits of operation.
10. Loading conditions are 1TTL and 100 pF.
11. $t_{OFF\ (MAX)}$ and $t_{OEZ\ (MAX)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
12. $t_{CRP\ (MIN)}$ requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycles.
13. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN)}$ must be satisfied for a read cycle.
14. $t_{WP\ (MIN.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH\ (MIN.)}$ should be satisfied.
15. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS\ (MIN.)} \leq t_{WCS}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle. If $t_{RWD\ (MIN.)} \leq t_{RWD}$, $t_{CWD\ (MIN.)} \leq t_{CWD}$, $t_{AWD\ (MIN.)} \leq t_{AWD}$, $t_{CPWD\ (MIN.)} \leq t_{CPWD}$, the cycle is a read modify write cycle and condition of the data out (at access time) is indeterminate.
17. This specification is applicable only for μPD42S4280.

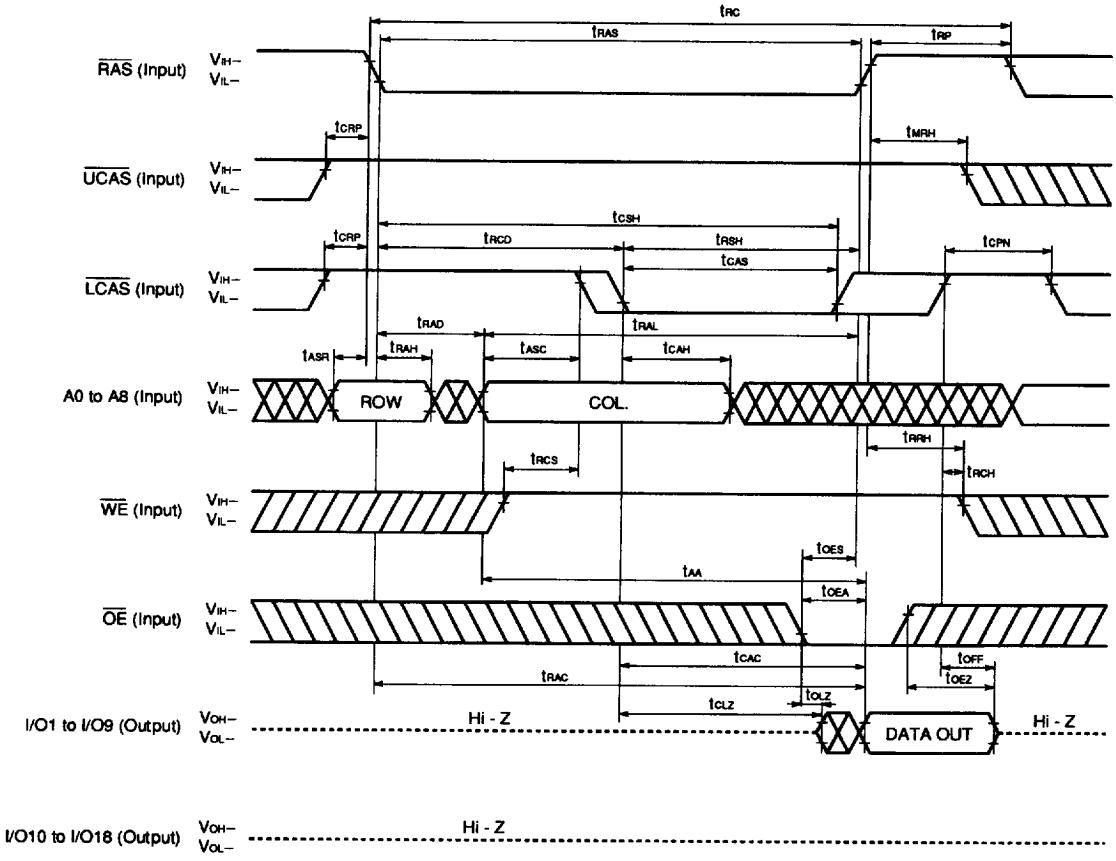
READ CYCLE



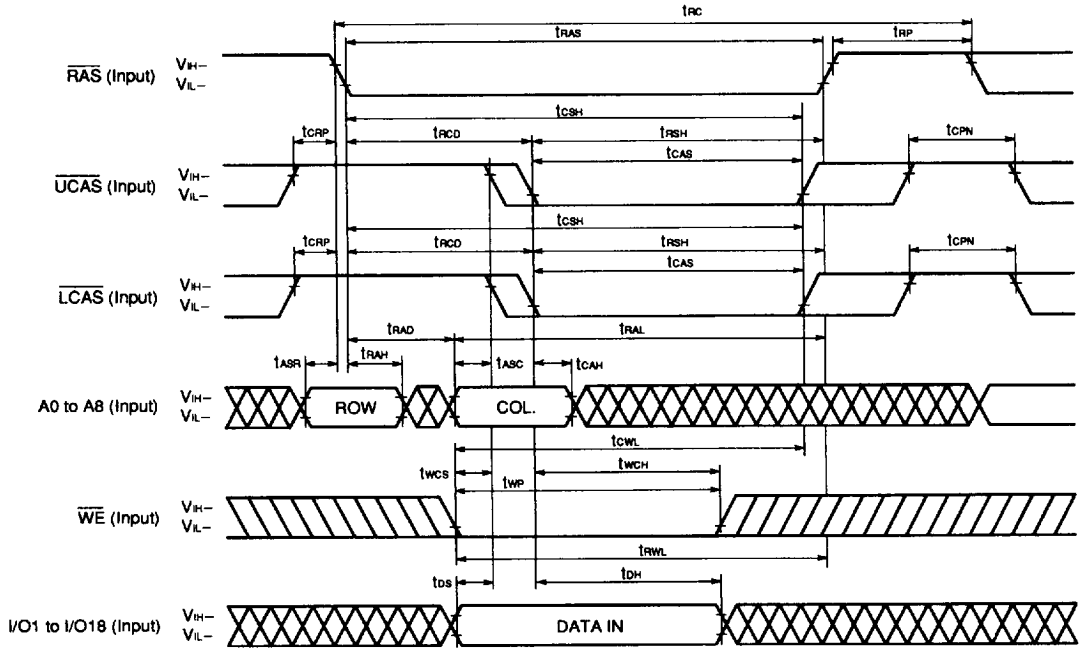
UPPER BYTE READ CYCLE



LOWER BYTE READ CYCLE

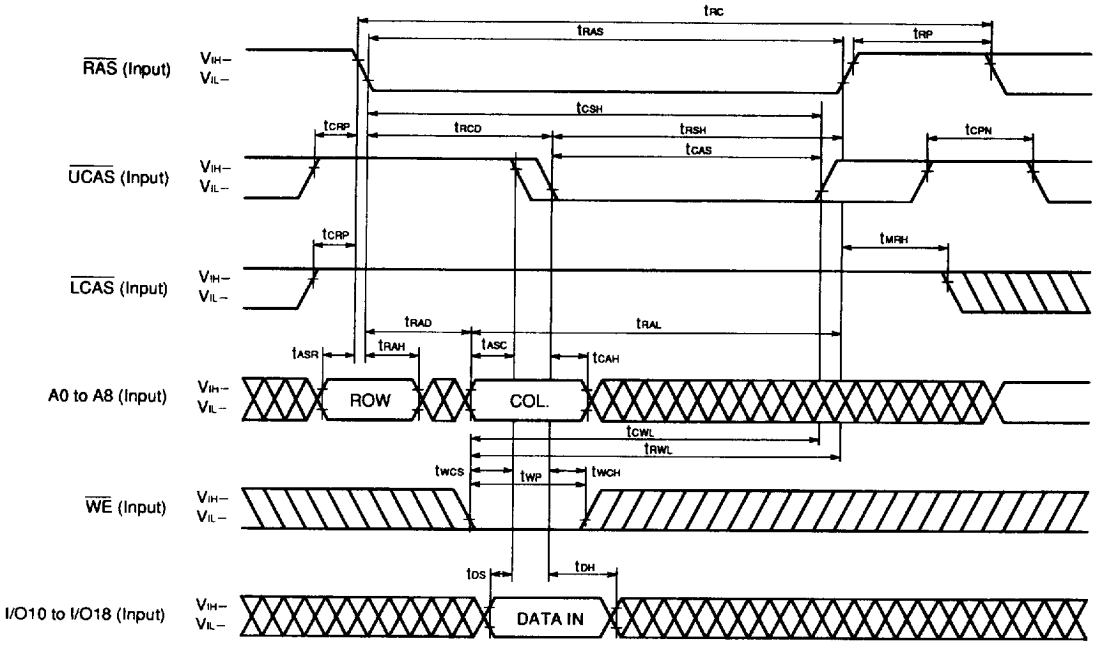


EARLY WRITE CYCLE



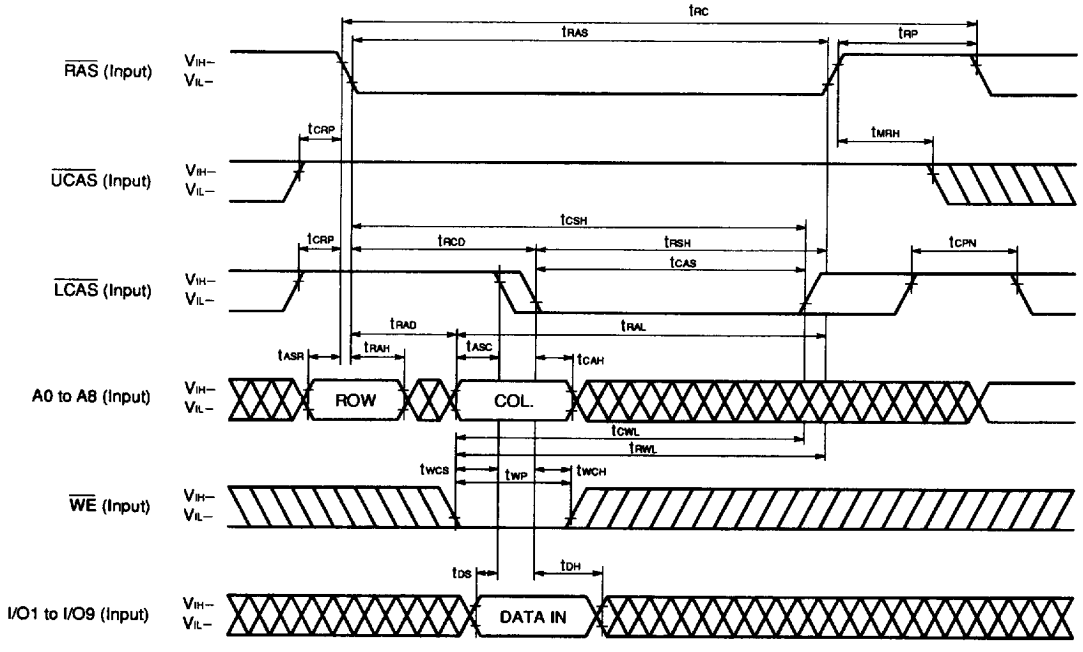
Remark $\overline{OE}$ = Don't care

UPPER BYTE EARLY WRITE CYCLE



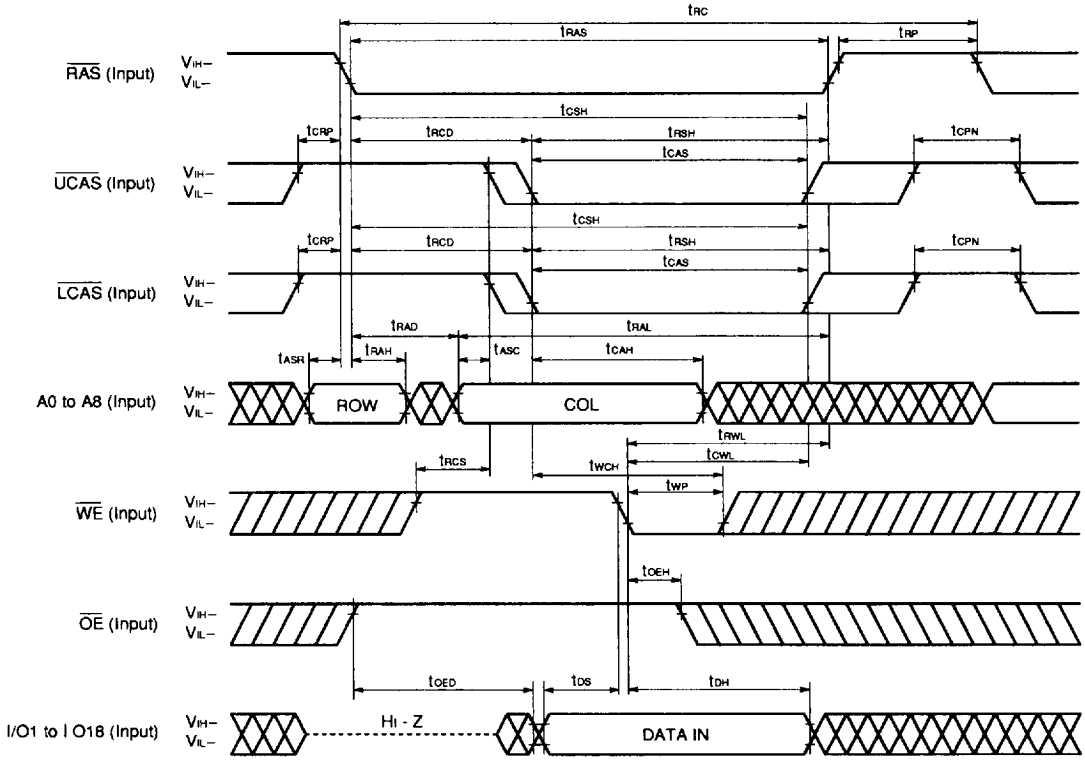
Remark $\overline{OE}$, I/O1 to I/O9 = Don't care

LOWER BYTE EARLY WRITE CYCLE

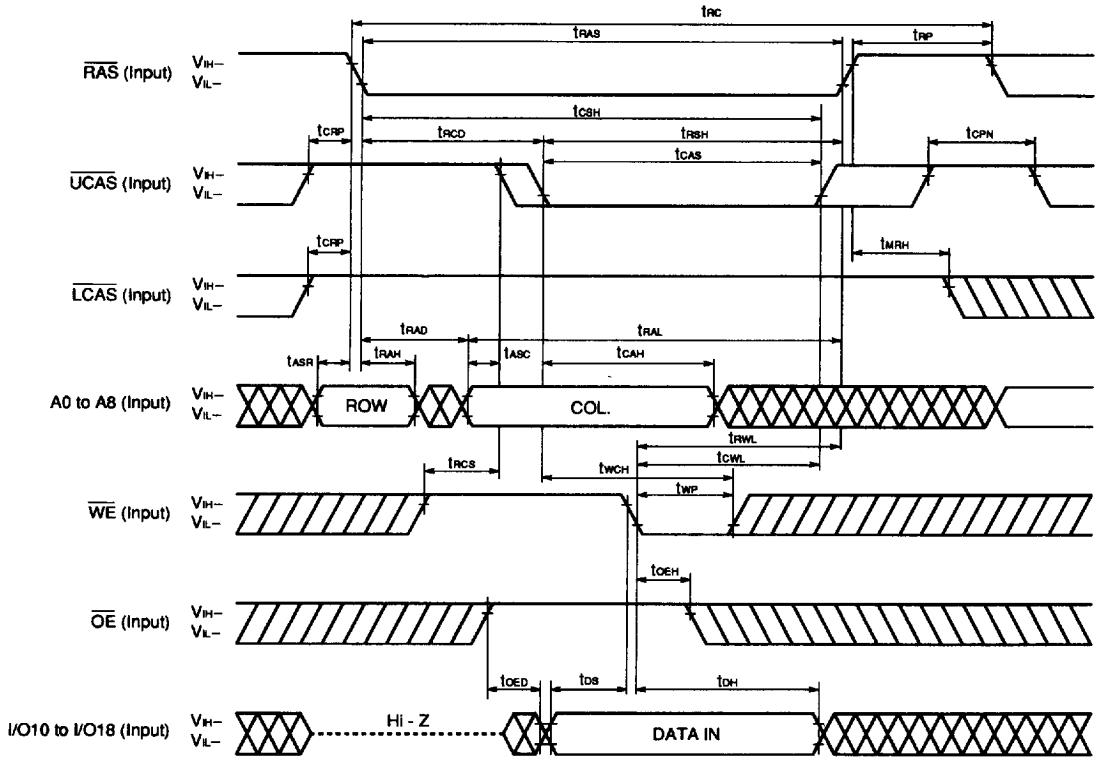


Remark $\overline{OE}$, I/O10 to I/O18 = Don't care

LATE WRITE CYCLE

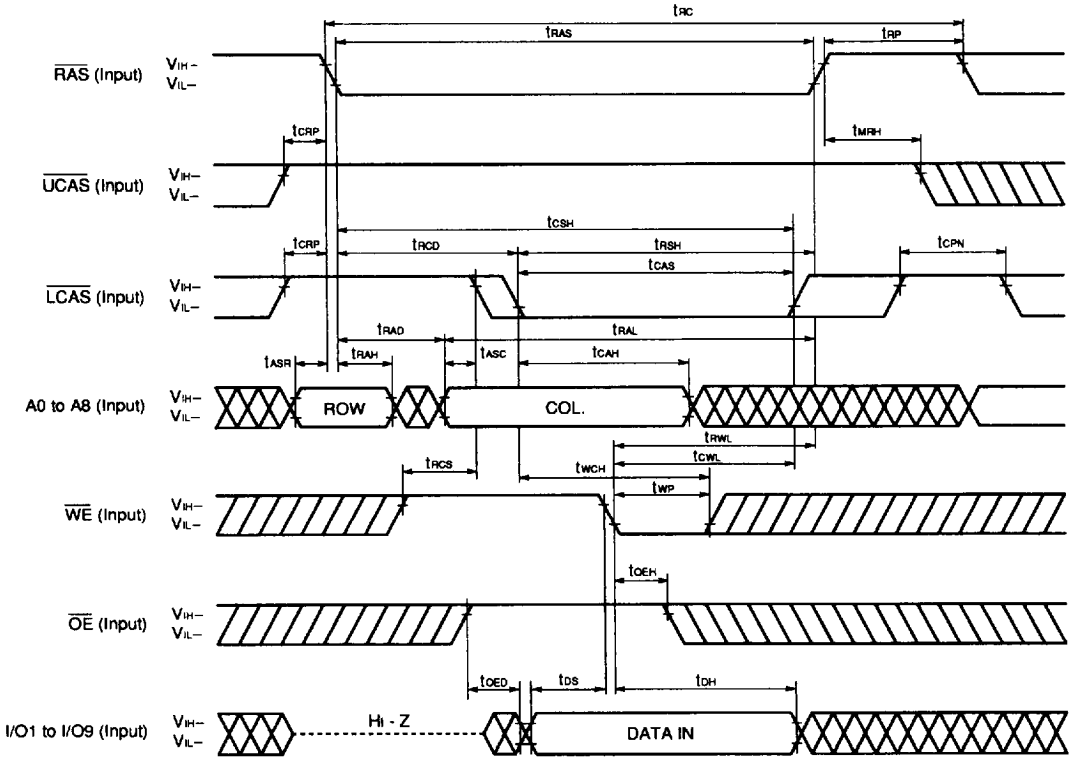


UPPER BYTE LATE WRITE CYCLE



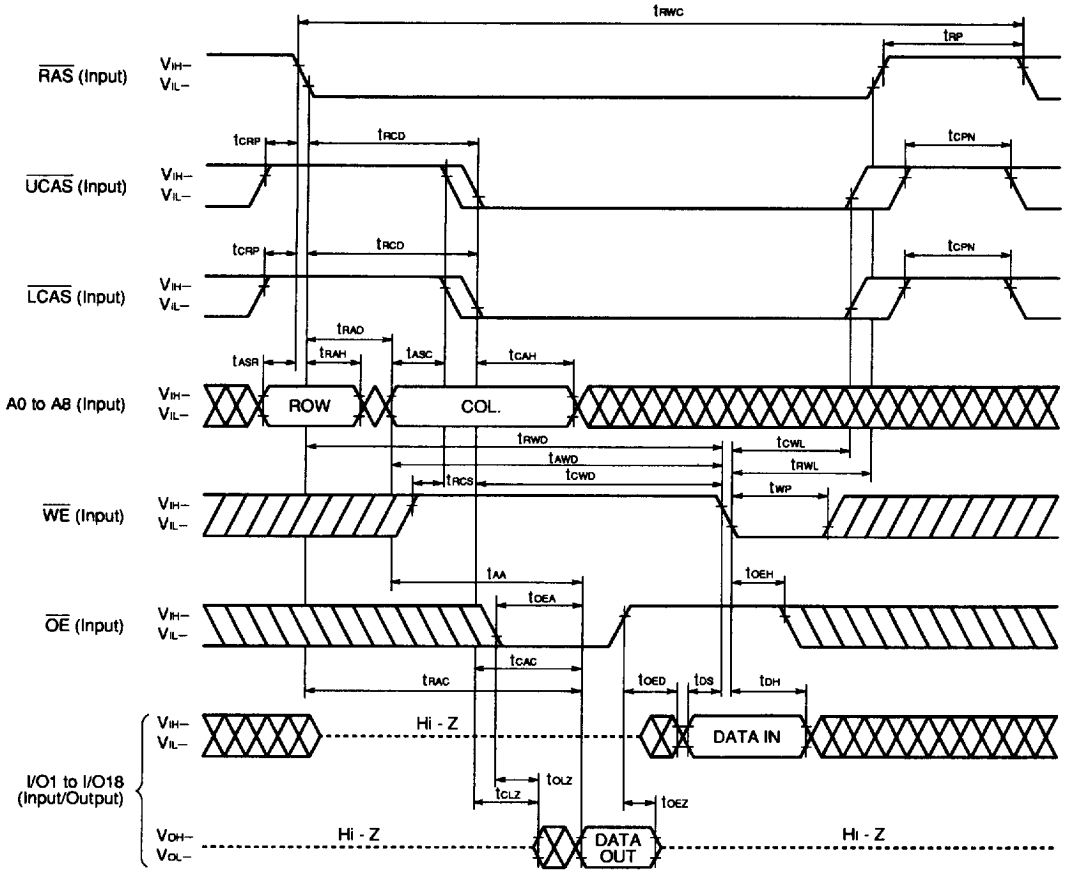
Remark I/O1 to I/O9 = Don't care

LOWER BYTE LATE WRITE CYCLE

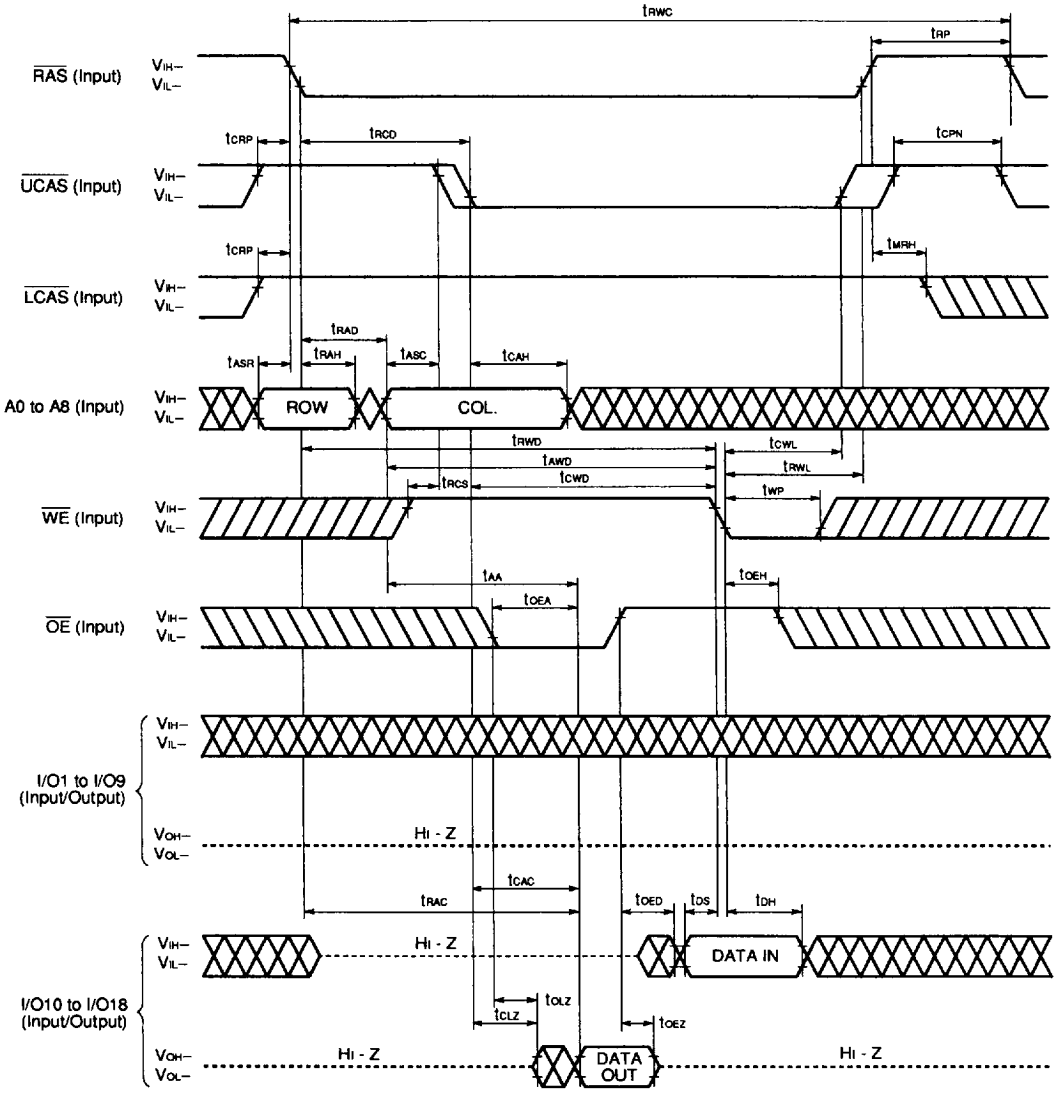


Remark I/O10 to I/O18 = Don't care

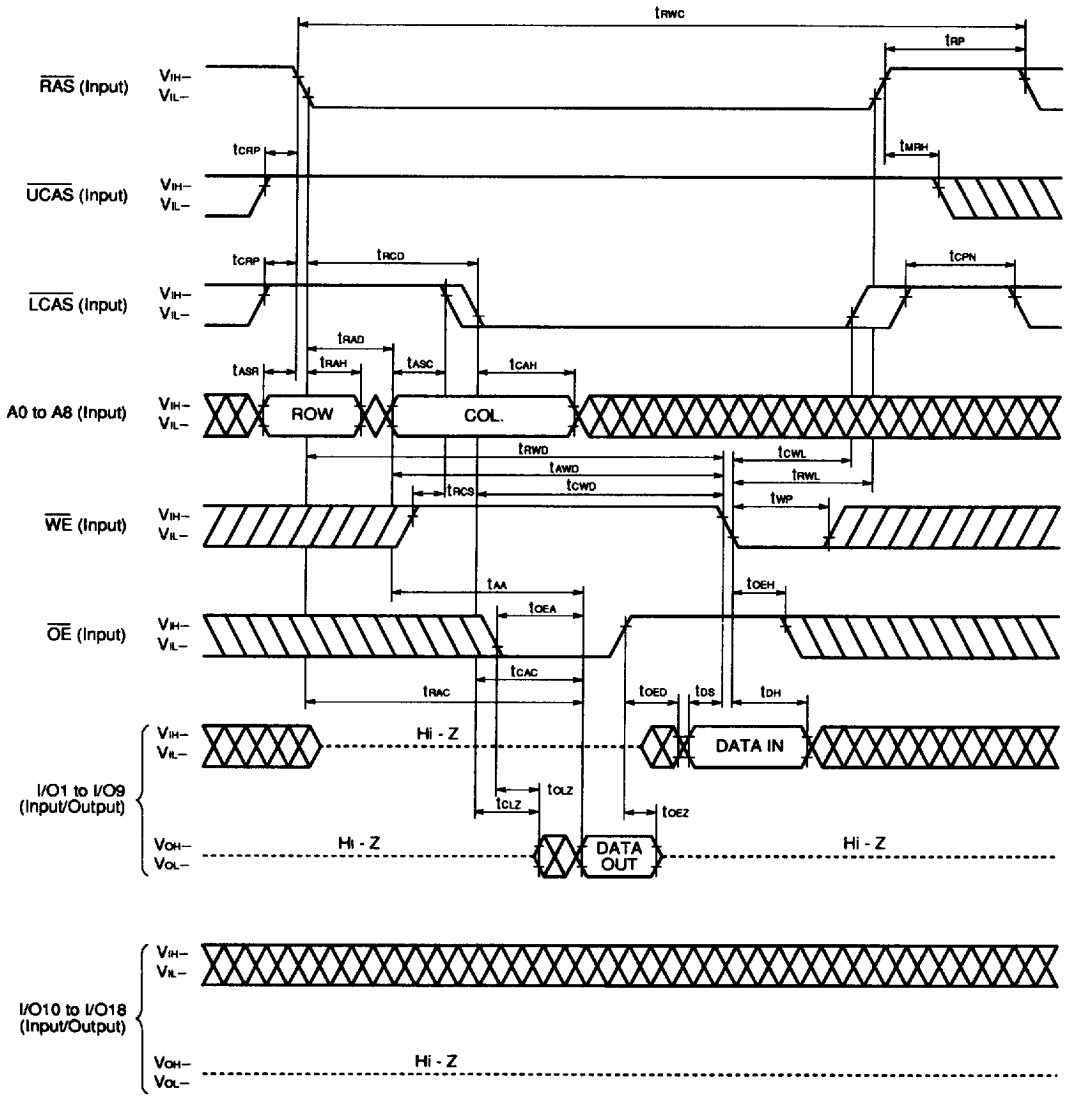
READ MODIFY WRITE CYCLE



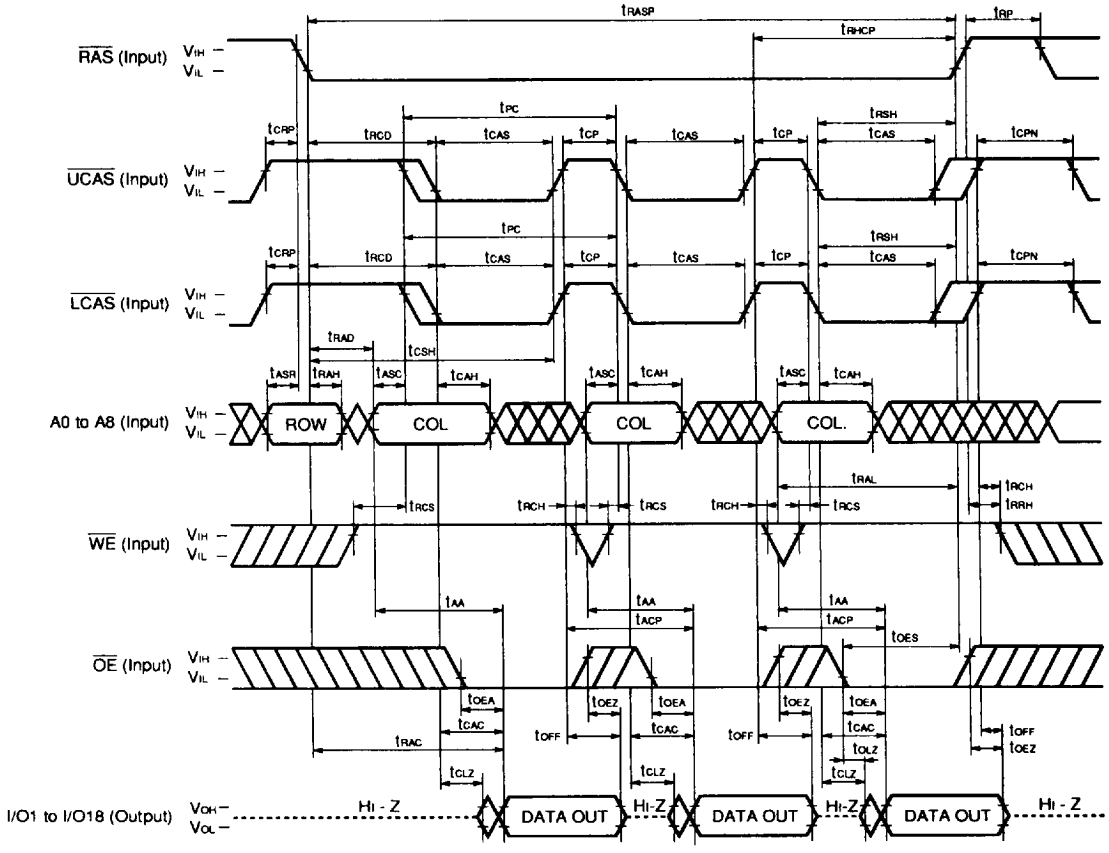
UPPER BYTE READ MODIFY WRITE CYCLE



LOWER BYTE READ MODIFY WRITE CYCLE

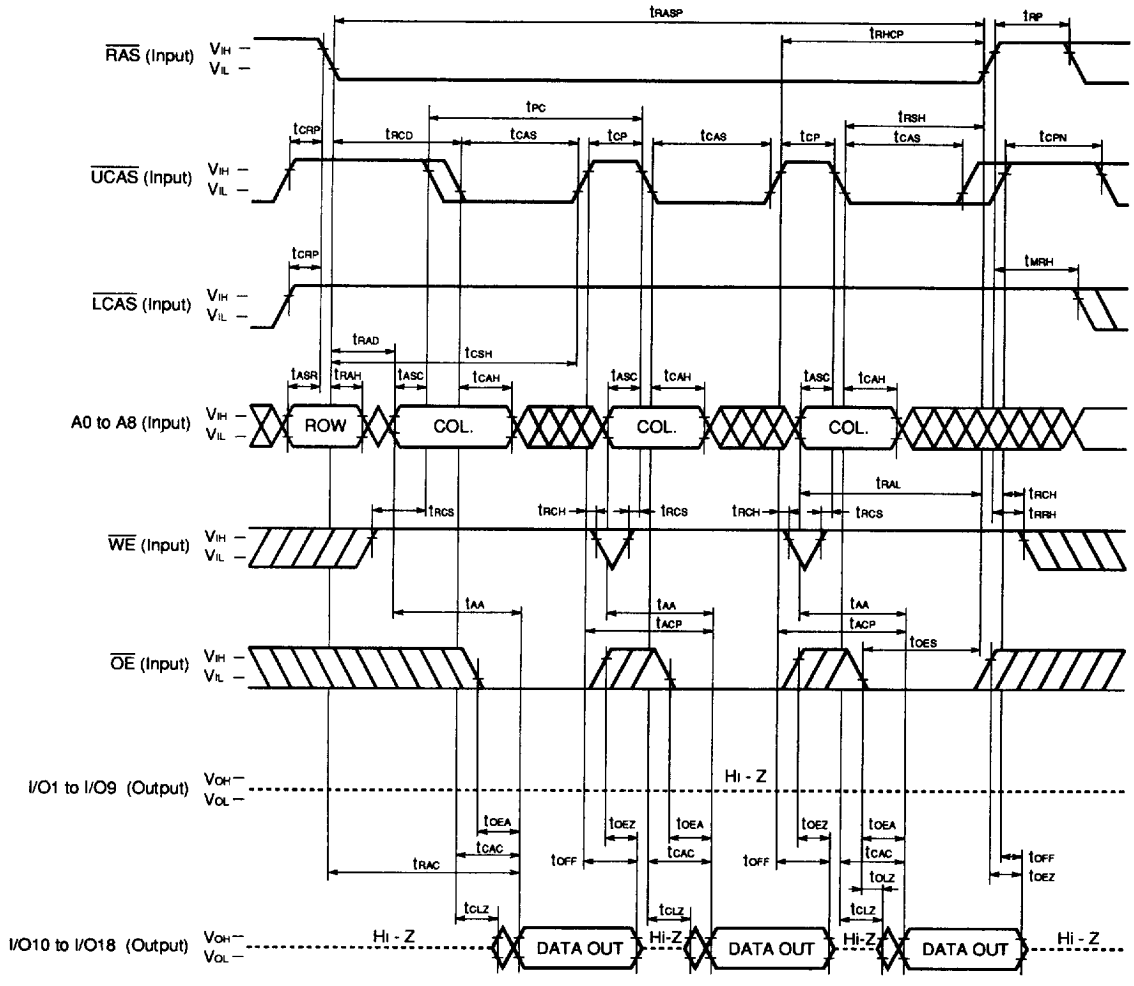


FAST PAGE MODE READ CYCLE



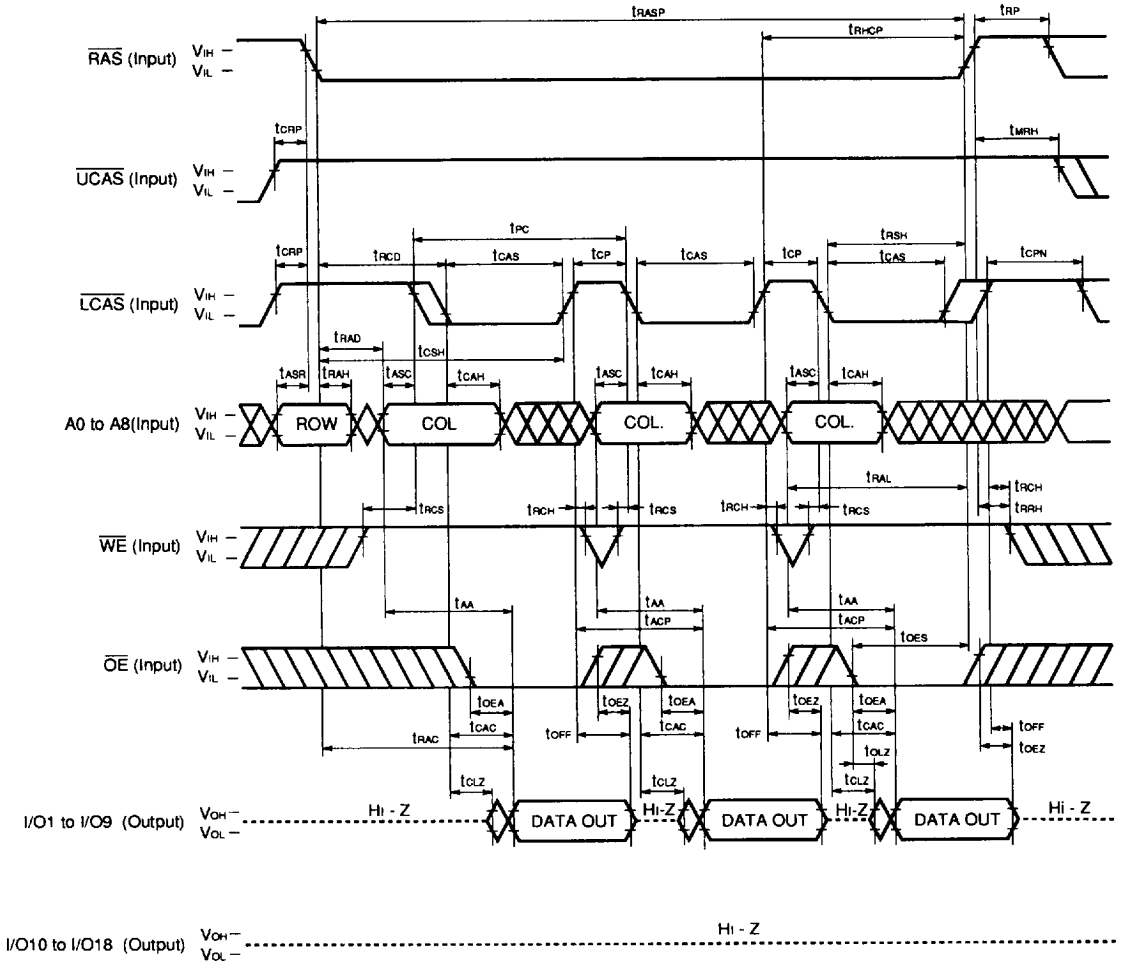
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE UPPER BYTE READ CYCLE



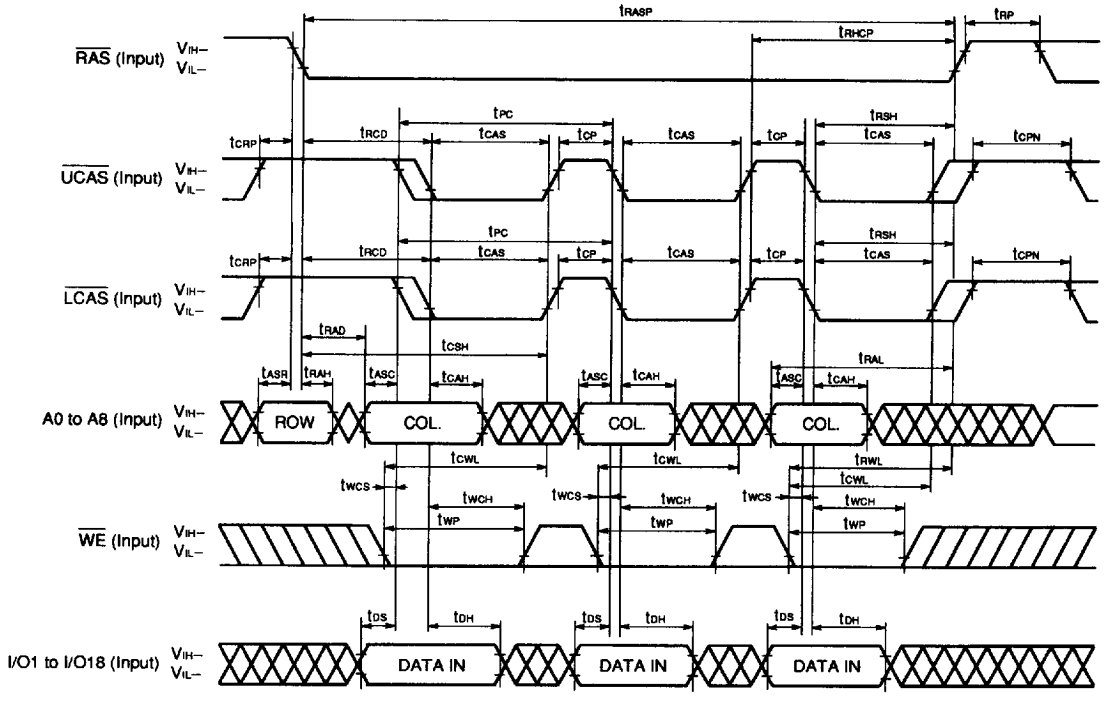
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LOWER BYTE READ CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

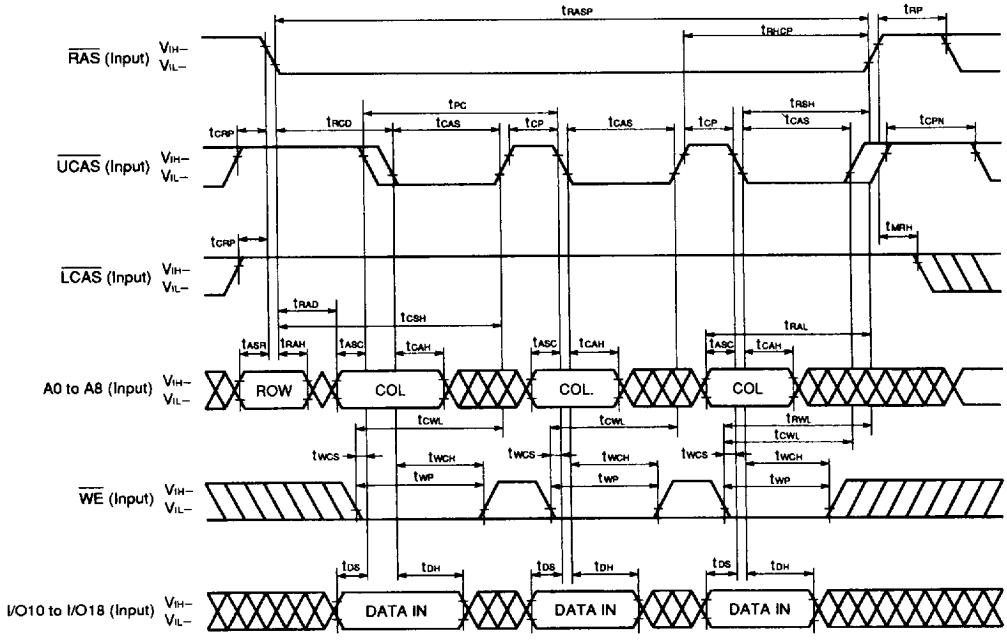
FAST PAGE MODE EARLY WRITE CYCLE



Remark $\overline{O'.}$ = Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

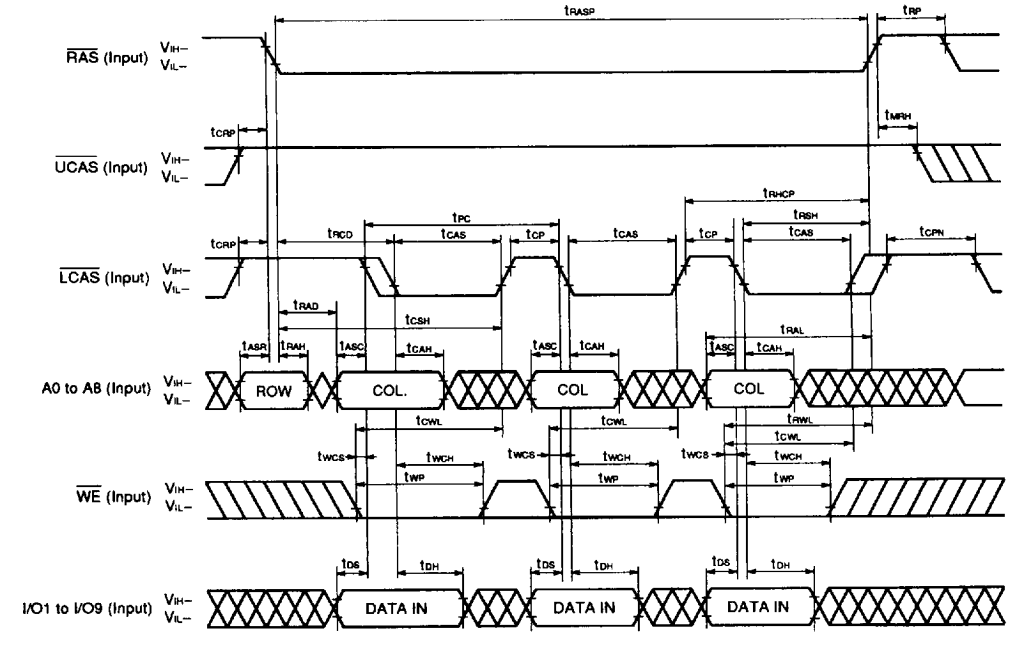
FAST PAGE MODE UPPER BYTE EARLY WRITE CYCLE



Remark I/O1 to I/O9, $\overline{OE}$ = Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

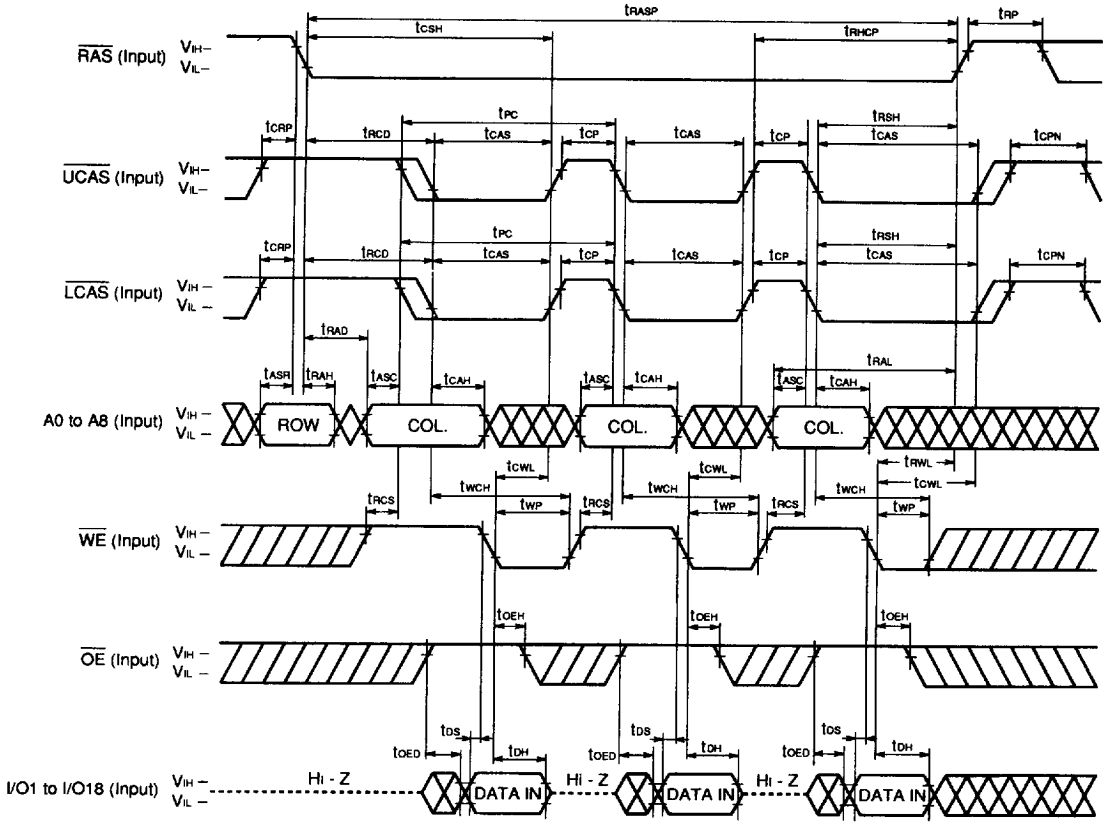
FAST PAGE MODE LOWER BYTE EARLY WRITE CYCLE



Remark I/O10 to I/O18, $\overline{OE}$ = Don't care

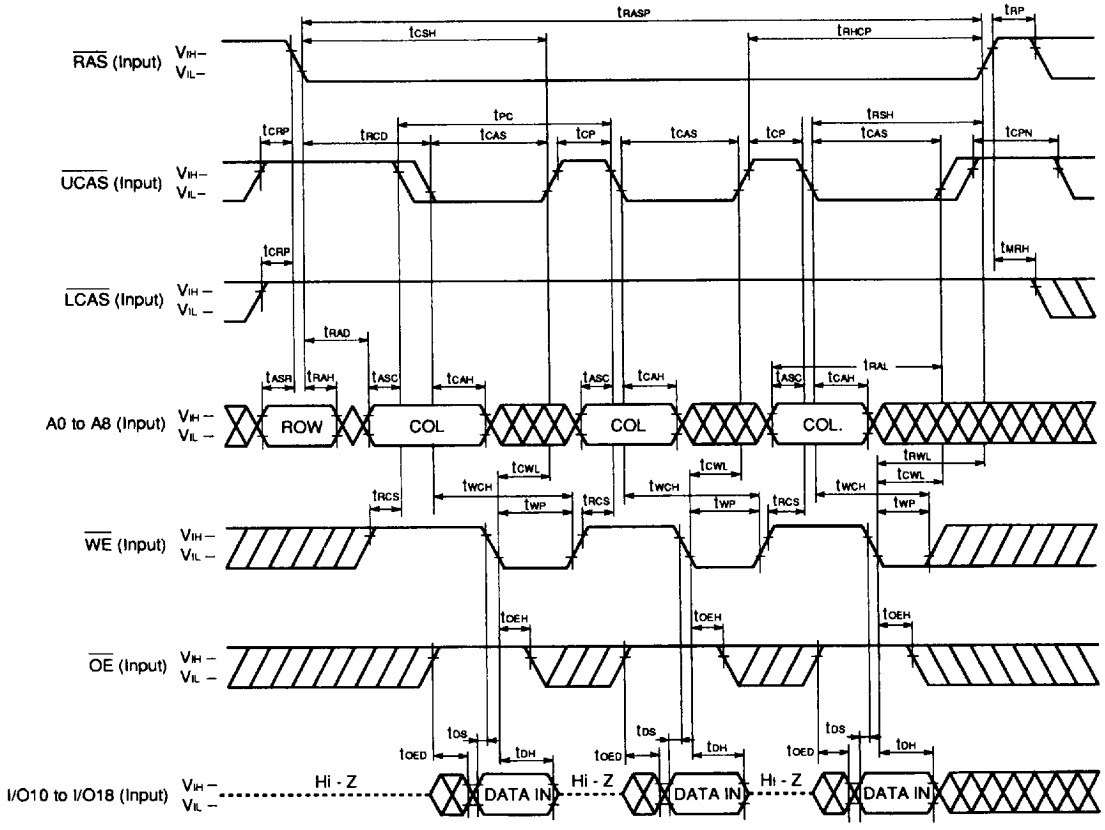
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LATE WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

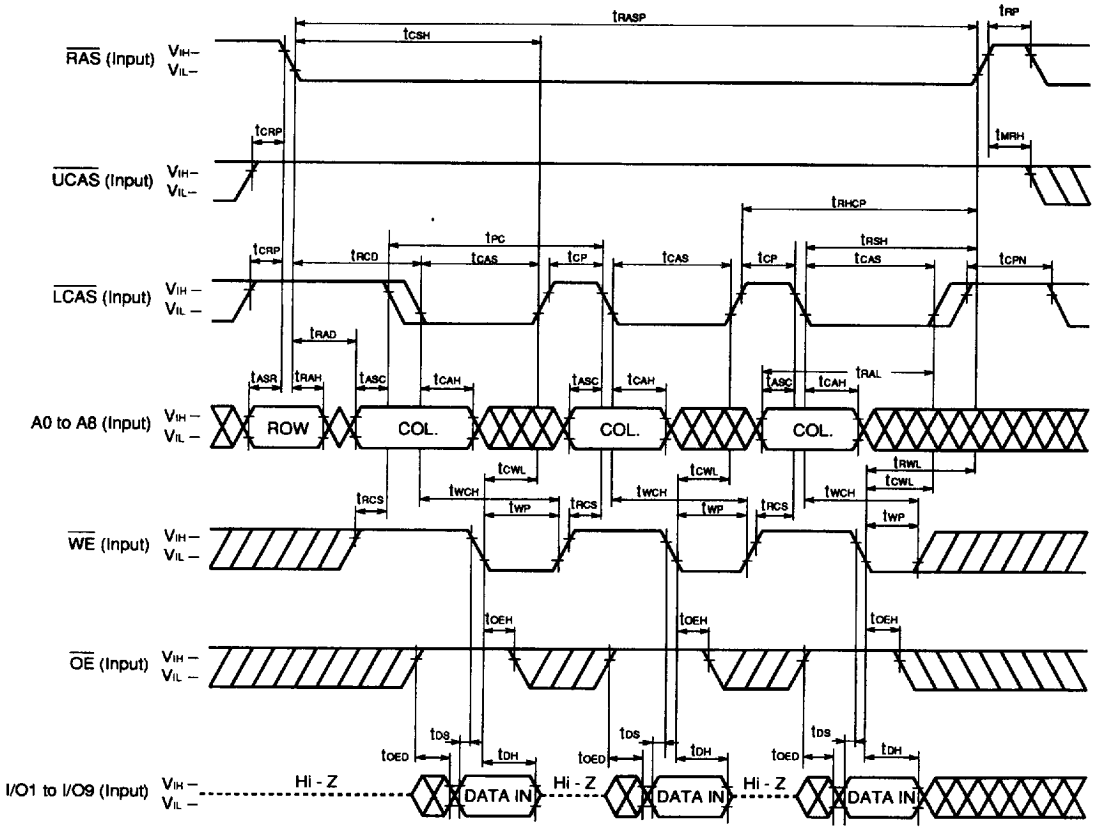
FAST PAGE MODE UPPER BYTE LATE WRITE CYCLE



Remark I/O1 to I/O9 = Don't care

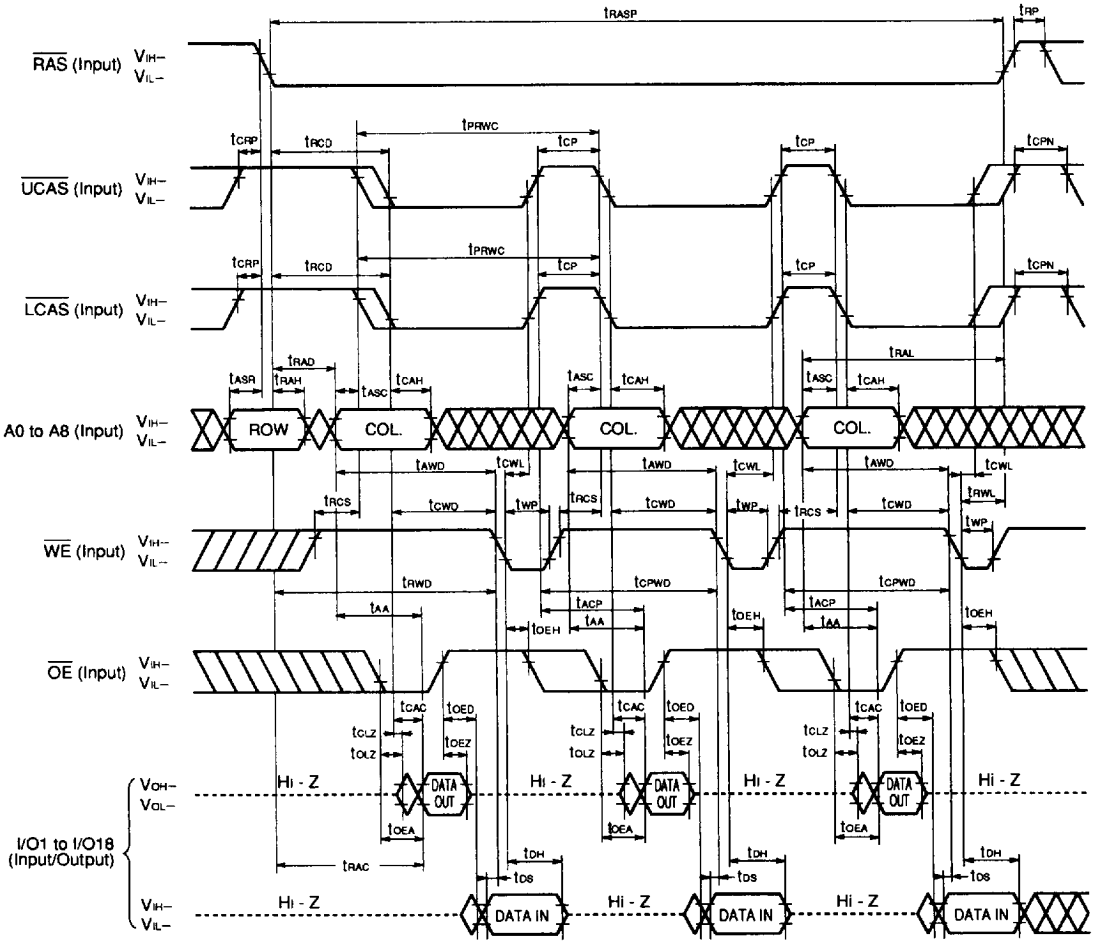
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LOWER BYTE LATE WRITE CYCLE



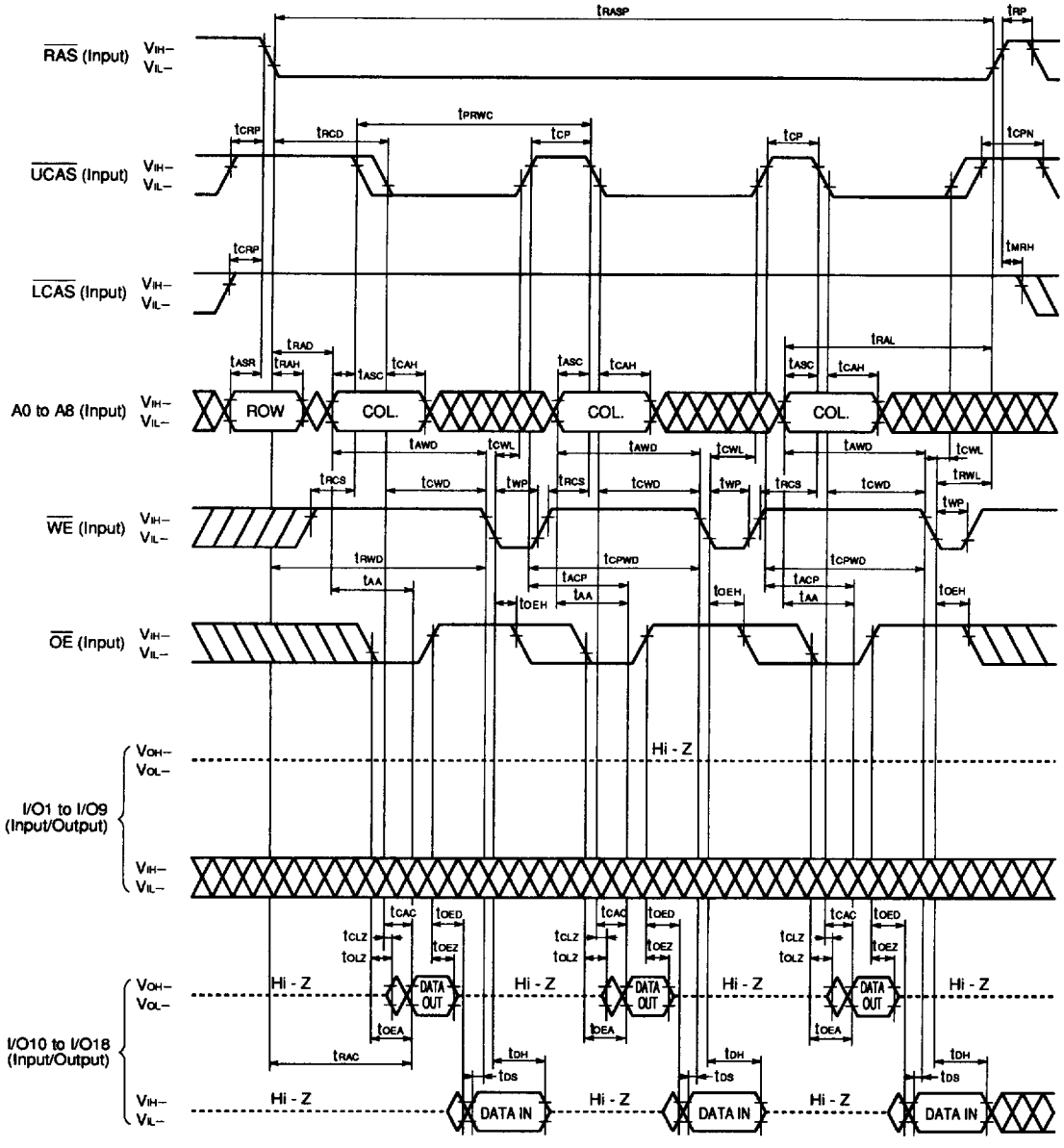
Remark I/O10 to I/O18 = Don't care
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE READ MODIFY WRITE CYCLE



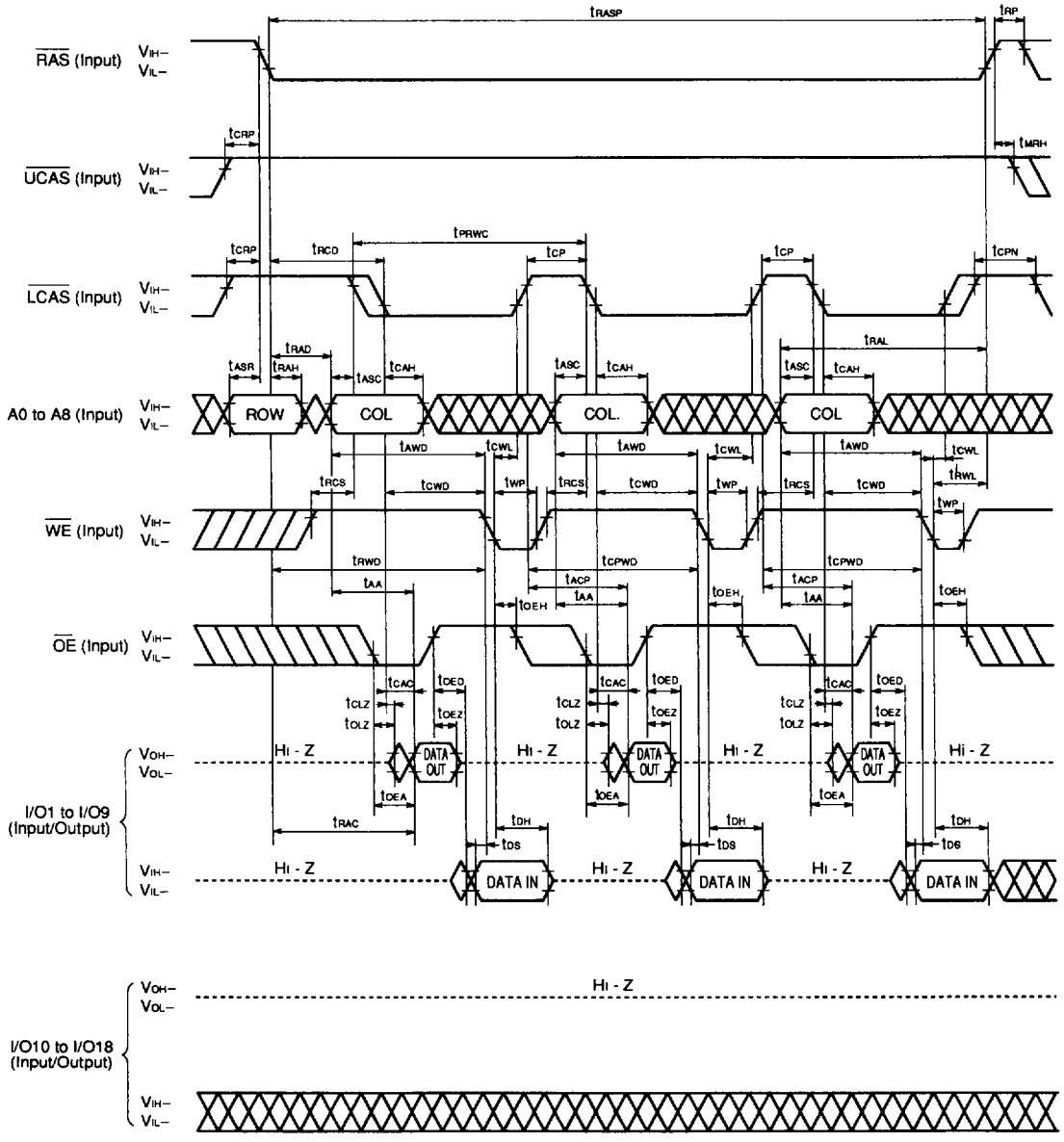
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE UPPER BYTE READ MODIFY WRITE CYCLE



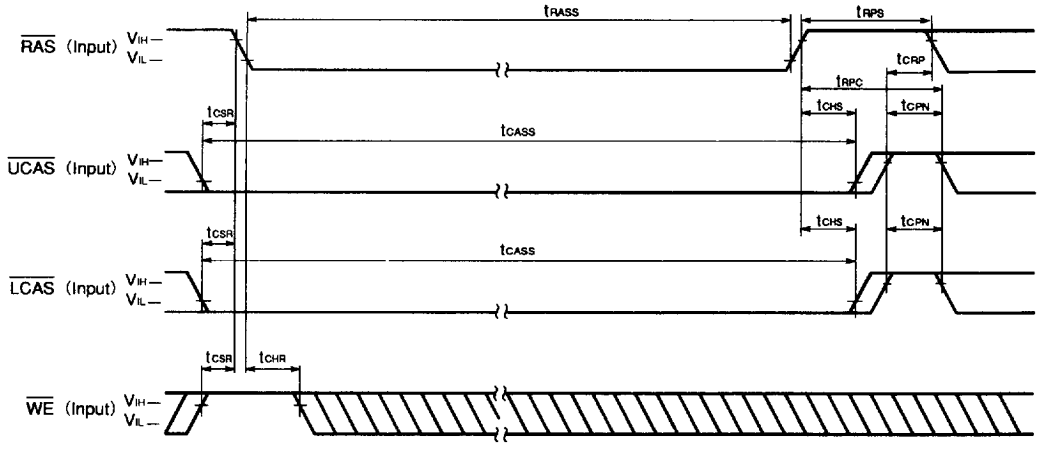
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LOWER BYTE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

★ $\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE (Only for μPD42S4280)



Remark Address, $\overline{OE}$ = Don't care I/O1 to I/O18 = Hi - Z

How to use $\overline{CAS}$ before $\overline{RAS}$ self refresh mode.

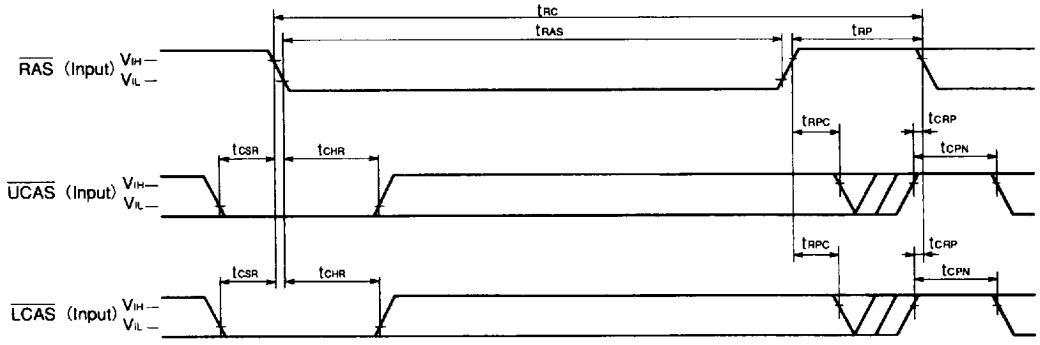
$\overline{CAS}$ before $\overline{RAS}$ self refresh mode can't be used by itself. It must be used with performing one of 3 refreshes below.

- **When using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh**
  Refresh 512 times during 128 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

- **When using burst $\overline{CAS}$ before $\overline{RAS}$ refresh**
  Refresh 512 times during 8 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

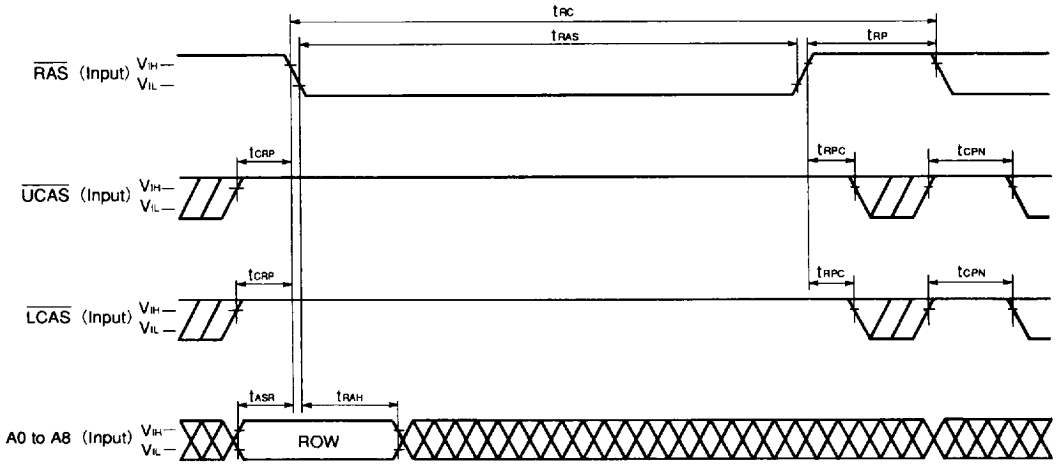
- **When using $\overline{RAS}$ only refresh**
  Refresh all refresh addresses during 8 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

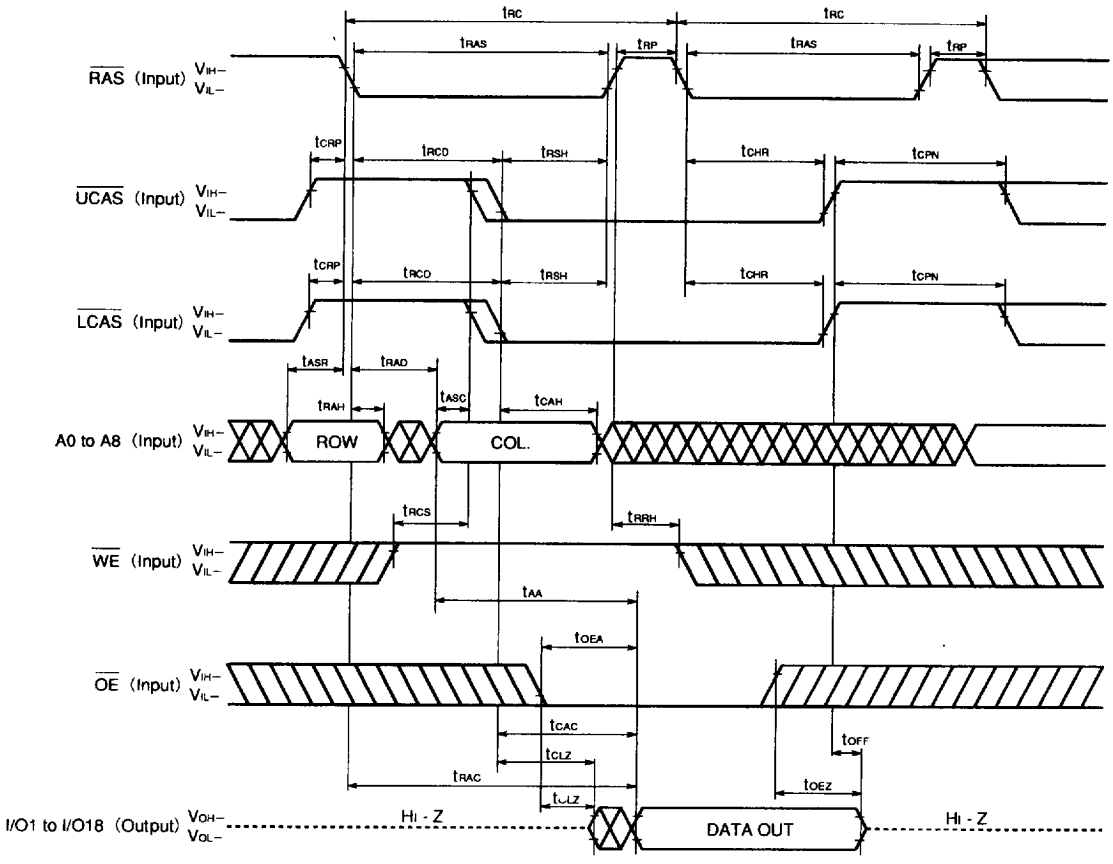


Remark A0 to A8, $\overline{WE}$, $\overline{OE}$ = Don't care I/O1 to I/O18 = Hi - Z

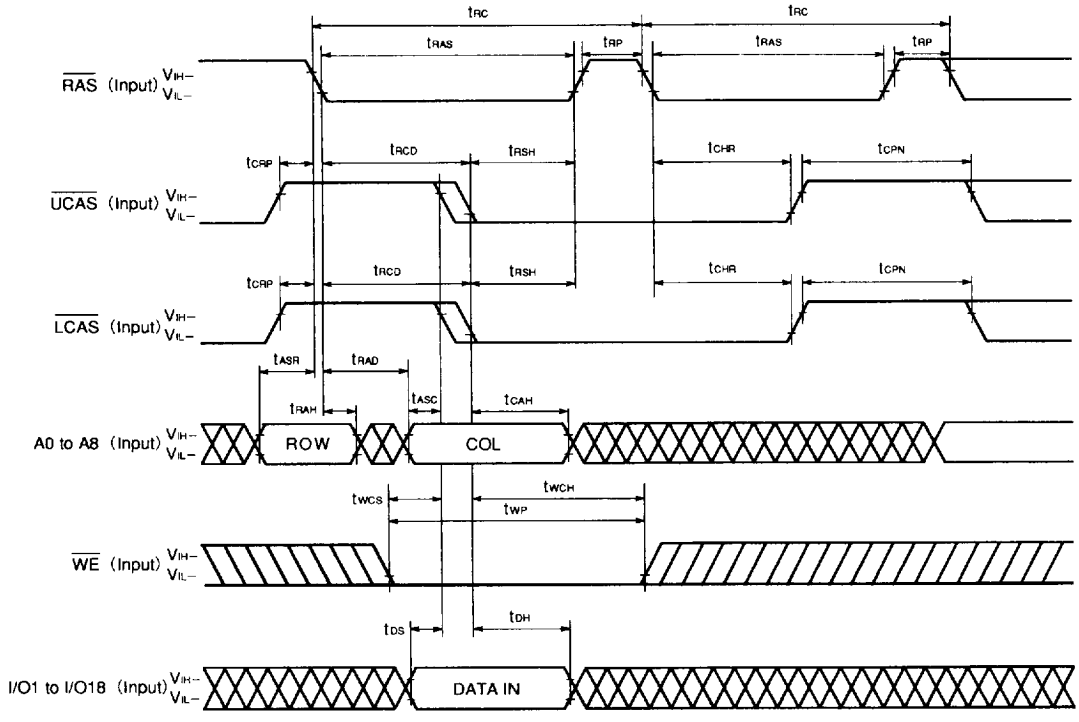
$\overline{RAS}$ ONLY REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

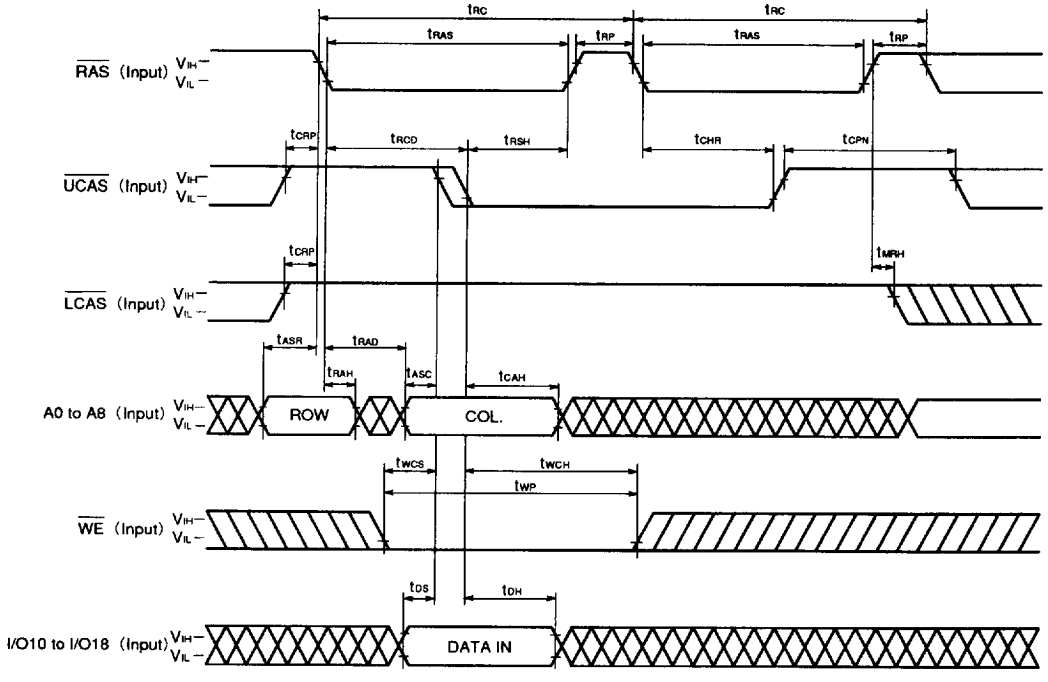


HIDDEN REFRESH CYCLE (WRITE)



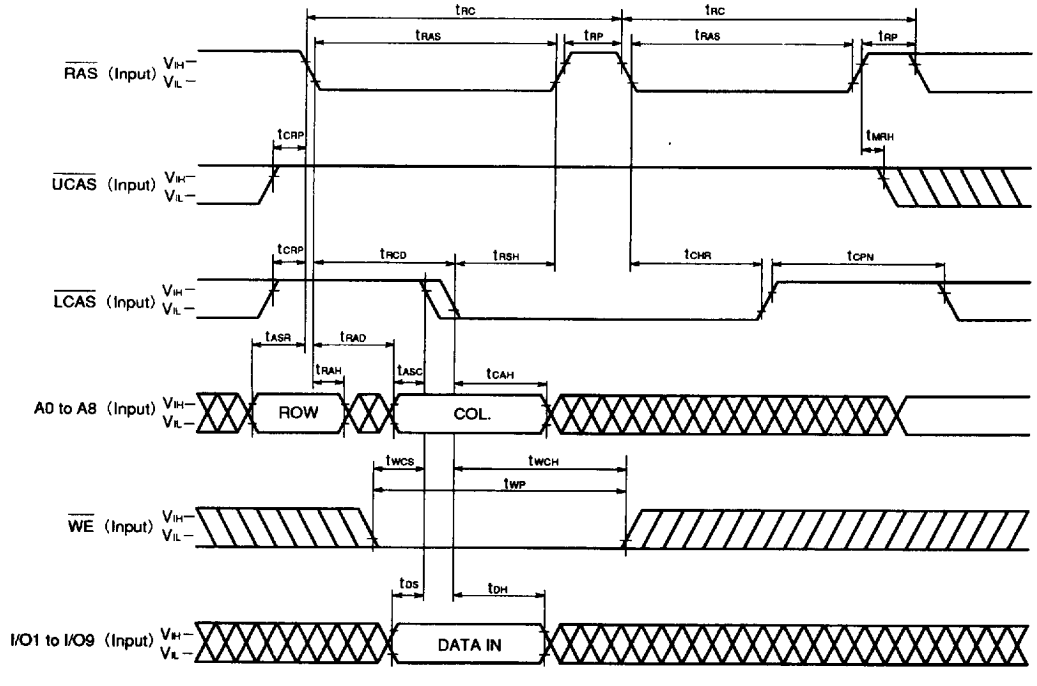
Remark $\overline{OE}$ = Don't care

HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Remark $\overline{OE}$, I/O1 to I/O9 = Don't care

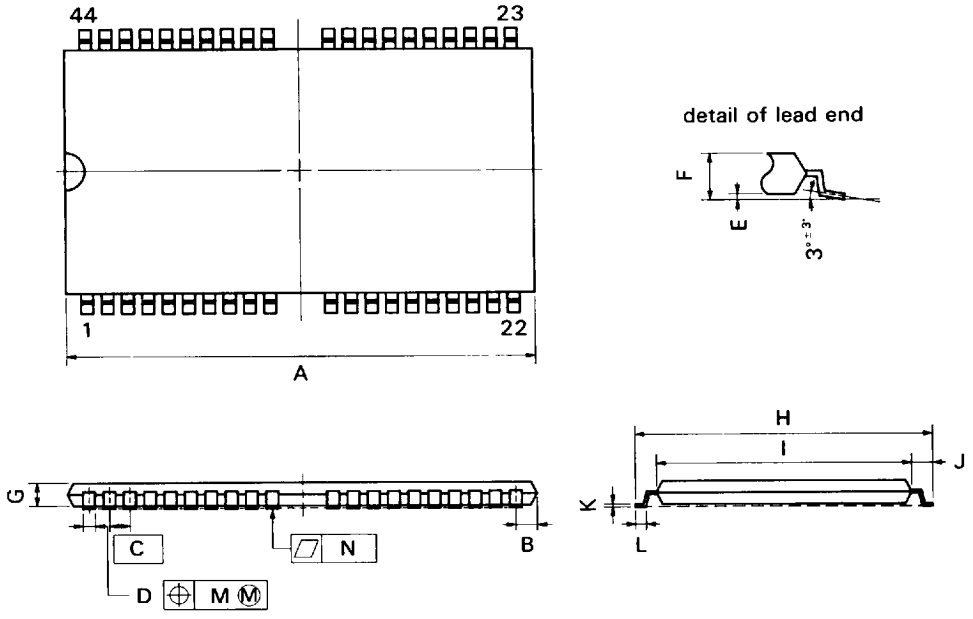
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



Remark $\overline{OE}$, I/O10 to I/O18 = Don't care

PACKAGE INFORMATIONS

44 PIN PLASTIC TSOP (400mil)



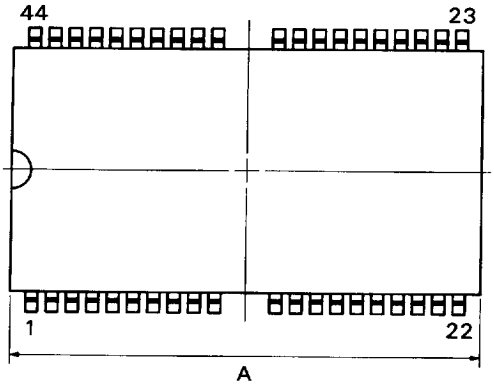
S44G5 80 7JF

NOTE

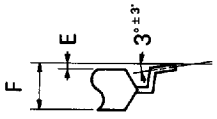
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition

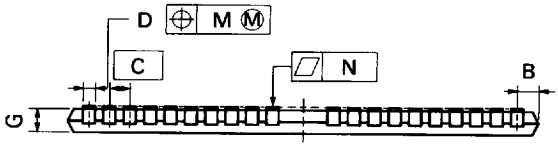
ITEM	MILLIMETERS	INCHES
A	18 81 MAX	0 741 MAX
B	1 0 MAX	0 040 MAX.
C	0 8 (T.P)	0 031 (T.P)
D	$0.30^{+0\ 10}$	$0\ 012^{+0\ 004}_{0\ 005}$
E	$0\ 05^{+0\ 05}$	$0\ 002^{+0\ 002}$
F	1 1 MAX	0 044 MAX
G	0 97	0 038
H	$11\ 76^{\pm 0\ 2}$	$0.463^{+0\ 008}$
I	$10\ 16^{+0\ 1}$	$0\ 400^{\pm 0\ 004}$
J	$0\ 8^{\pm 0\ 2}$	$0\ 031^{+0\ 009}_{0\ 008}$
K	$0\ 125^{+0\ 10}_{0\ 05}$	$0\ 005^{+0\ 004}_{0\ 002}$
L	$0\ 5^{+0\ 1}$	$0\ 020^{+0\ 004}_{0\ 005}$
M	0 13	0 005
N	0 10	0.004

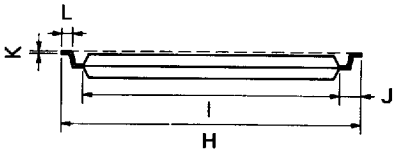
44 PIN PLASTIC TSOP (400mil)



detail of lead end







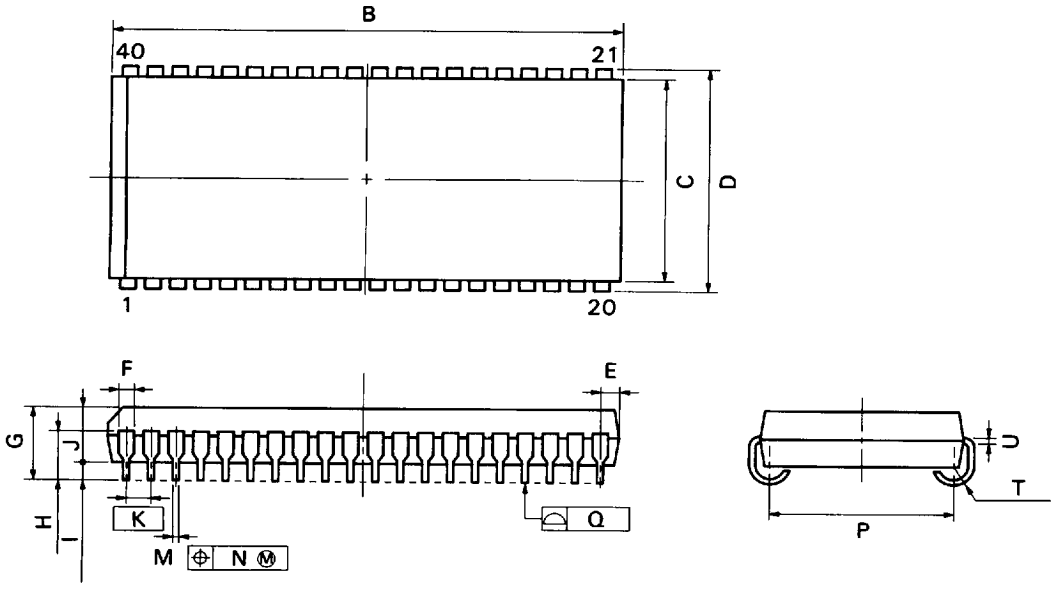
S44G5-80-7KF

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
E	$0.05^{\pm 0.05}$	$0.002^{\pm 0.002}$
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	$11.76^{\pm 0.2}$	$0.463^{\pm 0.008}$
I	$10.16^{\pm 0.1}$	$0.400^{\pm 0.004}$
J	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004

40PIN PLASTIC SOJ (400 mil)



P40LE-400A-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$26.29^{+0.2}_{-0.35}$	$1.035^{+0.008}_{-0.014}$
C	10.16	0.400
D	$11.18^{\pm 0.2}$	$0.440^{\pm 0.008}$
E	$1.08^{\pm 0.15}$	$0.043^{+0.006}_{-0.007}$
F	0.7	0.028
G	$3.5^{\pm 0.2}$	$0.138^{\pm 0.008}$
H	$2.4^{\pm 0.2}$	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	$9.4^{\pm 0.20}$	$0.370^{\pm 0.008}$
Q	0.15	0.006
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices when soldering μPD42S4280, 424280.

TYPES OF SURFACE MOUNT DEVICE

μPD42S4280G5, 424280G5 (44-pin Plastic TSOP)
μPD42S4280LE, 424280LE (40-pin Plastic SOJ)