# NEC

NEC Electronics Inc.

**μPD481440**
**262,144 x 16-Bit**
**Graphics Memory**

## Description

The μPD481440 is a fast-page memory with optional extended data output, organized as 262,144 words by 16 bits and designed to operate from a single +5-volt power supply. This graphics memory also incorporates powerful functions useful in video sytems, including write-per-bit, flash write, and block write. Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$. After a valid read, data is latched on the rising edge of $\overline{CAS}$ and remains valid until the next falling edge of $\overline{CAS}$. Data out will transition to the high-impedance state when both $\overline{RAS}$ and $\overline{CAS}$ or $\overline{OE}$ are inactive.

Word writing ($I/O_1$ - $I/O_{16}$), upper byte writing ($I/O_9$ - $I/O_{16}$), and lower byte writing ($I/O_1$ - $I/O_8$) are all possible using $\overline{UWE}$ and $\overline{LWE}$. If either $\overline{UWE}$ or $\overline{LWE}$ goes low during an early write cycle, all data outputs remain in high impedance. $\overline{UWE}$ or $\overline{LWE}$ going low causes a byte write cycle, while bringing both $\overline{UWE}$ and $\overline{LWE}$ low at the same time will result in a word write cycle. $\overline{UWE}$ and $\overline{LWE}$ cannot be staggered within the same write cycle.

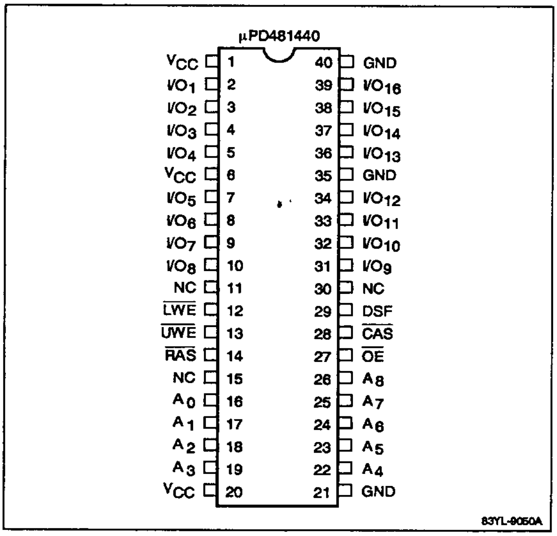
Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of $A_0$ - $A_8$ during an 8-ms refresh period.

## Features

- 262,144 by 16-bit organization
- Single +5-volt power supply
- Fast-page option with extended data output
- Byte write control with $\overline{UWE}$ and $\overline{LWE}$
- Persistent and nonpersistent write-per-bit option, which provides I/O masking for 16 I/O's
- Block write option with write-per-bit control and column mask function
- Flash write option with byte masking control
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- TTL-compatible inputs and outputs
- Low input capacitance
- 512 refresh cycles every 8 ms
- 40-pin plastic SOJ package

## Pin Configurations

***40-Pin Plastic SOJ***

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## Pin Identification

| Name | Function |
|---|---|
| $A_0$ - $A_8$ | Address inputs |
| $\overline{CAS}$ | Column address strobe |
| DSF | Special function pin |
| $I/O_1$ - $I/O_{16}$ | Data inputs and outputs |
| $\overline{LWE}$, $\overline{UWE}$ | Byte write enables |
| $\overline{OE}$ | Output enable |
| $\overline{RAS}$ | Row address strobe |
| GND | Ground |
| $V_{CC}$ | +5-volt power supply |
| NC | No connection |

## Ordering Information

| Part Number | $\overline{RAS}$ Access Time (max) | R/W Cycle Time (max) | Fast-Page Cycle (max) | Package |
|---|---|---|---|---|
| $\mu$PD481440LE-70 | 70 ns | 130 ns | 45 ns | 40-pin plastic SOJ |
| LE-80 | 80 ns | 150 ns | 50 ns | |

## Pin Functions

**$A_0$ - $A_8$ (Address Inputs).** These pins are multiplexed as row and column address inputs. Each of 16 data bits in the random access port corresponds to 262,144 storage cells, which means that 9-bit row addresses and 9-bit column addresses are required to decode one cell location. Row addresses are first used to select one of the 512 possible rows for a read, write, or refresh cycle.

**$I/O_1$ - $I/O_{16}$ (Common Data Inputs and Outputs).** Each of the 16 mask bits can be individually latched at the falling edge of $\overline{RAS}$ in any write cycle and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$, $\overline{LWE}$, or $\overline{UWE}$.

**$\overline{RAS}$ (Row Address Strobe).** This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 8192 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The 9 row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{LWE}$/ $\overline{UWE}$, and DSF are simultaneously latched to determine device operation.

**$\overline{CAS}$ (Column Address Strobe).** This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The 9 column address bits are latched at the falling edge of $\overline{CAS}$.

**DSF (Special Function Control).** At the leading edge of $\overline{RAS}$ and $\overline{CAS}$, the high or low level of DSF is latched to initiate one of the operations shown in table 1.

**$\overline{LWE}$/$\overline{UWE}$ (Write-Per-Bit or Masked Write Control).** At the falling edge of $\overline{RAS}$, the $\overline{LWE}$/$\overline{UWE}$ and DSF inputs must be low and $\overline{CAS}$ high to enable the write-per-bit option.

Either $\overline{LWE}$ or $\overline{UWE}$ must be low to initiate the lower or upper byte mask function. If both are low, then a word masking operation is performed.

**$\overline{OE}$ (Output Enable).** At the $\overline{RAS}$ falling edge, $\overline{CAS}$ and $\overline{LWE}$/$\overline{UWE}$ high and $\overline{OE}$ low initiate a data transfer. $\overline{OE}$ high initiates conventional read or write cycles and ontrols the output buffer in the random access port.

## Addressing

The storage array is arranged in a 512-row by 512-column by 16 I/O matrix whereby each of 16 data bits in the random access port corresponds to 262,144 storage cells, and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins $A_0$ - $A_8$ and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins $A_0$ - $A_8$ and latched onto the chip by $\overline{CAS}$.

All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 8192 cells on the selected row are sensed simultaneously, and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

## Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed: $\overline{LWE}$, $\overline{UWE}$, $I/O_n$ (n = 1 through 16).

**Read Cycle.** A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining $\overline{LWE}$/$\overline{UWE}$ high (inactive) while $\overline{CAS}$ is active. The $I/O_n$ pin remains in high impedance until valid data appears at the output at access time. Device access time $t_{ACC}$ will be the longest of the following four calculated intervals:

- $t_{RAC}$
- $\overline{RAS}$ to $\overline{CAS}$ delay ($t_{RCD}$) + $t_{CAC}$
- $\overline{RAS}$ to column address delay ($t_{RAD}$) + $t_{AA}$
- $\overline{RAS}$ to $\overline{OE}$ delay + $t_{OEA}$

Access times from $\overline{RAS}$ ($t_{RAC}$), from $\overline{CAS}$ ($t_{CAC}$), from the column addresses ($t_{AA}$), and from $\overline{OE}$ ($t_{OEA}$) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance. See explanation of "Extended Data Output."

**Write Cycle.** A write cycle is executed by bringing $\overline{LWE}/\overline{UWE}$ low during the $\overline{RAS}/\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or $\overline{LWE}/\overline{UWE}$ strobes the data on $I/O_n$ into the on-chip data latch. To make use of the write-per-bit option, $\overline{LWE}/\overline{UWE}$ must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping $I/O_n$ high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

**Write-per-Bit-Cycle.** A write-per-bit-cycle uses an I/O masking function to allow the system designer the flexibility of writing or not writing any combinations of $I/O_1$ - $I/O_{16}$. Two types of masking are possible: (1) new mask or the non-persistent mask that requires the user to provide the mask data each cycle and (2) old mask or the persistent mask. With the persistent mask option, an LMR or load mask register cycle is performed and the mask data is used during write, block write, and flash write cycles.

**Early Write Cycle.** An early write cycle is executed by bringing $\overline{LWE}/\overline{UWE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle.

**Read-Write/Read-Modify-Write Cycle.** This cycle is executed by bringing $\overline{LWE}/\overline{UWE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. $I/O_n$ shows read data at access time. Afterward, in preparation for the upcoming write cycle, $I/O_n$ returns to high impedance when $\overline{OE}$ goes high. The data to be written is strobed by $\overline{LWE}/\overline{UWE}$, with setup and hold times referenced to this signal.

**Late Write Cycle.** This cycle shows the timing flexibility of $\overline{OE}$, which can be activated just after $\overline{LWE}/\overline{UWE}$ falls, even when $\overline{LWE}/\overline{UWE}$ is brought low after $\overline{CAS}$.

**Refresh Cycle.** A cycle at each of the 512 row addresses ($A_0$ - $A_8$) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, color register set, flash write, or block write) refreshes the 8192 bits selected by the $\overline{RAS}$ addresses or by the on-chip address counter.

**$\overline{RAS}$-Only Refresh Cycle.** A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep $I/O_n$ in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

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**$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (CBRN).** This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle. This CBR cycle has no effect on the mask mode.

**$\overline{CAS}$ Before $\overline{RAS}$ Cycle (CBR).** CBR has the same function as CBRN except the write-per-bit mask mode is changed to new mask mode.

**Hidden Refresh Cycle.** This cycle is executed after a read cycle without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

## Glossary of Special Functions

Table 1 is a truth table for implementing the functions described below.

**Load Mask Register Cycle (LMR).** In this cycle, data on I/O$_n$ is written to a 16-bit write mask register, where it is retained and used by subsequent masked write and masked block write cycles.

**Masked Write Cycle With New Mask (RWM new mask).** When the write-per-bit function is enabled as shown below, mask data on the I/O$_n$ pins is latched by $\overline{RAS}$ and loaded directly into the write mask register. A masked write cycle is then executed using $\overline{CAS}$ or $\overline{LWE}/\overline{UWE}$ to strobe the I/O$_n$ data into the on-chip data latch.

| Mask Register Data | Action |
|---|---|
| 1 | Write |
| 0 | Do not write |

**Masked Write Cycle With Old Mask (RWM old mask).** This write-per-bit cycle, commonly referred to as a persistent mask write cycle, uses the mask data previously set by the last load mask register cycle.

**Load Color Register Cycle (LCR).** This cycle is executed in the same fashion as a conventional read or write cycle, with a read or write cycle available to the color register under the control of $\overline{LWE}/\overline{UWE}$. In read operation, color register data is read on the common I/O$_n$ pins. In write operation, common I/O$_n$ data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by $A_0$ - $A_8$. This setup cycle precedes the first flash write or block write cycle supplying the 16 write data bits.

**Block Write Cycle (BW no mask).** In a block write cycle, $A_1$ and $A_0$ are ignored. I/O$_1$ - I/O$_4$ are used to select one or a combination of four column addresses for writing in an early lower-byte write, late lower-byte write, page early lower-byte write or page late lower-byte write cycle. I/O$_9$ - I/O$_{12}$ are used for column selection on the upper-byte write cycles.

Block write data is previously stored in the color register using a set color register cycle. Column select data is latched by the I/O$_n$ pins at the falling edge of $\overline{CAS}$ or $\overline{LWE}/\overline{UWE}$. Block write cycles are useful for clearing windows and for accelerating polygon fill operations.

***Table 1. μPD481440 Function Truth Table***

| Mnemonic Code | $\overline{RAS}$ (Notes 1, 2) $\overline{CAS}$ | $\overline{UWE}$ | $\overline{LWE}$ | DSF | $\overline{CAS}$ DSF | Available Function |
|---|---|---|---|---|---|---|
| RW | H | H | H | L | L | Read/write cycle |
| BW | H | H | H | L | H | Read/block write cycle |
| FW | H | L | L | H | X | Flash write cycle |
| FW | H | L | H | H | X | Flash write cycle (upper byte) |
| FW | H | H | L | H | X | Flash write cycle (lower byte) |
| LCR | H | H | H | H | H | Color register set cycle |
| LMR | H | H | H | H | L | Load old mask register cycle |
| RWM | H | L | L | L | L | Read/masked write cycle |
| RWM | H | L | H | L | L | Read/masked write cycle (upper byte) |
| RWM | H | H | L | L | L | Read/masked write cycle (lower byte) |
| BWM | H | L | L | L | H | Read/masked block write cycle |
| BWM | H | L | H | L | H | Read/masked block write cycle (upper byte) |
| BWM | H | H | L | L | H | Read/masked block write cycle (lower byte) |
| CBR | L | H | H | L | X | CBR refresh with reset to new mask |
| CBRN | L | H | H | H | X | CBR refresh with no reset |

**Notes:**

(1) An operation is started by the falling edge of $\overline{RAS}$. The level of CAS, UWE/LWE, and DSF at this negative transition defines the memory operation according to this table.

(2) The $\overline{UWE}$ and $\overline{LWE}$ pins have the OR function. That is if either upper or lower write enable goes low, then depending on $\overline{CAS}$ and $\overline{DSF}$, a byte-controlled FW, RW, or BW will be performed. The inactive write enable has no other function.

(3) X = Don't care.

**Block Write Cycle (BWM new mask).** This cycle allows for $I/O_1$ - $I/O_{16}$ masking during a block write cycle. The masking function is identical to a standard masked write cycle with new mask. The column mask data on the $I/O_n$ pins is latched by $\overline{CAS}$. See table 2.

**Block Write Cycle (BWM old mask).** This cycle uses the masked data previously set by the last LMR cycle to write four consecutive columns. See table 2 for column masking description.

***Table 2. Block Write Addresses***

| Byte | Column Select | | Column Address $A_1$ | $A_0$ | Write |
|---|---|---|---|---|---|
| Lower ($I/O_8$ - $I/O_5$ are Don't Care) | $I/O_4$ | 1 | 1 | 1 | Yes |
| | | 0 | 1 | 1 | No |
| | $I/O_3$ | 1 | 1 | 0 | Yes |
| | | 0 | 1 | 0 | No |
| | $I/O_2$ | 1 | 0 | 1 | Yes |
| | | 0 | 0 | 1 | No |
| | $I/O_1$ | 1 | 0 | 0 | Yes |
| | | 0 | 0 | 0 | No |
| Upper ($I/O_{16}$ - $I/O_{13}$ are Don't Care) | $I/O_{12}$ | 1 | 1 | 1 | Yes |
| | | 0 | 1 | 1 | No |
| | $I/O_{11}$ | 1 | 1 | 0 | Yes |
| | | 0 | 1 | 0 | No |
| | $I/O_{10}$ | 1 | 0 | 1 | Yes |
| | | 0 | 0 | 1 | No |
| | $I/O_9$ | 1 | 0 | 0 | Yes |
| | | 0 | 0 | 0 | No |

**Flash Write Cycle (FW.)** A flash write cycle can clear or set each of the sixteen 512-bit data sets on the selected one of 512 possible rows according to data stored in the previously set color register. Only the byte masking function is provided. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

**Fast-Page Mode With Extended Data Output.** In operation, this mode is the same as standard fast-page mode. A faster data rate is possible by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while CAS cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. During fast-page mode, read, write, and read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the succeeding fast-page write cycle.

## Extended Data Output

The introduction of the extended data output feature causes the output data to remain valid even after $\overline{CAS}$ goes high. This is made possible by the addition of a transparent latch to the data amplifier circuit. Extended data output eliminates the $t_{OFF}$ parameter. The resulting longer data valid time allows for the speedup of the fast-page cycle time. Fast-page mode applications that try to run at minimum cycle times find that timing skews and propagation delays make the data valid time so narrow that reliable sampling is impossible. Extended data output is intended to solve this problem and permit faster page-mode cycle times.



In this operation, data pins $I/O_1$ - $I/O_{16}$ remain in the low-impedance state and the valid data appears after the device access time. Device access time, $t_{PAC}$ (page-mode access time), is the longest of these intervals: $t_{AA}$, $t_{ACP}$, $t_{CAC}$.

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input voltage, high | $V_{IH}$ | 2.4 | | $V_{CC}$ + 1.0 | V |
| Input voltage, low | $V_{IL}$ | −1.0 | | 0.8 | V |
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ambient temperature | $T_A$ | 0 | | 70 | °C |

## Absolute Maximum Ratings

| | |
|---|---|
| Voltage on any pin relative to GND | −1.0 to +7.0 V |
| Operating temperature, $T_{OPR}$ | 0 to +70°C |
| Storage temperature, $T_{STG}$ | −55 to +125°C |
| Short-circuit output current, $I_{OS}$ | 50 mA |
| Power dissipation, $P_D$ | 1.0 W |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

## Capacitance

$T_A$ = 25°C; f = 1 MHz

| Parameter | Symbol | Max | Unit | Pins Under Test |
|---|---|---|---|---|
| Input capacitance | $C_{I1}$ | 5 | pF | Addresses |
| | $C_{I2}$ | 7 | pF | $\overline{RAS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$, DSF |
| Input/output capacitance | $C_O$ | 7 | pF | $I/O_1$ - $I/O_{16}$ |

## DC Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10%

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Standby current | $I_{CC2}$ | | | 2.0 | mA | $\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min); $I_O$ = 0 mA |
| | | | | 1.0 | mA | $\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; $I_O$ = 0 mA |
| Input leakage current | $I_{I(L)}$ | –10 | | 10 | μA | $V_{IN}$ = 0 V to $V_{CC}$; all other pins not under test = 0 V |
| Output leakage current | $I_{O(L)}$ | –10 | | 10 | μA | $D_{OUT}$ disabled; $V_{OUT}$ = 0 V to $V_{CC}$ |
| Output voltage, low | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 2.1 mA |
| Output voltage, high | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = –2.5 mA |

## AC Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10%

| | | -70 | | -80 | | | |
|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit | Test Conditions |
| Operating current, average | $I_{CC1}$ | | 170 | | 155 | mA | $\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Notes 3, 4) |
| Operating current, $\overline{RAS}$-only refresh cycle, average | $I_{CC3}$ | | 170 | | 155 | mA | $\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$ min; $t_{RC} = t_{RC}$ min (Notes 3, 4) |
| Operating current, fast-page cycle, average | $I_{CC4}$ | | 170 | | 155 | mA | $\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min (Notes 3, 4 ) |
| Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average | $I_{CC5}$ | | 170 | | 155 | mA | $\overline{RAS}$ cycling; $\overline{CAS} \leq V_{IL}$ max; $t_{RC} = t_{RC}$ min (Notes 3, 4) |
| Operating current (register set mode) | $I_{CC6}$ | | 170 | | 155 | ns | $\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Notes 3, 4) |
| Operating current (flash write mode) | $I_{CC7}$ | | 170 | | 155 | ns | $\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ min (Notes 3, 4) |
| Operating current (block write mode) | $I_{CC8}$ | | 185 | | 170 | ns | $\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Notes 3, 4) |
| Operating current (fast page block write mode) | $I_{CC9}$ | | 170 | | 155 | ns | $\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; (Notes 3, 4) |
| Access time from column address | $t_{AA}$ | | 35 | | 40 | ns | (Notes 9, 15) |
| Access time from $\overline{CAS}$ precharge (rising edge) | $t_{ACP}$ | | 40 | | 45 | ns | (Note 9) |
| Column address setup time | $t_{ASC}$ | 0 | | 0 | | ns | |
| Row address setup time | $t_{ASR}$ | 0 | | 0 | | ns | |
| Column address to $\overline{UWE}$ delay time | $t_{AWD}$ | 55 | | 65 | | ns | (Note 13) |
| Access time from $\overline{CAS}$ (falling edge) | $t_{CAC}$ | | 20 | | 20 | ns | (Notes 9, 14) |
| Column address hold time | $t_{CAH}$ | 15 | | 15 | | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 20 | 10,000 | 20 | 10,000 | ns | |
| $\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing | $t_{CHR}$ | 15 | | 15 | | ns | (Note 15) |

## AC Characteristics (cont)

| Parameter | Symbol | -70 Min | -70 Max | -80 Min | -80 Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $\overline{\text{CAS}}$ to output in low-Z | $t_{CLZ}$ | 0 | | 0 | | ns | (Note 9) |
| Fast-page $\overline{\text{CAS}}$ precharge time | $t_{CP}$ | 10 | | 10 | | ns | |
| $\overline{\text{CAS}}$ precharge time | $t_{CPN}$ | 10 | | 10 | | ns | |
| Fast-page $\overline{\text{CAS}}$ precharge to $\overline{\text{UWE}}$ delay time | $t_{CPWD}$ | 60 | | 70 | | ns | (Note 13) |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | $t_{CRP}$ | 10 | | 10 | | ns | (Note 10) |
| $\overline{\text{CAS}}$ hold time | $t_{CSH}$ | 70 | | 80 | | ns | |
| $\overline{\text{CAS}}$ setup time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle | $t_{CSR}$ | 10 | | 10 | | ns | (Note 15) |
| $\overline{\text{CAS}}$ to $\overline{\text{UWE}}$ delay | $t_{CWD}$ | 40 | | 45 | | ns | (Note 13) |
| Write command referenced to $\overline{\text{CAS}}$ lead time | $t_{CWL}$ | 15 | | 20 | | ns | |
| Data-in hold time | $t_{DH}$ | 15 | | 15 | | ns | (Note 12) |
| Output hold time from $\overline{\text{CAS}}$ | $t_{DHC}$ | 5 | | 5 | | ns | |
| Data-in setup time | $t_{DS}$ | 0 | | 0 | | ns | (Note 12) |
| DSF setup time from $\overline{\text{CAS}}$ | $t_{FCS}$ | 0 | | 0 | | ns | |
| DSF hold timefrom $\overline{\text{CAS}}$ | $t_{FCH}$ | 12 | | 15 | | ns | |
| DSF hold time from $\overline{\text{RAS}}$ | $t_{FRH}$ | 10 | | 12 | | ns | |
| DSF setup time from $\overline{\text{RAS}}$ | $t_{FRS}$ | 0 | | 0 | | ns | |
| Mask write hold time referenced to $\overline{\text{CAS}}$ precharge | $t_{MCH}$ | 0 | | 0 | | ns | |
| Mask write setup time | $t_{MCS}$ | 0 | | 0 | | ns | |
| Masked byte hold time referenced to $\overline{\text{RAS}}$ | $t_{MRH}$ | 0 | | 0 | | ns | |
| Access time from $\overline{\text{OE}}$ | $t_{OEA}$ | | 20 | | 20 | ns | (Notes 3, 4, 7, 8) |
| $\overline{\text{OE}}$ data delay time | $t_{OED}$ | 15 | | 20 | | ns | |
| $\overline{\text{OE}}$ command hold time | $t_{OEH}$ | 0 | | 0 | | ns | |
| $\overline{\text{OE}}$ to $\overline{\text{RAS}}$ inactive setup time | $t_{OES}$ | 0 | | 0 | | ns | |
| Output turnoff delay from $\overline{\text{OE}}$ | $t_{OEZ}$ | 0 | 15 | 0 | 20 | ns | (Note 10) |
| Output disable time from $\overline{\text{CAS}}$ high | $t_{OFC}$ | 0 | 15 | 0 | 20 | ns | (Note 17) |
| Output disable time from $\overline{\text{RAS}}$ high | $t_{OFR}$ | 0 | 15 | 0 | 20 | ns | (Note 17) |
| $\overline{\text{OE}}$ to output in low-Z | $t_{OLZ}$ | 0 | | 0 | | ns | |
| Fast-page read or write cycle time | $t_{PC}$ | 35 | | 40 | | ns | |
| Fast-page read-modify-write cycle time | $t_{PRWC}$ | 95 | | 105 | | ns | |
| Access time from $\overline{\text{RAS}}$ | $t_{RAC}$ | | 70 | | 80 | ns | (Notes 9, 14, 15) |
| $\overline{\text{RAS}}$ to column address delay time | $t_{RAD}$ | 15 | 35 | 15 | 40 | ns | (Note 15) |
| Row address hold time | $t_{RAH}$ | 10 | | 10 | | ns | |

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## AC Characteristics (cont)

| Parameter | Symbol | -70 Min | -70 Max | -80 Min | -80 Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Column address lead time referenced to $\overline{RAS}$ (rising edge) | $t_{RAL}$ | 35 | | 40 | | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 70 | 10,000 | 80 | 10,000 | ns | |
| Fast-page $\overline{RAS}$ pulse width | $t_{RASP}$ | 70 | 125,000 | 80 | 125,000 | ns | |
| Random read or write cycle time | $t_{RC}$ | 130 | | 150 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 20 | 50 | 20 | 60 | ns | (Note 14) |
| Read command hold time referenced to $\overline{CAS}$ | $t_{RCH}$ | 0 | | 0 | | ns | (Note 11) |
| Read command setup time | $t_{RCS}$ | 0 | | 0 | | ns | |
| Refresh period | $t_{REF}$ | | 8 | | 8 | ms | Addresses $A_0$ - $A_8$ |
| $\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge | $t_{RHCP}$ | 40 | | 45 | | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 50 | | 60 | | ns | |
| $\overline{RAS}$ precharge $\overline{CAS}$ hold time | $t_{RPC}$ | 5 | | 5 | | ns | |
| Read command hold time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | | 0 | | ns | |
| Access time from DSF | $t_{RSA}$ | | 25 | | 30 | ns | (Note 9) |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 20 | | 20 | | ns | |
| Read-modify-write cycle time | $t_{RWC}$ | 175 | | 200 | | ns | |
| $\overline{RAS}$ to $\overline{UWE}$ delay | $t_{RWD}$ | 90 | | 105 | | ns | (Note 13) |
| Write command referenced to $\overline{RAS}$ lead time | $t_{RWL}$ | 20 | | 25 | | ns | |
| Rise and fall transition time | $t_T$ | 3 | 50 | 3 | 50 | ns | (Note 8) |
| Write-per-bit hold time | $t_{WBH}$ | 10 | | 12 | | ns | |
| Write-per-bit setup time | $t_{WBS}$ | 0 | | 0 | | ns | |
| Write command hold time | $t_{WCH}$ | 15 | | 15 | | ns | |
| Write command setup time | $t_{WCS}$ | 0 | | 0 | | ns | (Note 13) |
| Output disable time from $\overline{WE}$ low | $t_{WEZ}$ | 0 | 15 | 0 | 20 | ns | (Note 17) |
| Write bit selection hold time | $t_{WH}$ | 10 | | 12 | | ns | |
| Write command pulse width | $t_{WP}$ | 15 | | 15 | | ns | (Note 16) |
| Write command pulse width | $t_{WPZ}$ | 15 | | 15 | | ns | (Note 18) |
| Write bit selection set-up time | $t_{WS}$ | 0 | | 0 | | ns | |

## AC Characteristics (cont)

**Notes:**

(1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

(2) All voltages are referenced to GND.

(3) $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, , $I_{CC5}$, $I_{CC6}$, $I_{CC7}$, $I_{CC8}$, and $I_{CC9}$ depend on cycle rate

(4) $I_{CC1}$, $I_{CC4}$, $I_{CC6}$, $I_{CC8}$, and $I_{CC9}$ depend on output loading. Specified values are obtained with outputs open.

(5) Column Address can be changed once while $\overline{RAS}$ = $V_{IL}$ and $\overline{CAS}$ = $V_{IH}$

(6) An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(7) Ac measurements assume $t_T$ = 5 ns.

(8) $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring the timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.

(9) Measured with a load equivalent to TTL load and 100 pF.

(10) $t_{OFF}$ (max) and $t_{OEZ}$ (max) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

(11) Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

(12) These parameters are referenced to $\overline{CAS}$ leading edge in early wirte cyles and to $\overline{LWE}/\overline{UWE}$ leading edge in late write cycles and in read-modify-write cycles.

(13) $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{CPWD}$, and $t_{AWD}$ are restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither set of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

(14) Operation within the $t_{RCD}$ (max) limit insures $t_{RAC}$ (max) can be met. Delay time $t_{RCD}$ (max) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled by $t_{CAC}$.

(15) Operation within the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met. Delay time $t_{RAD}$ (max) is specified as a reference point only. If $t_{RAD}$ is longer than the specified $t_{RAD}$ (max) limits, then access time is controlled by $t_{AA}$.

(16) $t_{WP}$ is applicable for late write cycle or read-modify-write cycle. In early write cycle, $t_{WCH}$ (min) should be satisfied.

(17) $t_{WEZ}$, $t_{OFC}$, and $t_{OFR}$ define the time at which the outputs achieve the open circuit condition and output control dependence on $\overline{OE}$ becomes invalid. The effective time is "the earlier of $t_{WEZ}$ and the later of $t_{OFC}$ and $t_{OFR}$." In addition, to make $t_{WEZ}$ effective, $t_{WPZ}$ must be satisfied.

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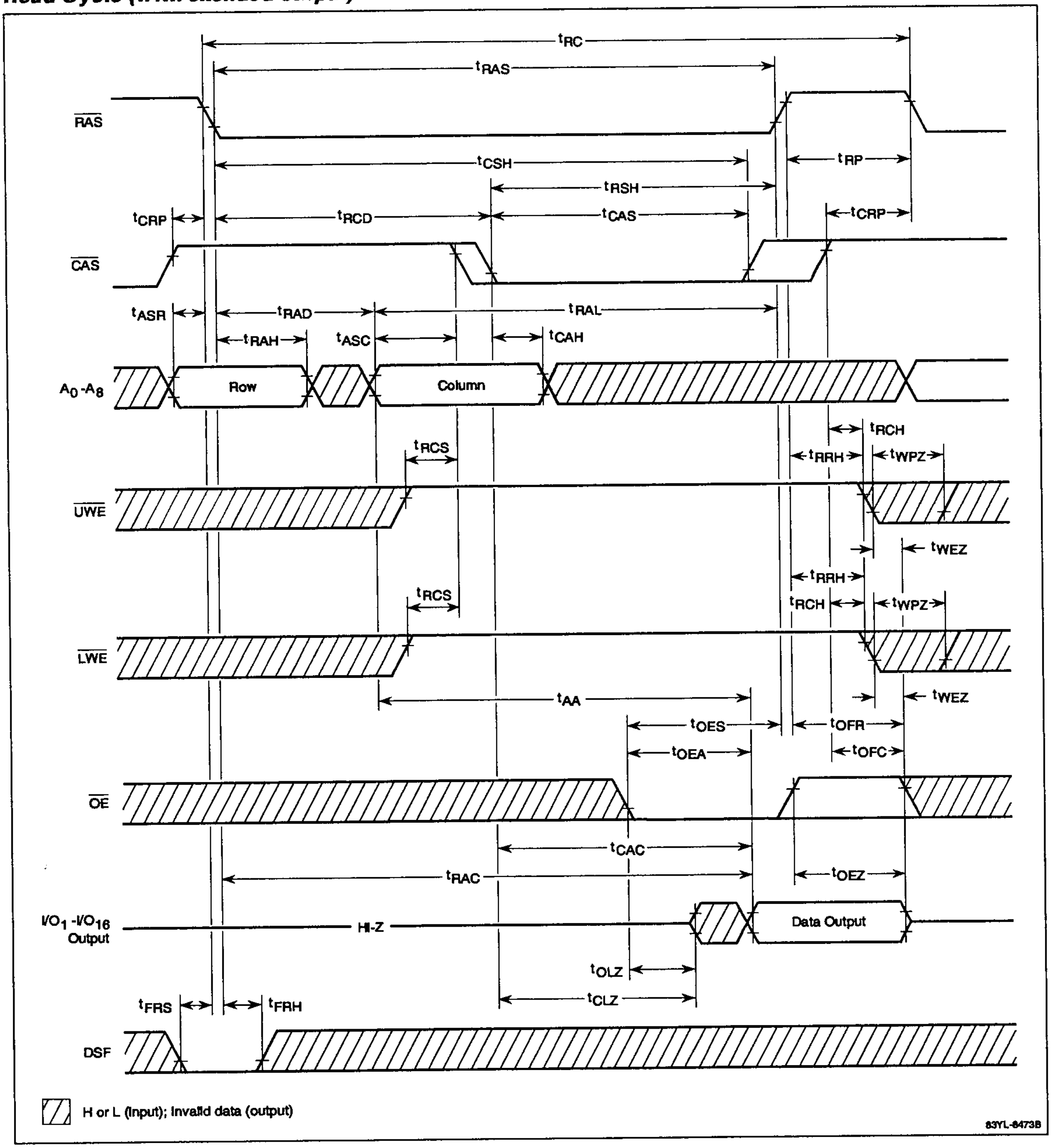
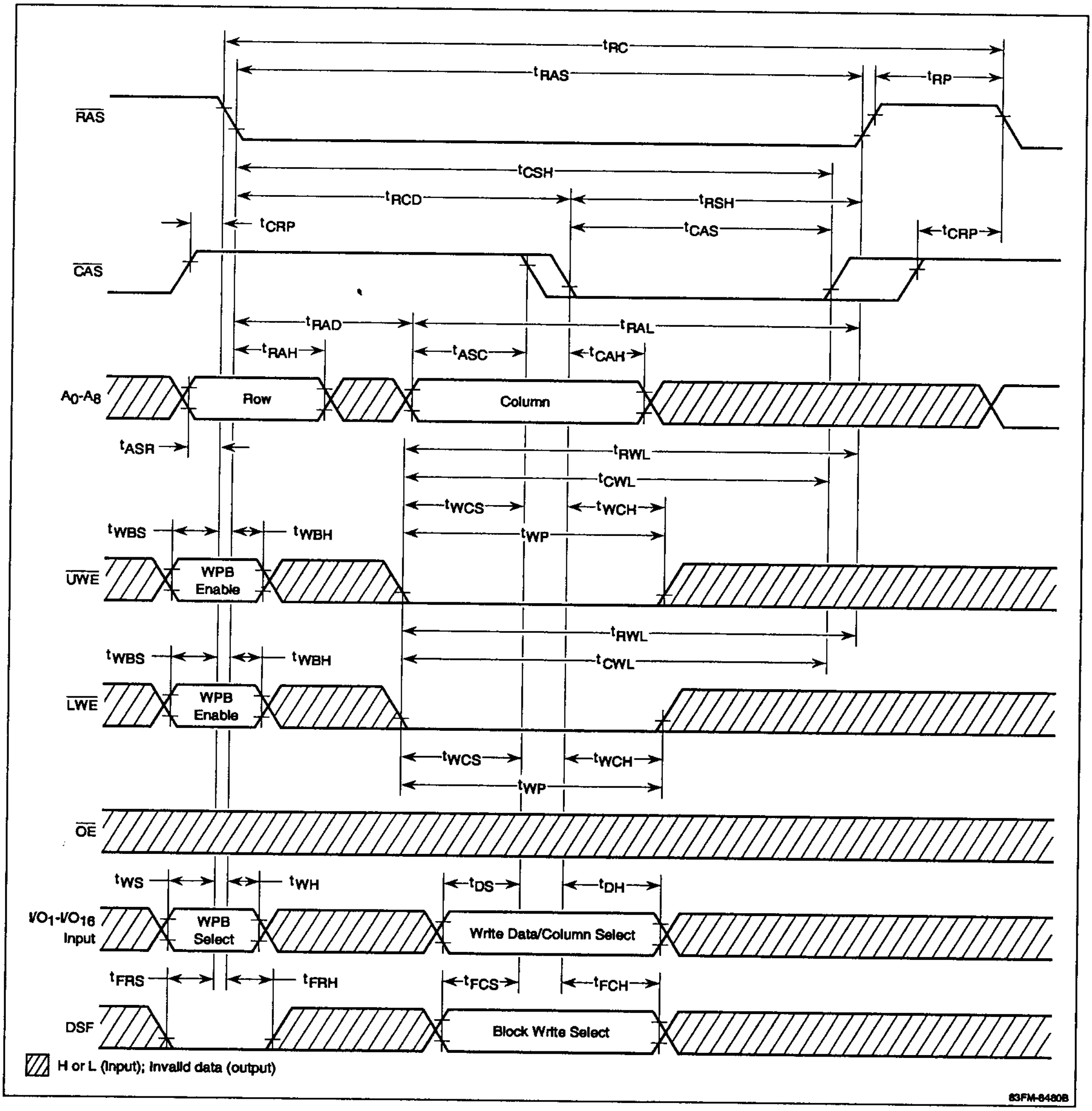
## Timing Waveforms

### *Read Cycle (With exended output)*



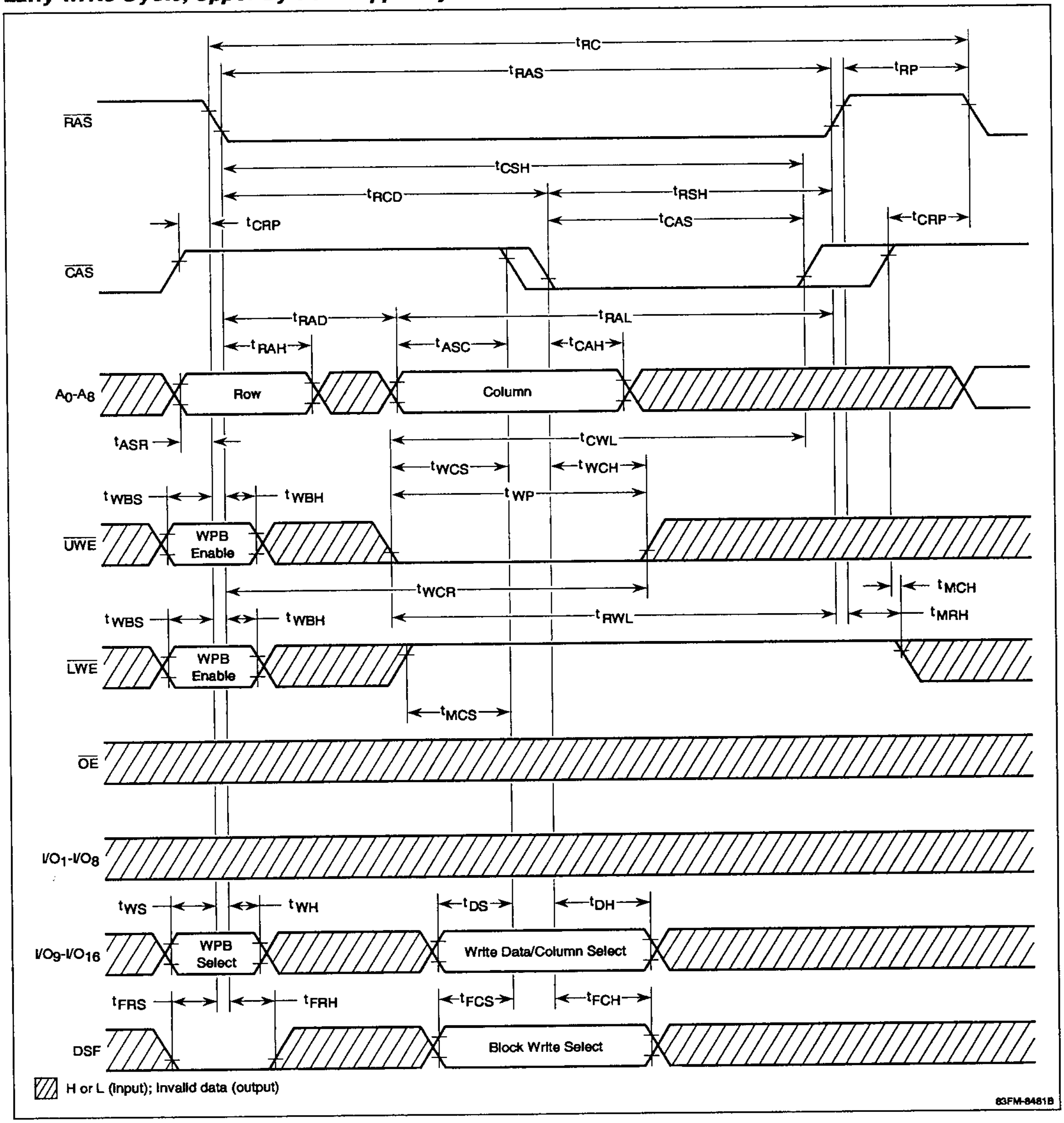
## Timing Waveforms (cont)

### *Early-Write Cycle; Word and Word Block*



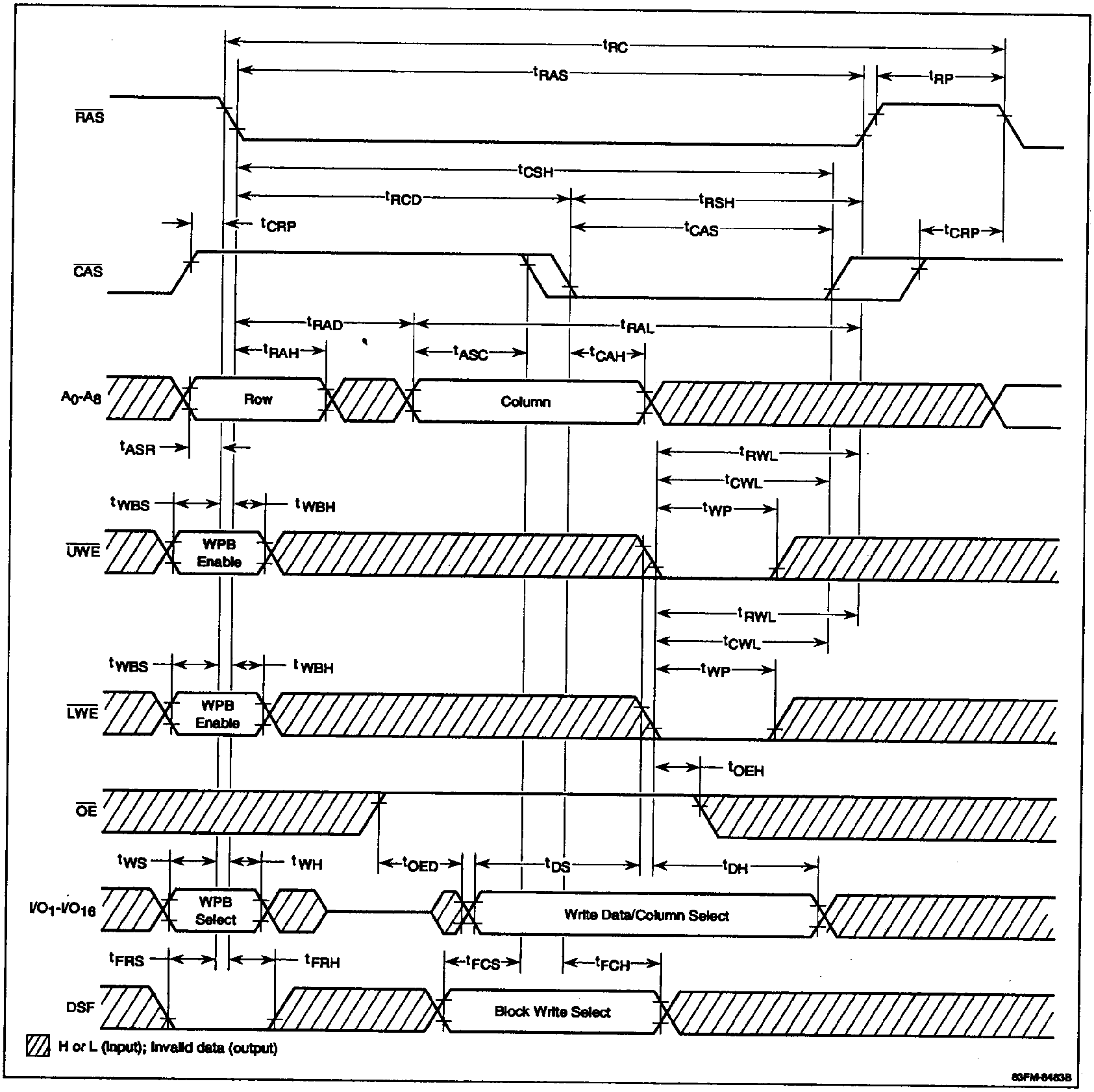
## Timing Waveforms (cont)

### *Early-Write Cycle; Upper-Byte and Upper-Byte Block*



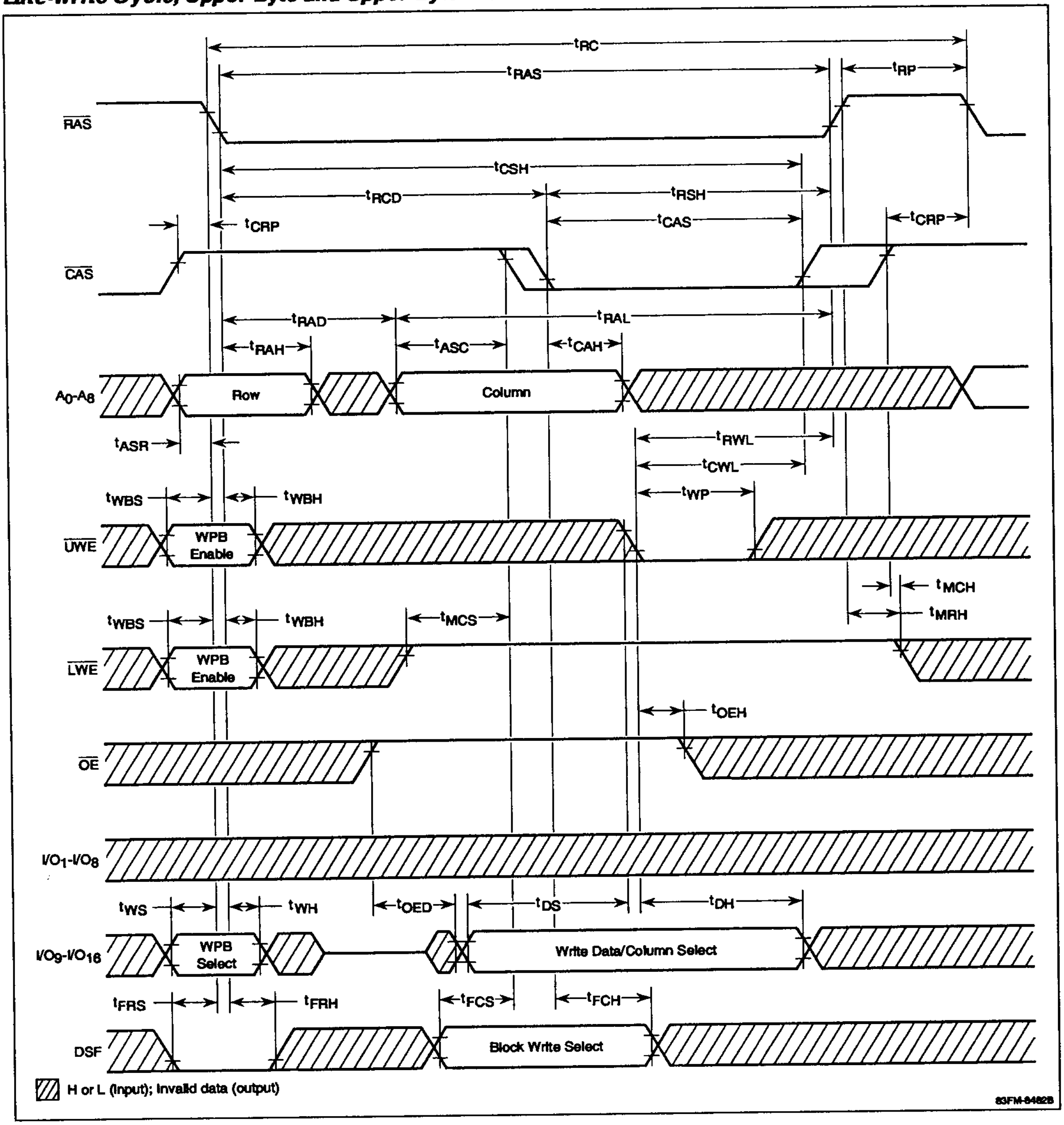
## Timing Waveforms (cont)

### *Late-Write Cycle; Word and Word Block*



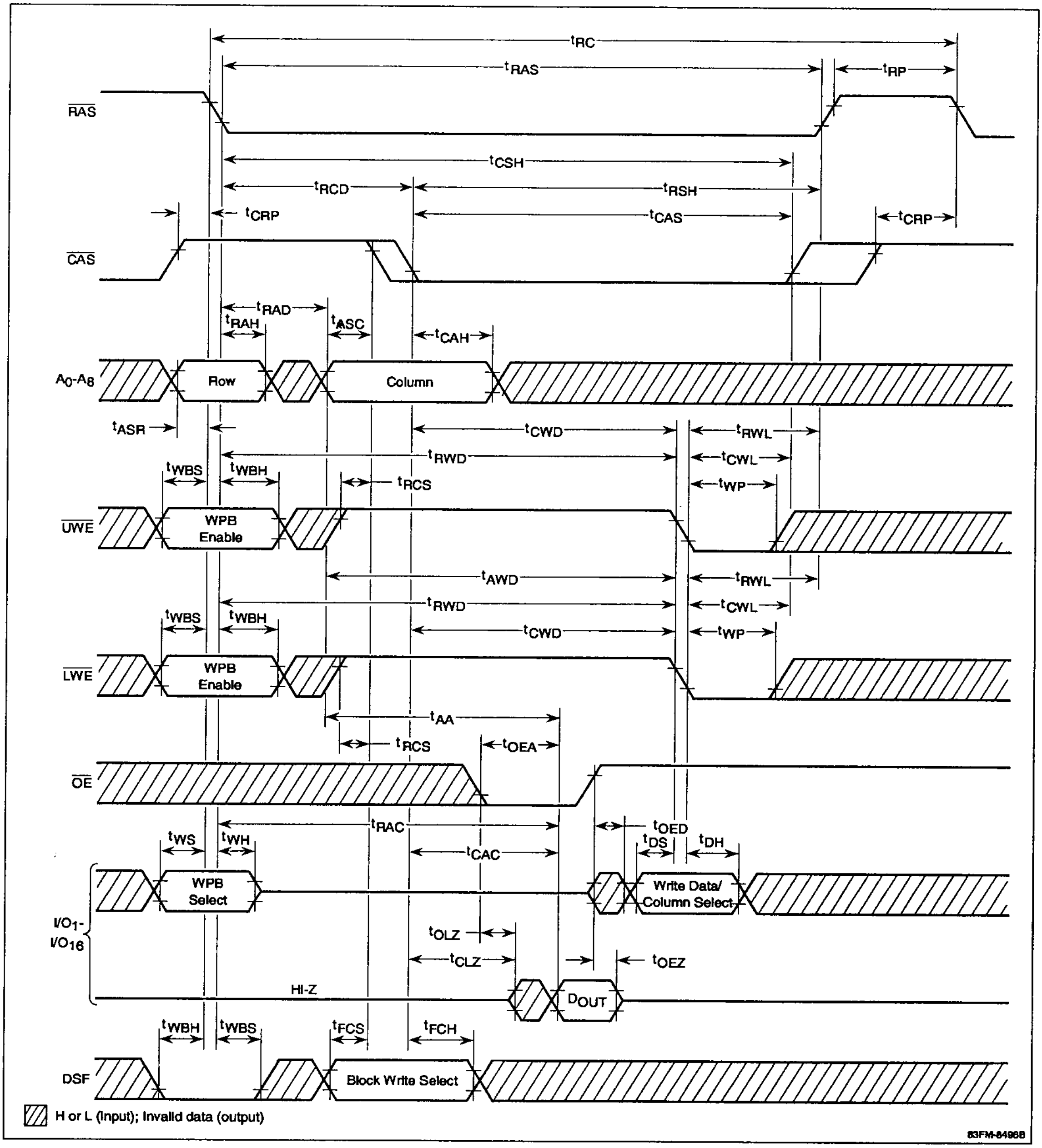
## Timing Waveforms (cont)

### *Late-Write Cycle; Upper-Byte and Upper-Byte Block*

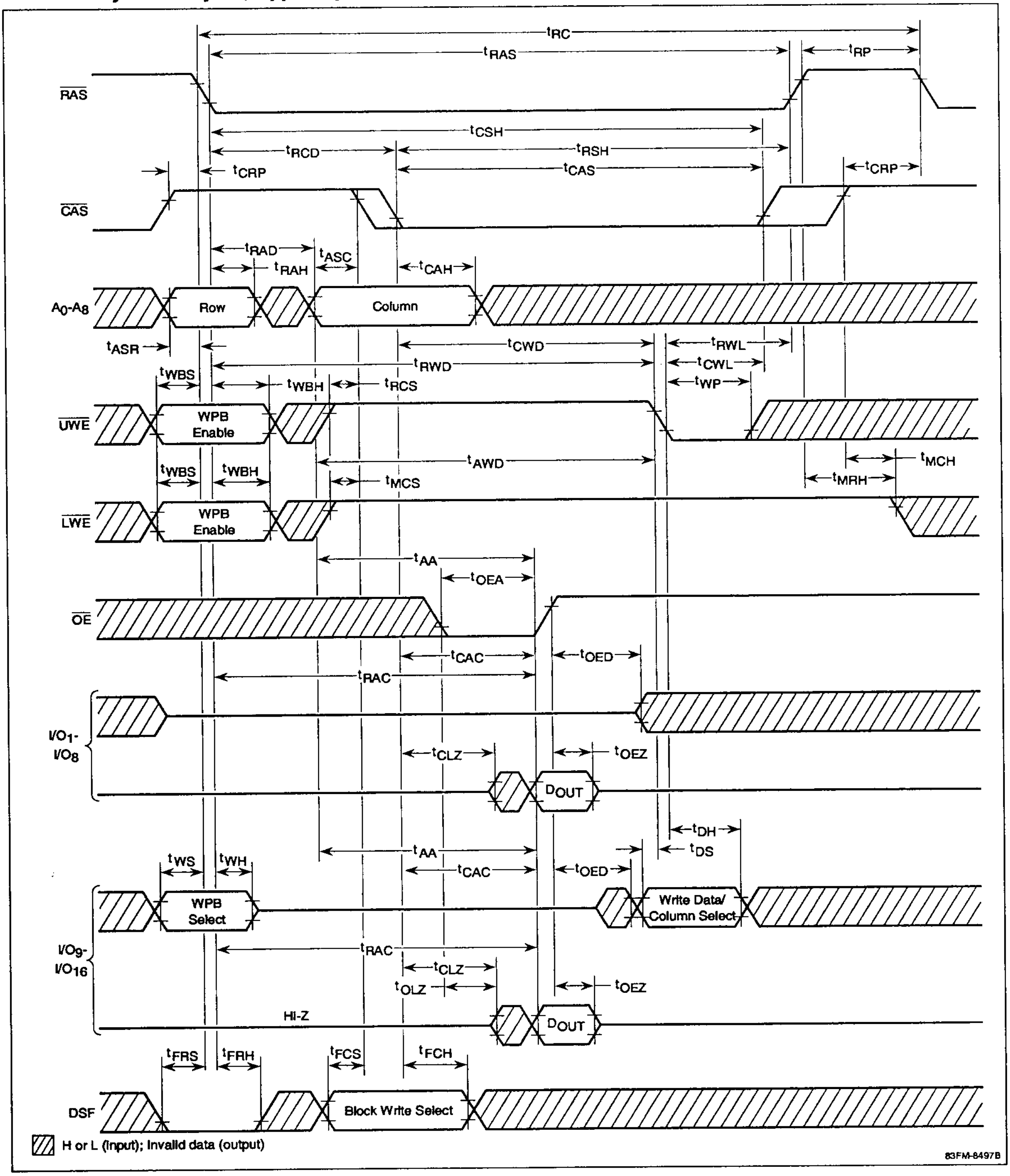


## Timing Waveforms (cont)

***Read-Modify-Write Cycle; Word and Word Block***

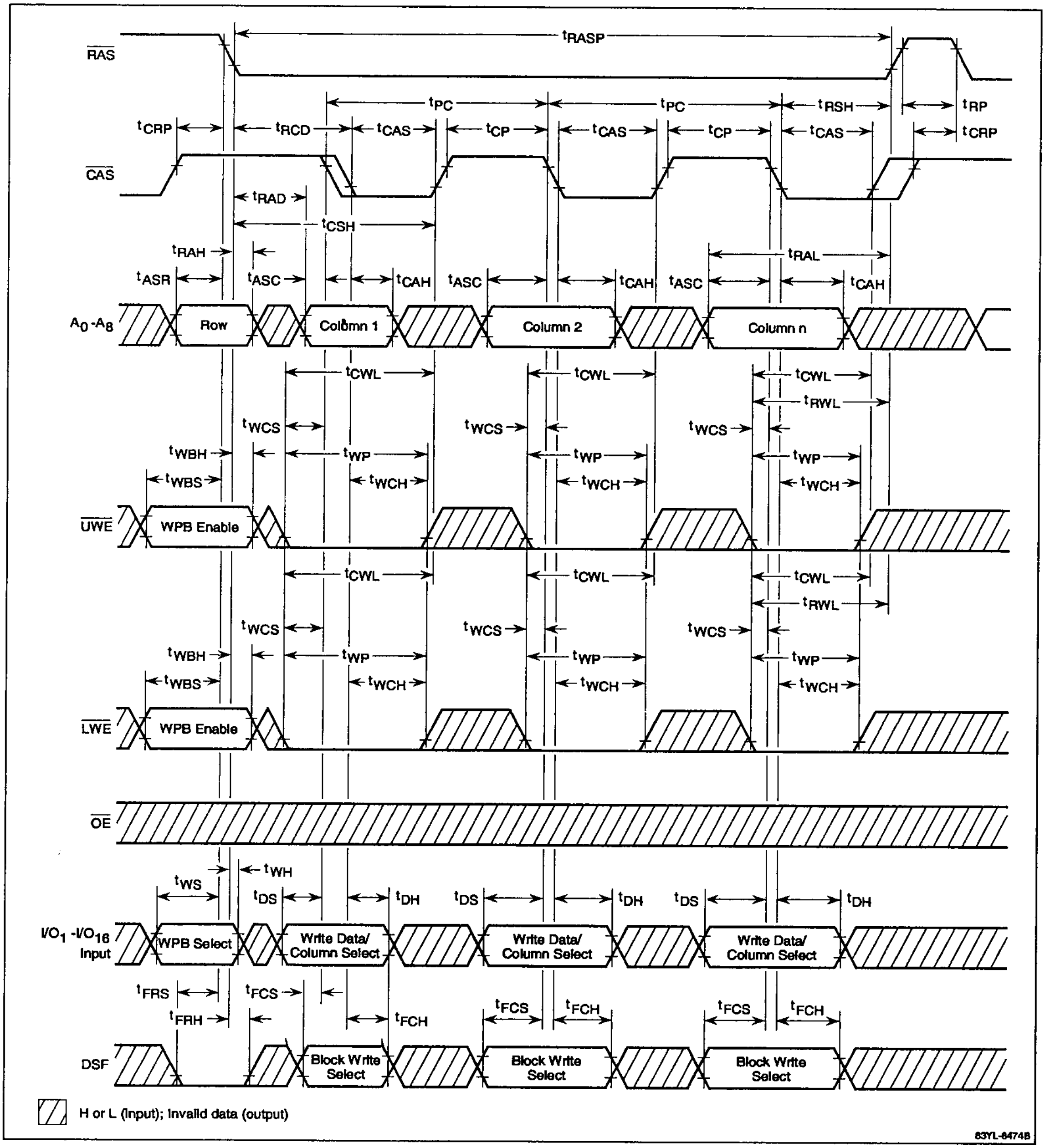


### Read-Modify-Write Cycle; Upper-Byte and Upper-Byte Block



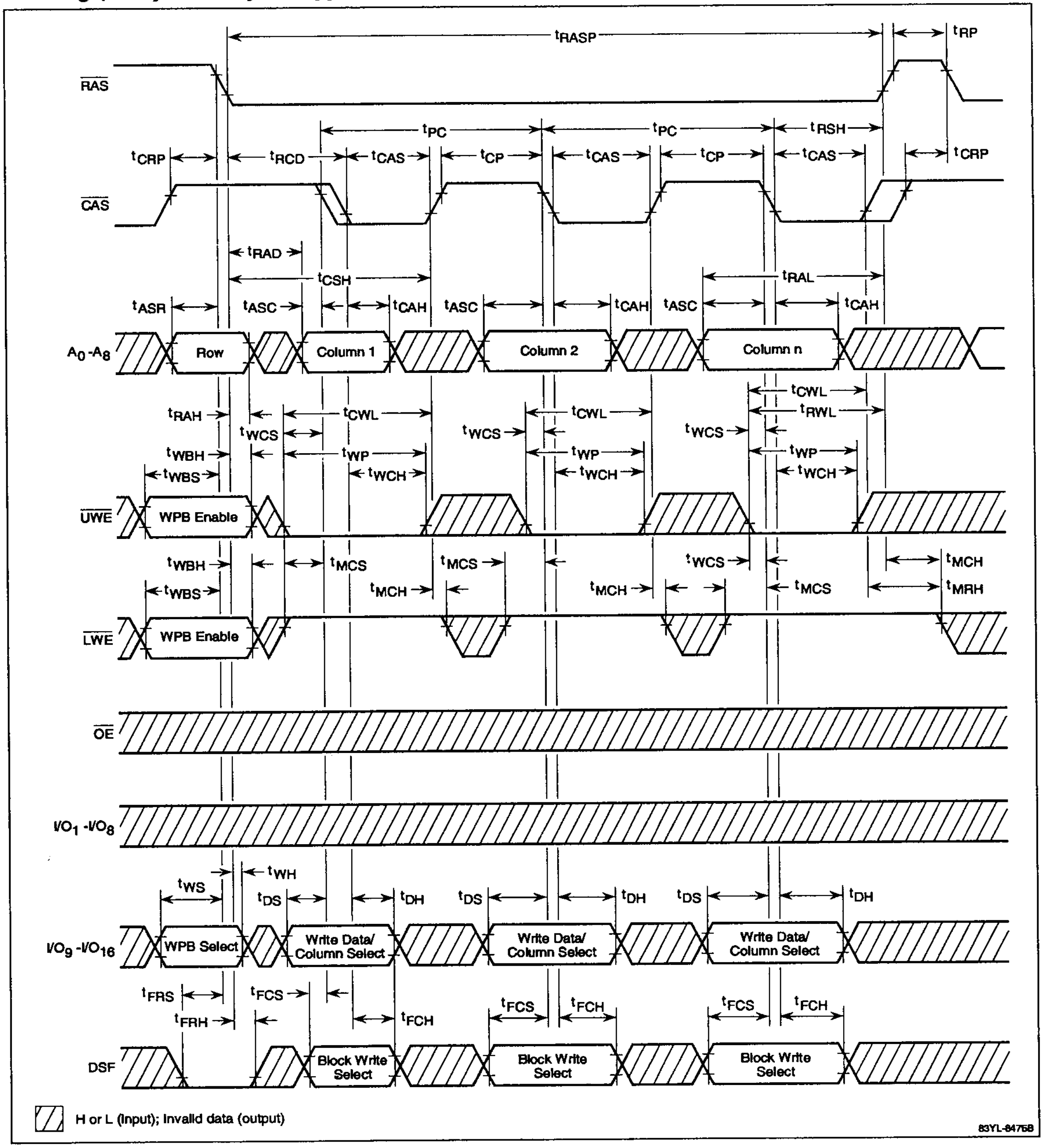
## Timing Waveforms (cont)

***Fast-Page, Early-Write Cycle; Word and Word Block***



## Timing Waveforms (cont)

### *Fast-Page, Early-Write Cycle; Upper-Byte and Upper-Byte Block*



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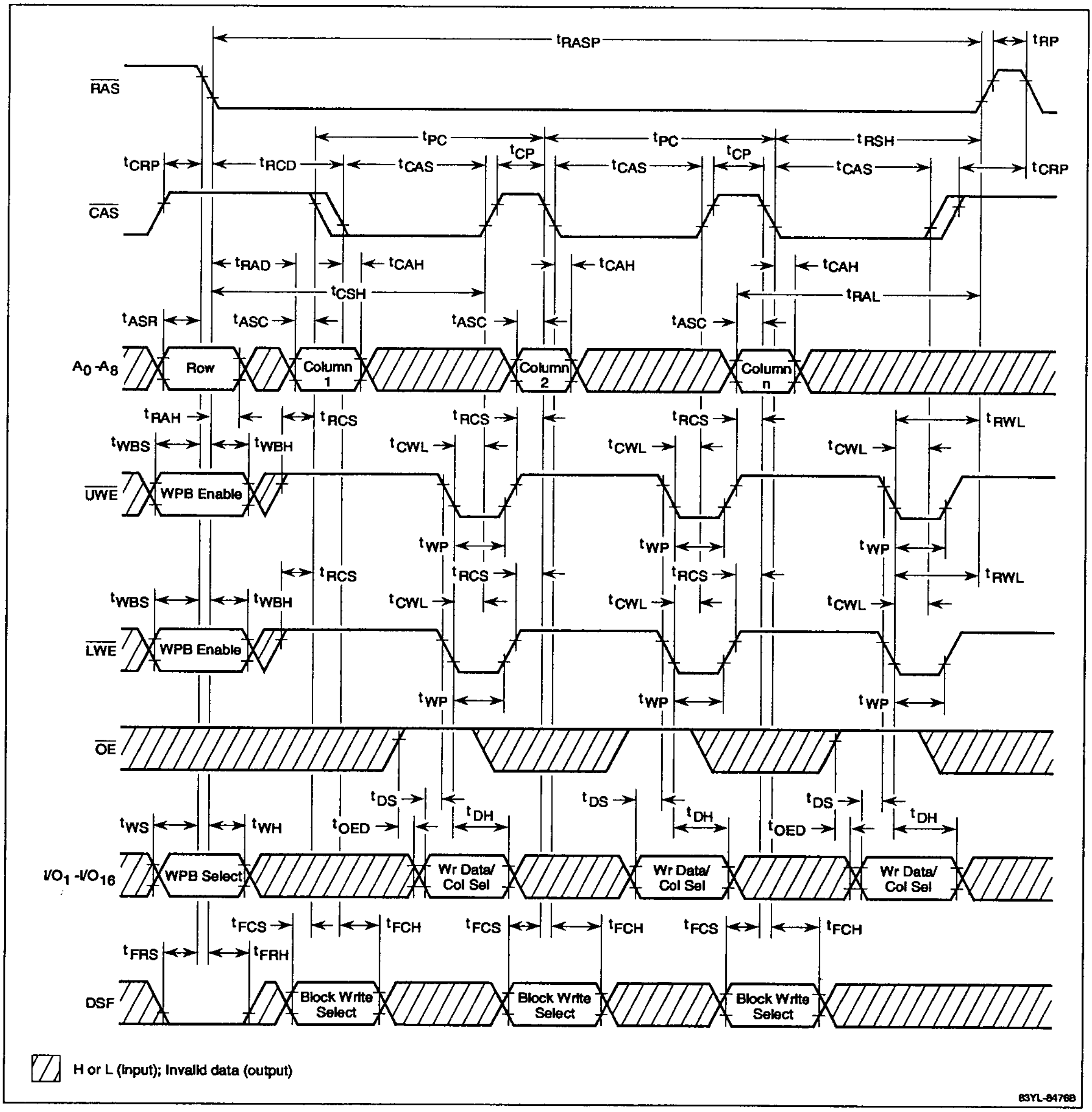
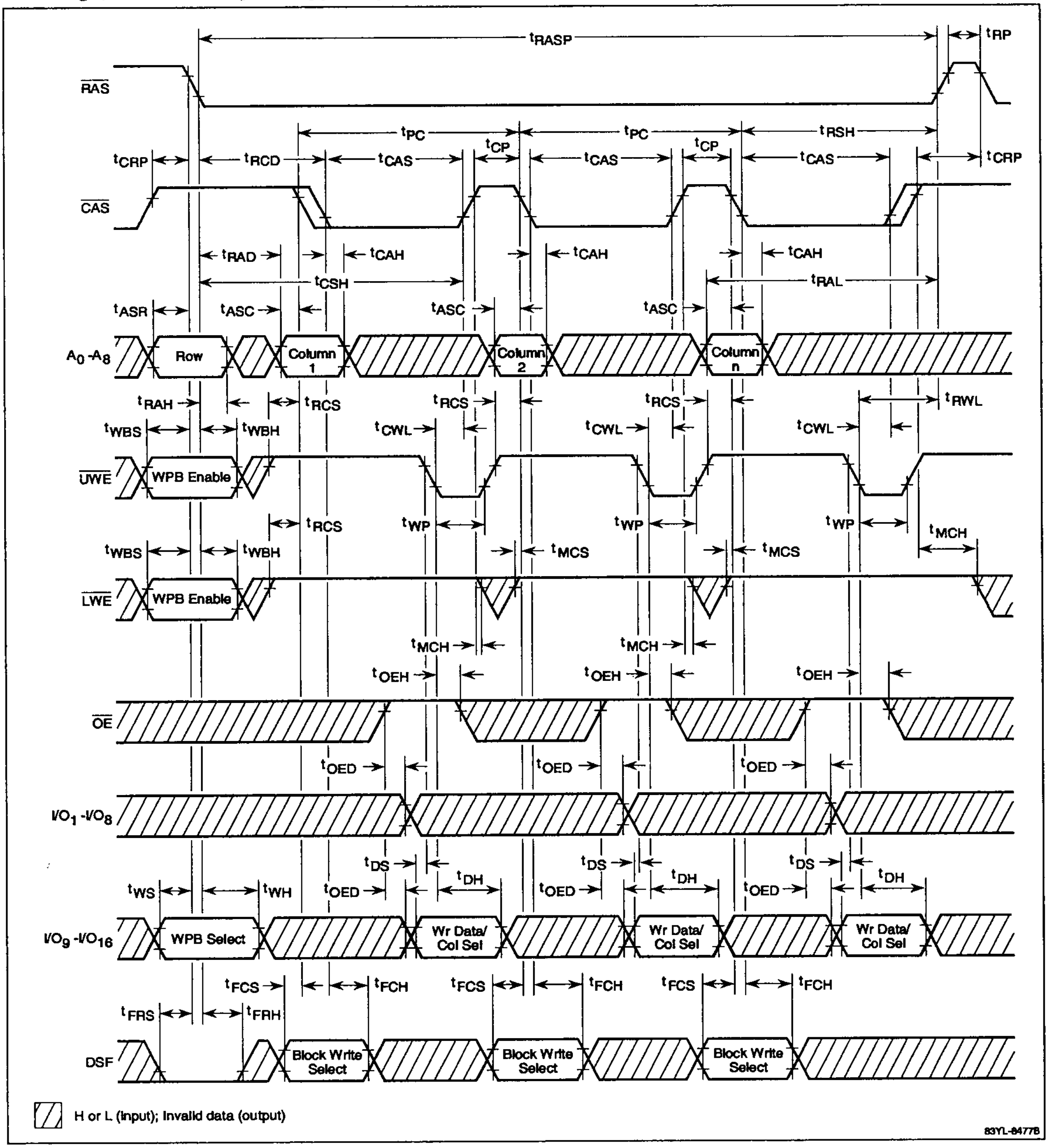
## Timing Waveforms (cont)

### *Fast-Page, Late-Write Cycle; Word and Word Block*



## Timing Waveforms (cont)

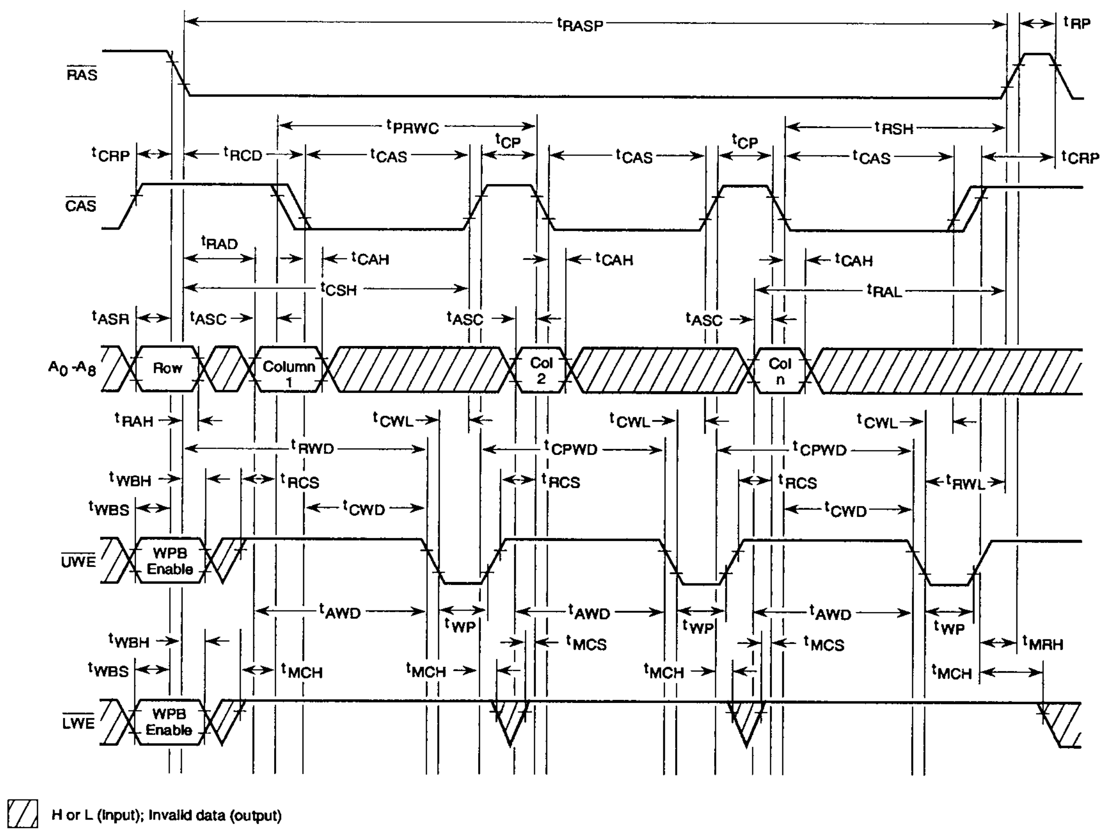
### *Fast-Page, Late-Write Cycle; Upper-Byte and Upper-Byte Block*



18m

## Timing Waveforms (cont)

***Fast-Page, Read-Modify-Write Cycle (With exended output); Upper-Byte and Upper-Byte Block (Sheet 1 of 2)***




The waveforms above are repeated on sheet 2 but without the timing parameters.

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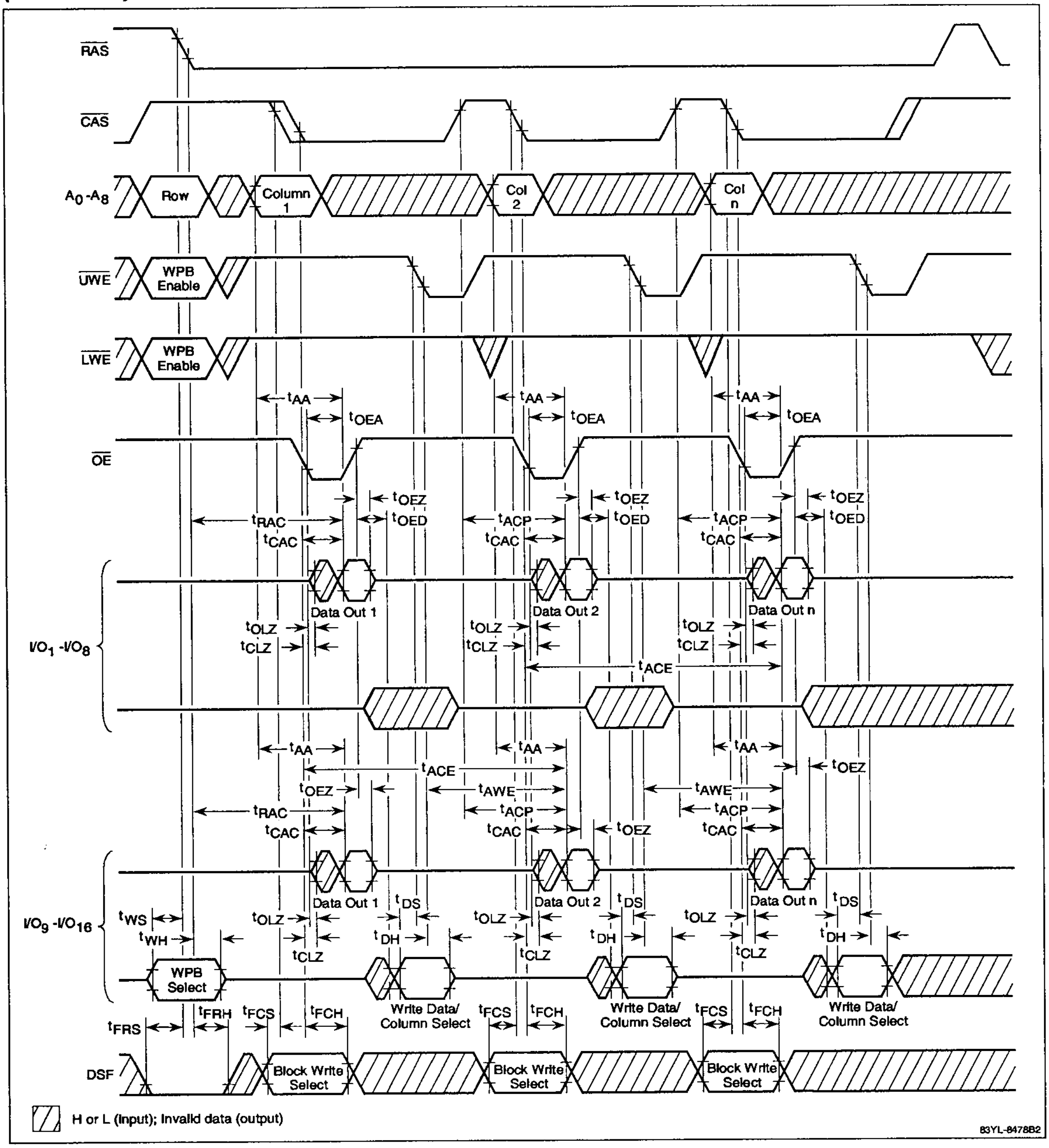
## Timing Waveforms (cont)

### *Fast-Page, Read-Modify-Write Cycle (With exended output); Upper-Byte and Upper-Byte Block (Sheet 2 of 2)*



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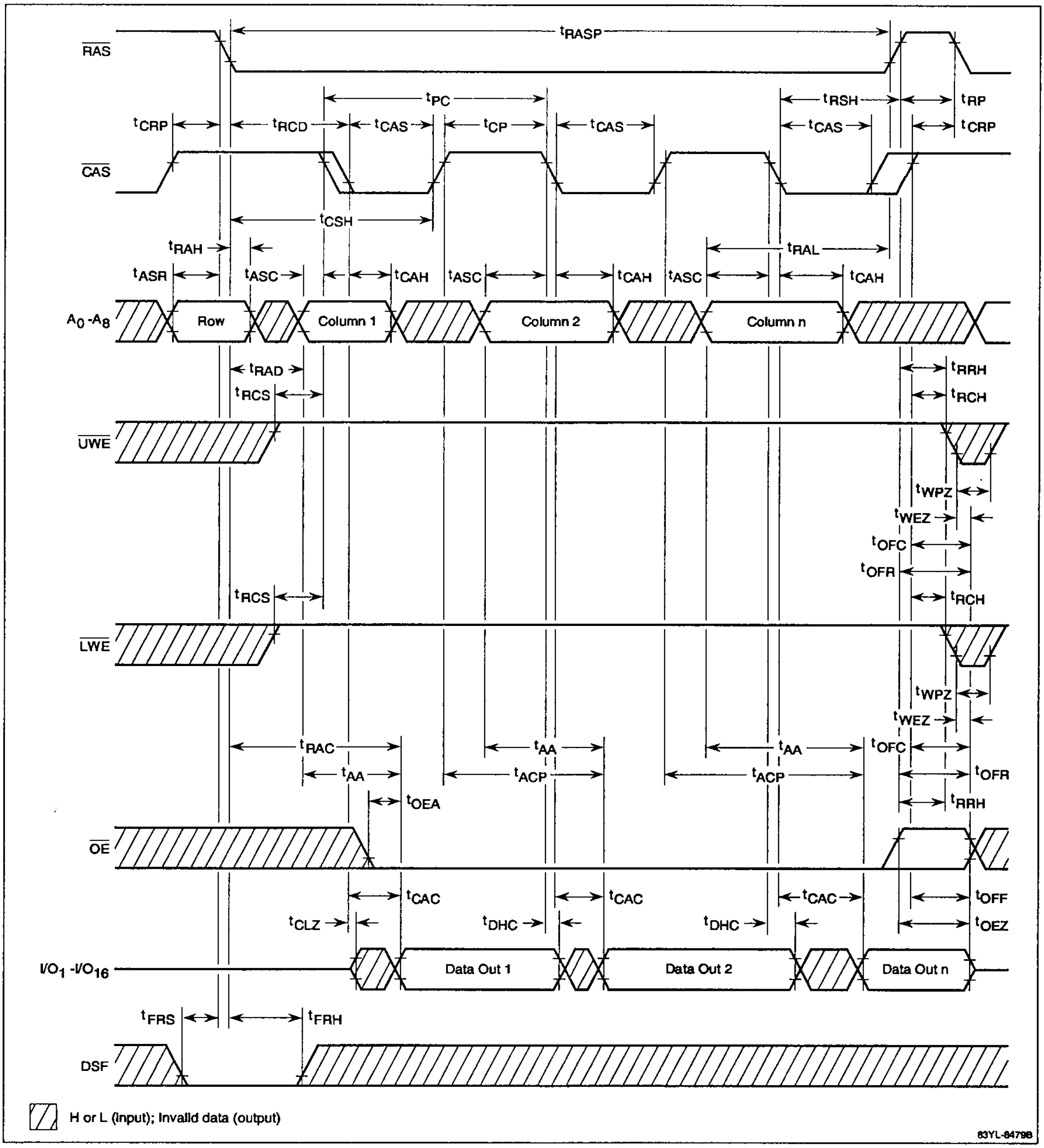
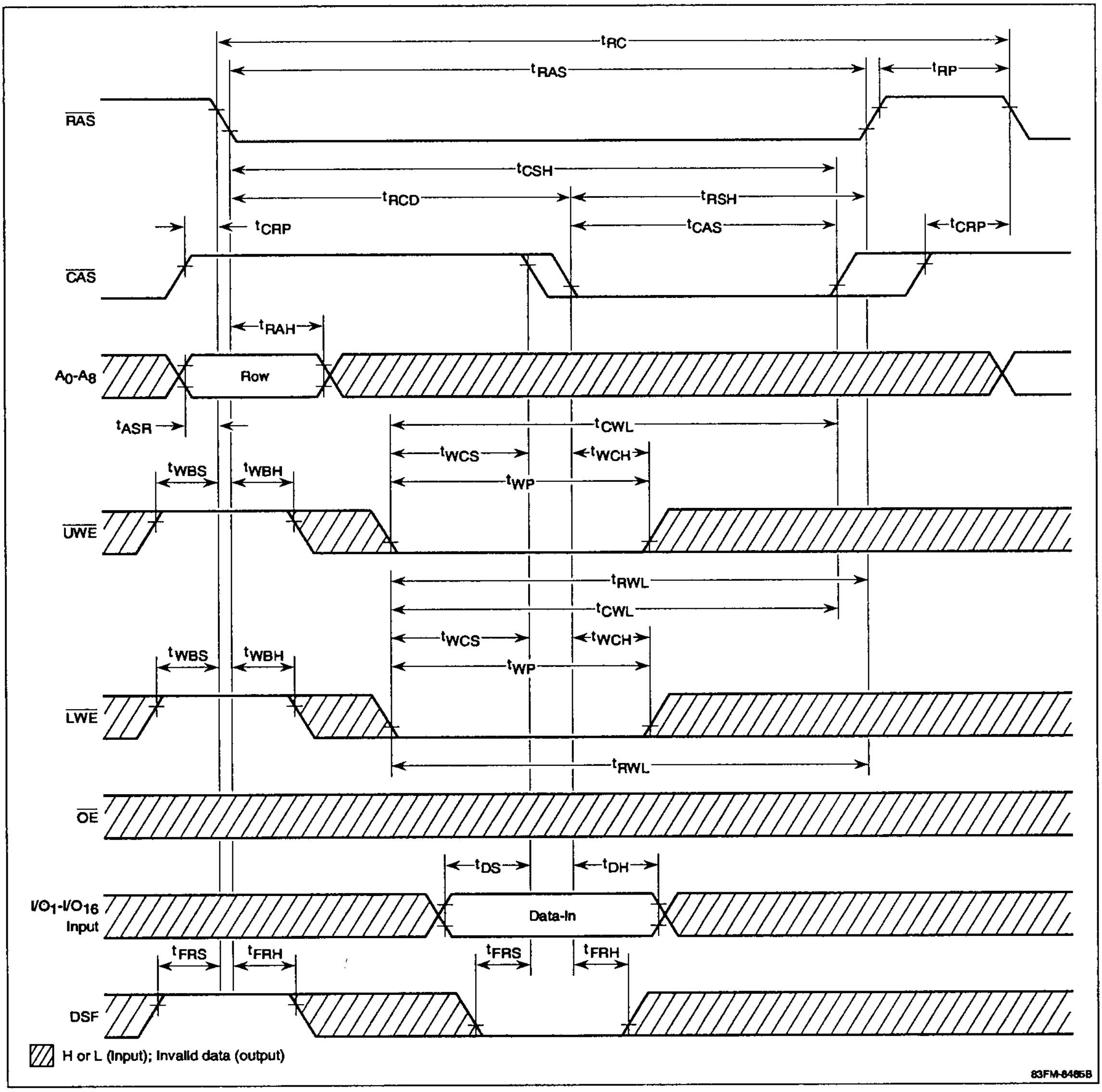
## Timing Waveforms (cont)

### *Fast-Page, Read Cycle (With extended output); Word*



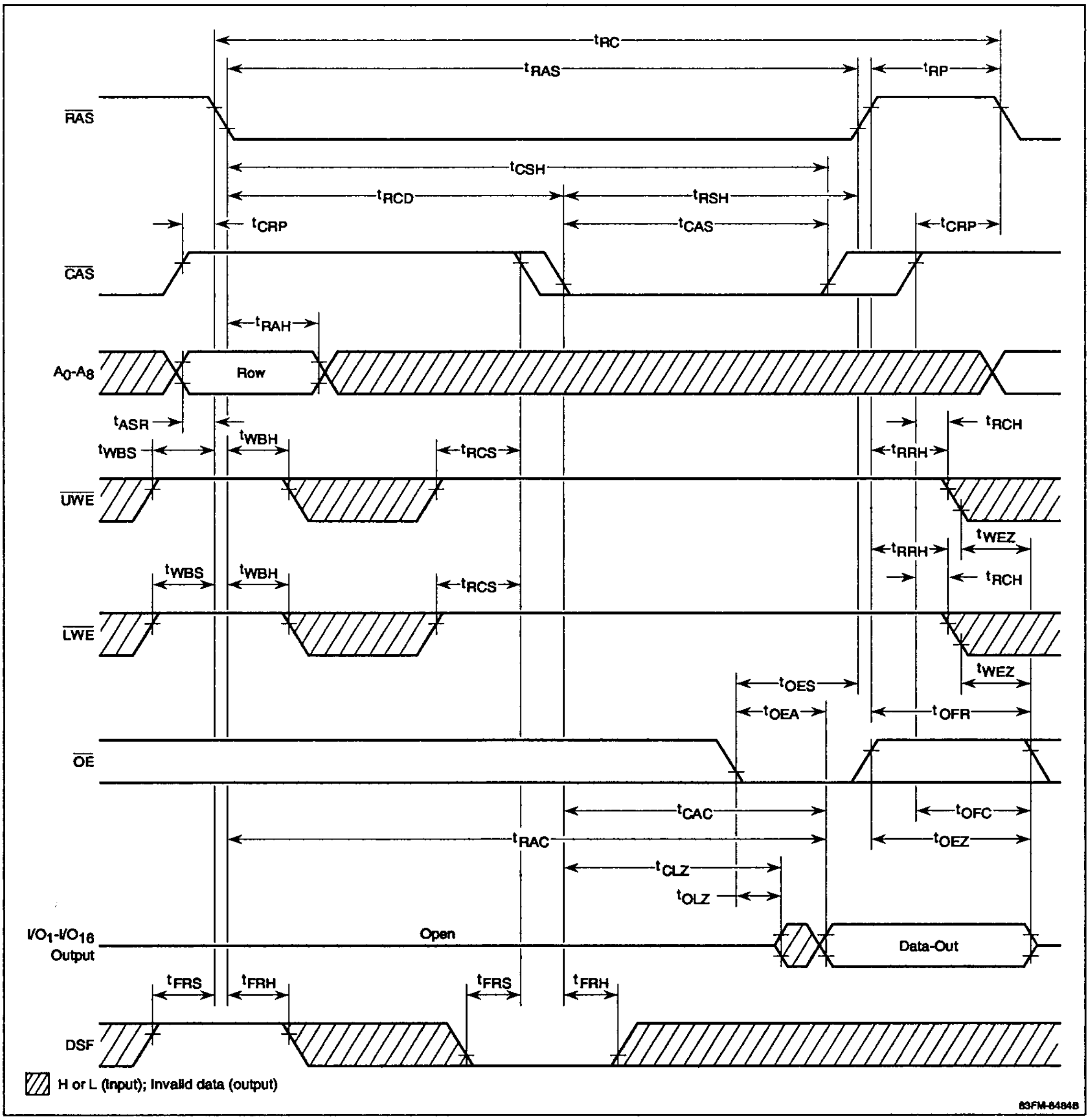
## Timing Waveforms (cont)

### *Load Old Mask Register Cycle (Early-write)*



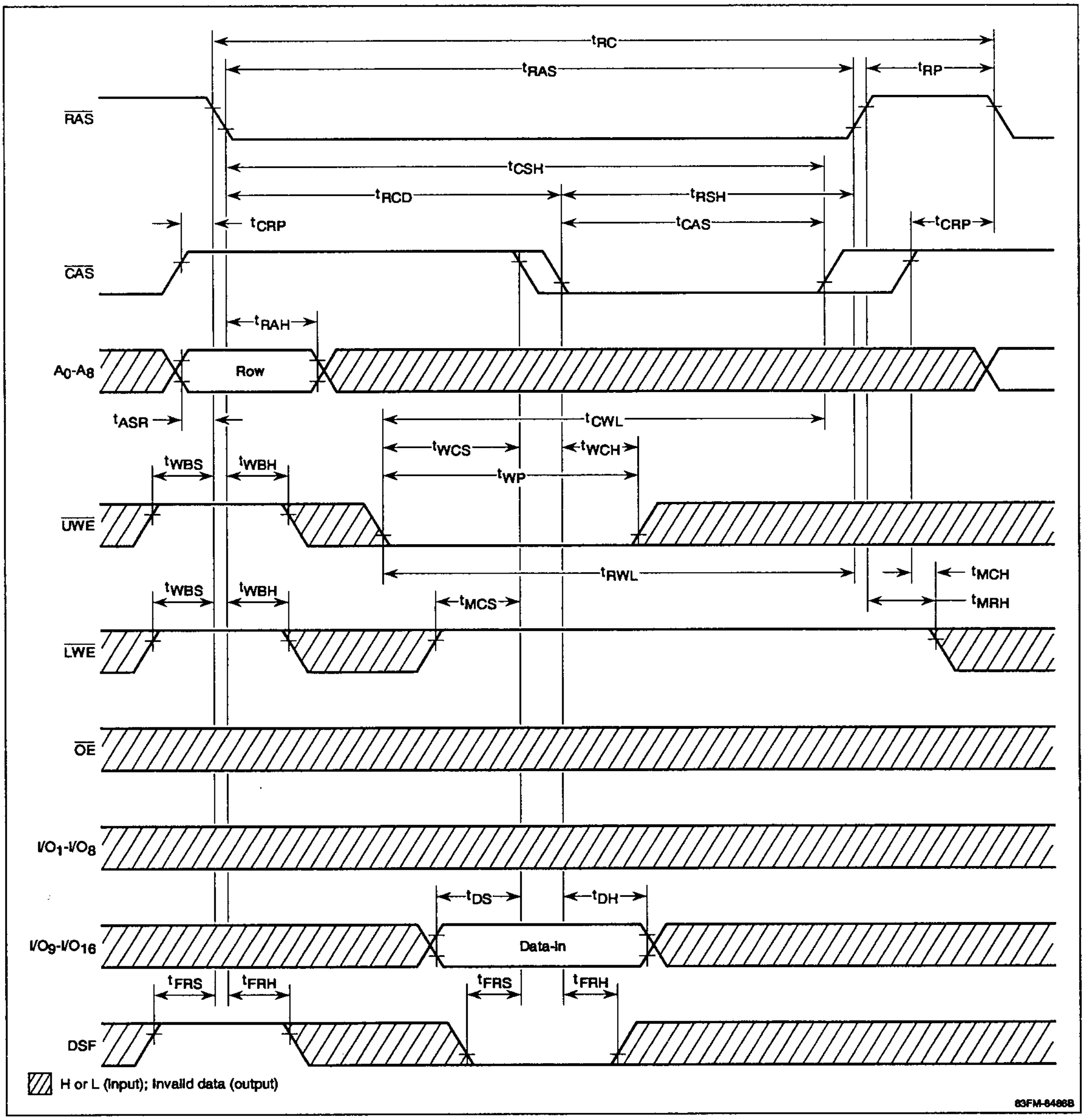
## Timing Waveforms (cont)

### *Load Old Mask Register Cycle (Read with extended output)*



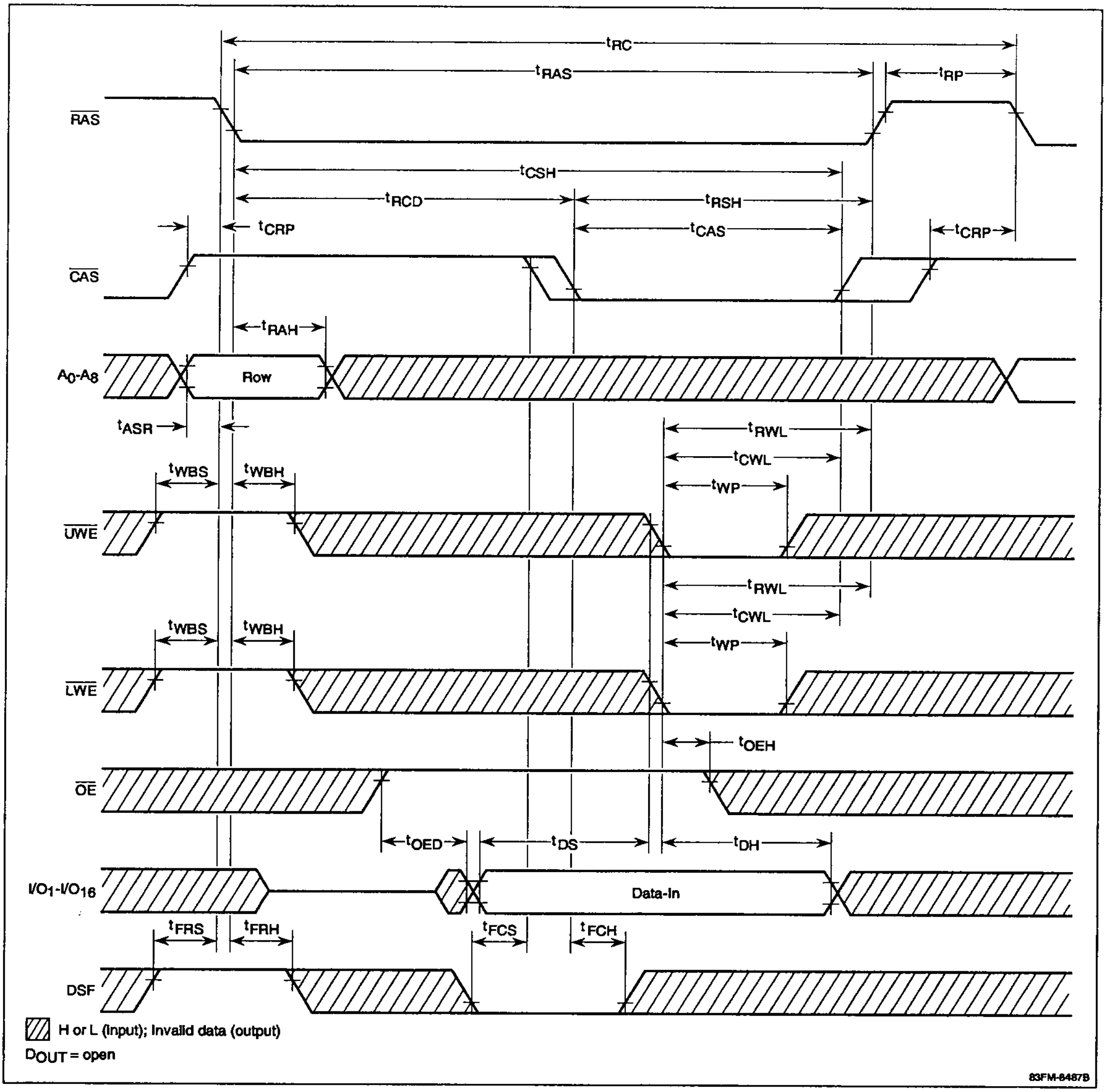
## Timing Waveforms (cont)

### *Load Old Mask Register Cycle (Upper-byte, early-write)*



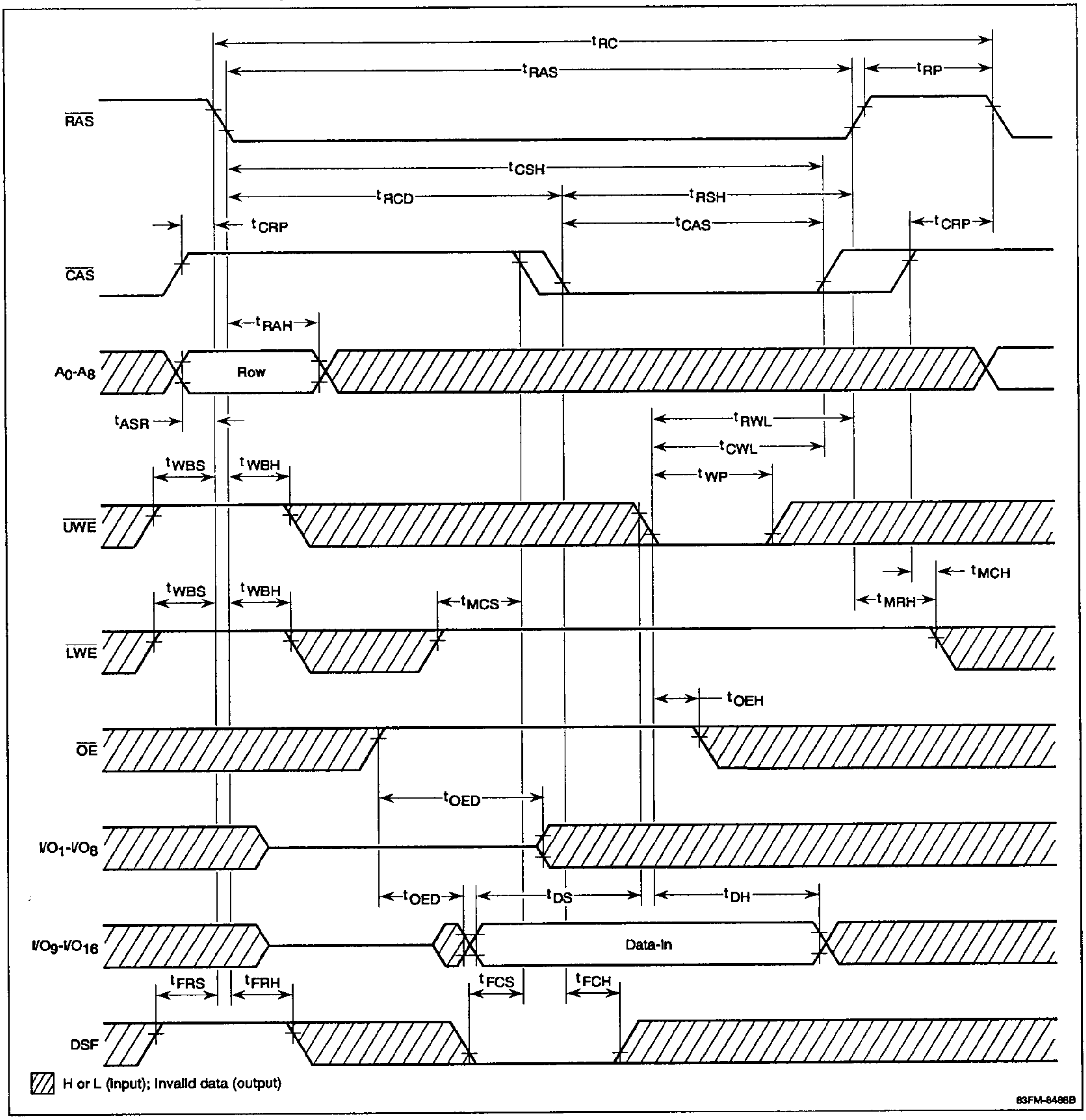
## Timing Waveforms (cont)

### *Load Old Mask Register Cycle (Late-write)*



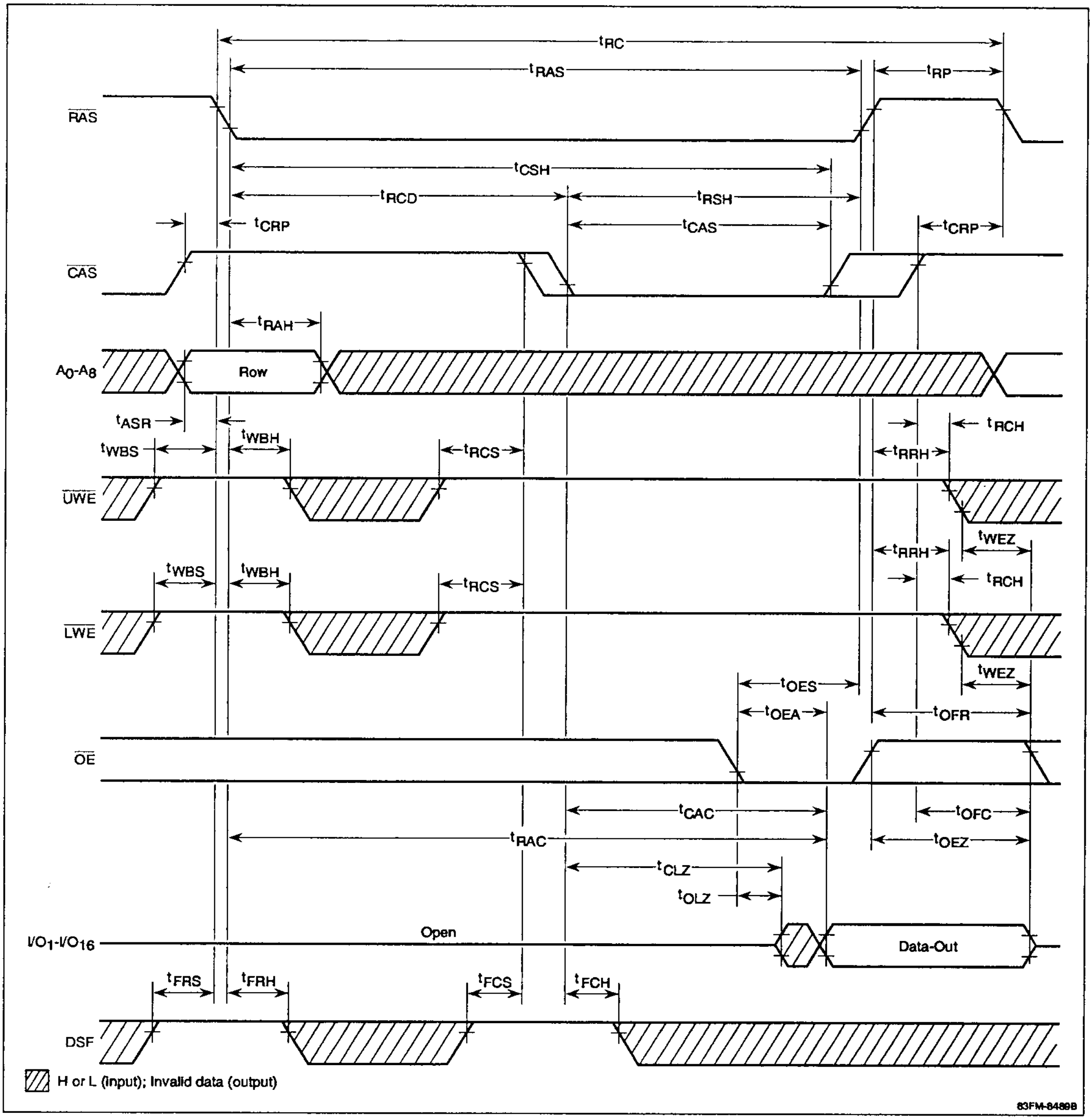
## Timing Waveforms (cont)

### *Load Old Mask Register Cycle (Upper-byte, late-write)*



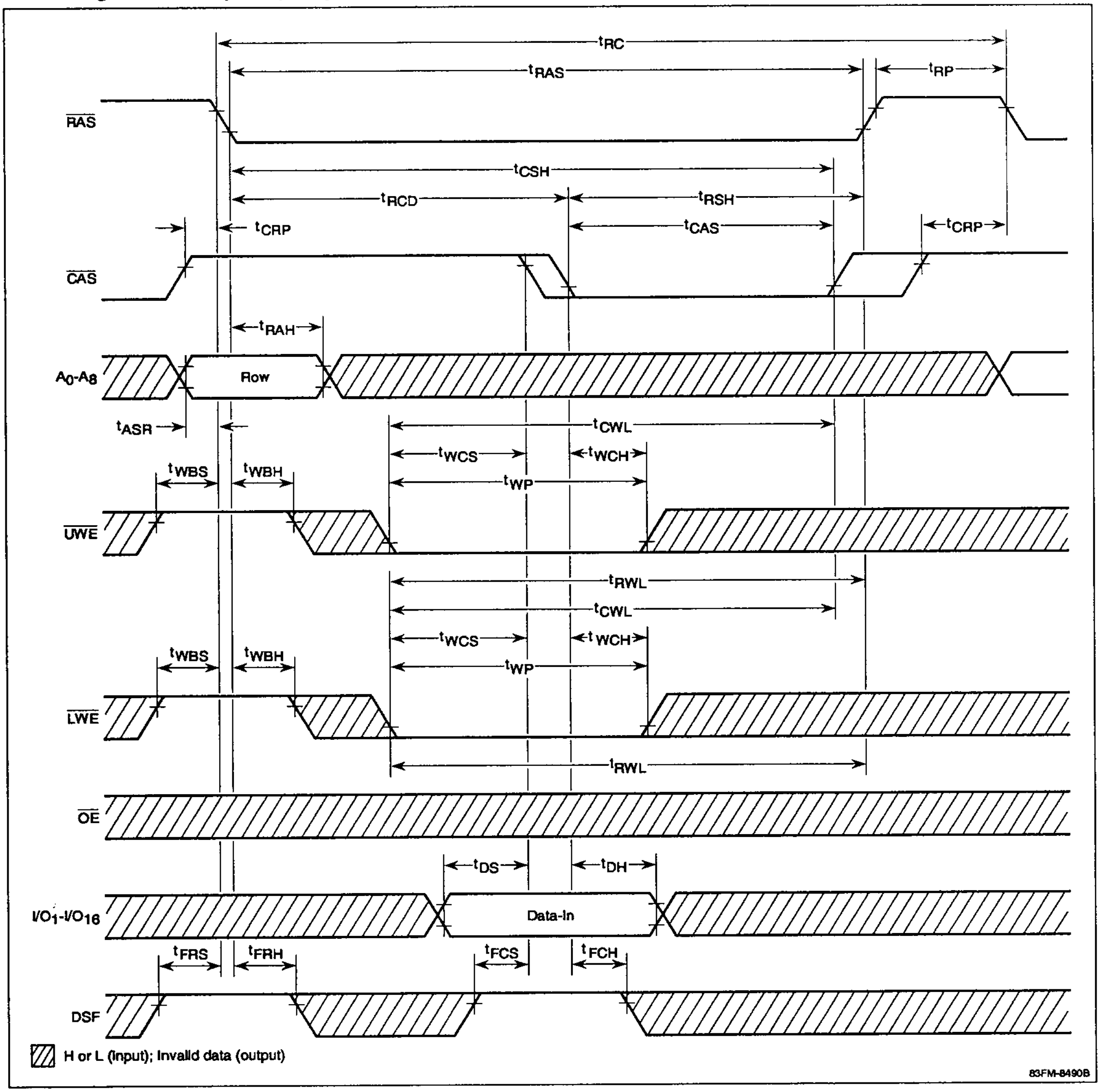
## Timing Waveforms (cont)

### *Color Register Set Cycle (Read with extended output)*



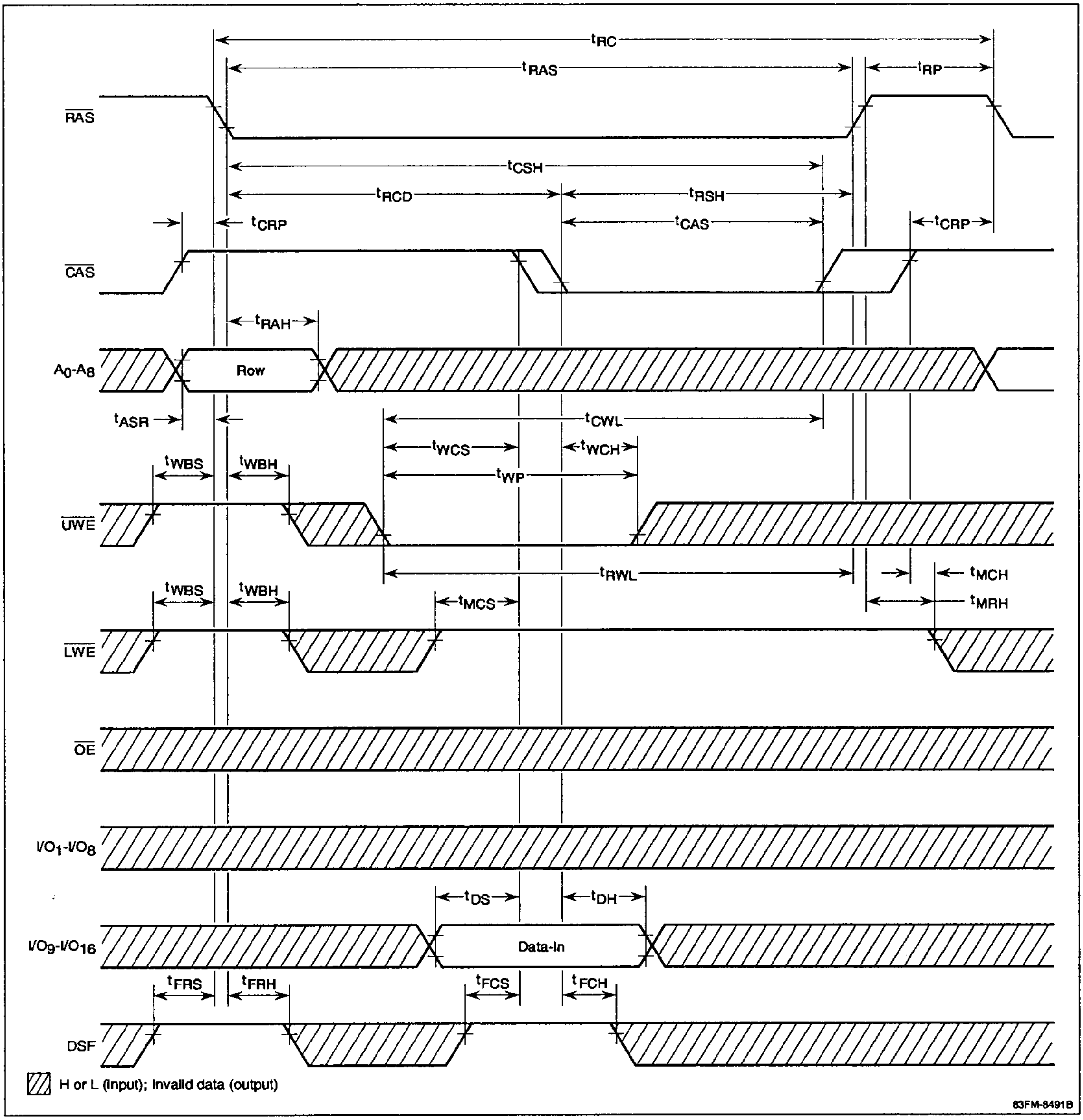
## Timing Waveforms (cont)

### *Color Register Set Cycle (Early-write)*



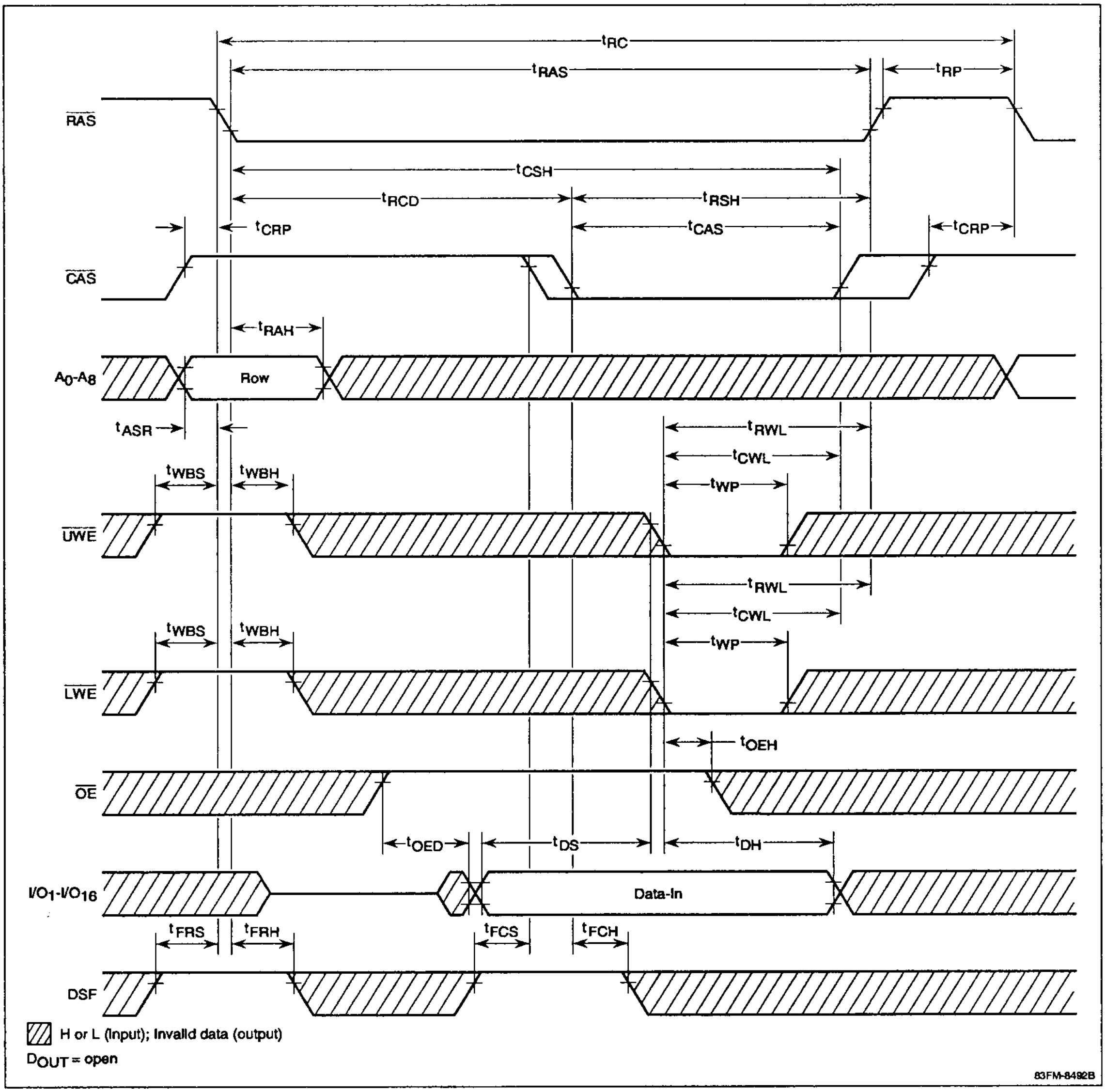
## Timing Waveforms (cont)

### *Color Register Set Cycle (Upper-byte, early-write)*



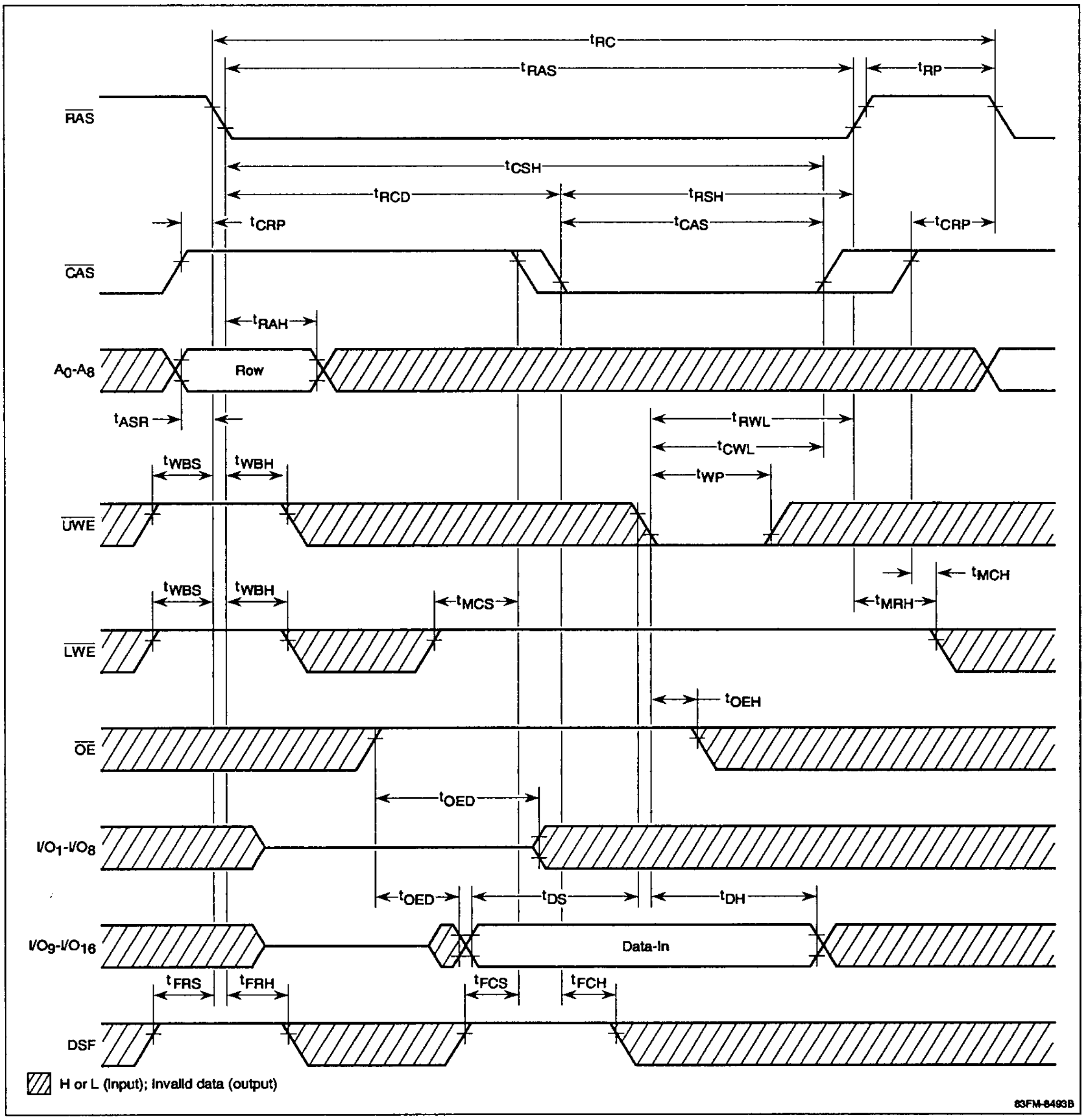
## Timing Waveforms (cont)

### *Color Register Set Cycle (Late-write)*



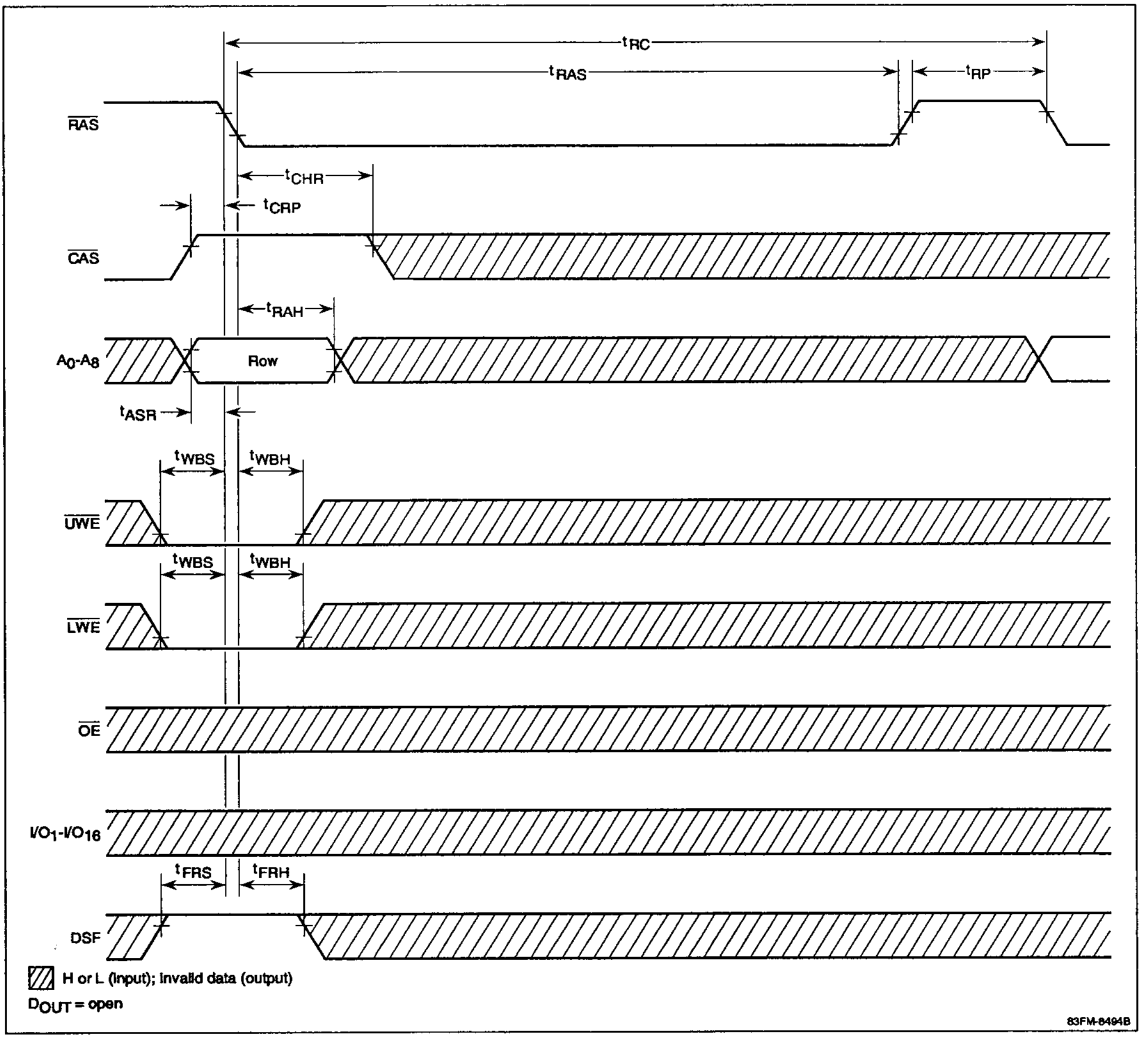
## Timing Waveforms (cont)

### *Color Register Set Cycle (Upper-byte, late-write)*



## Timing Waveforms (cont)

### *Flash-Write Cycle*



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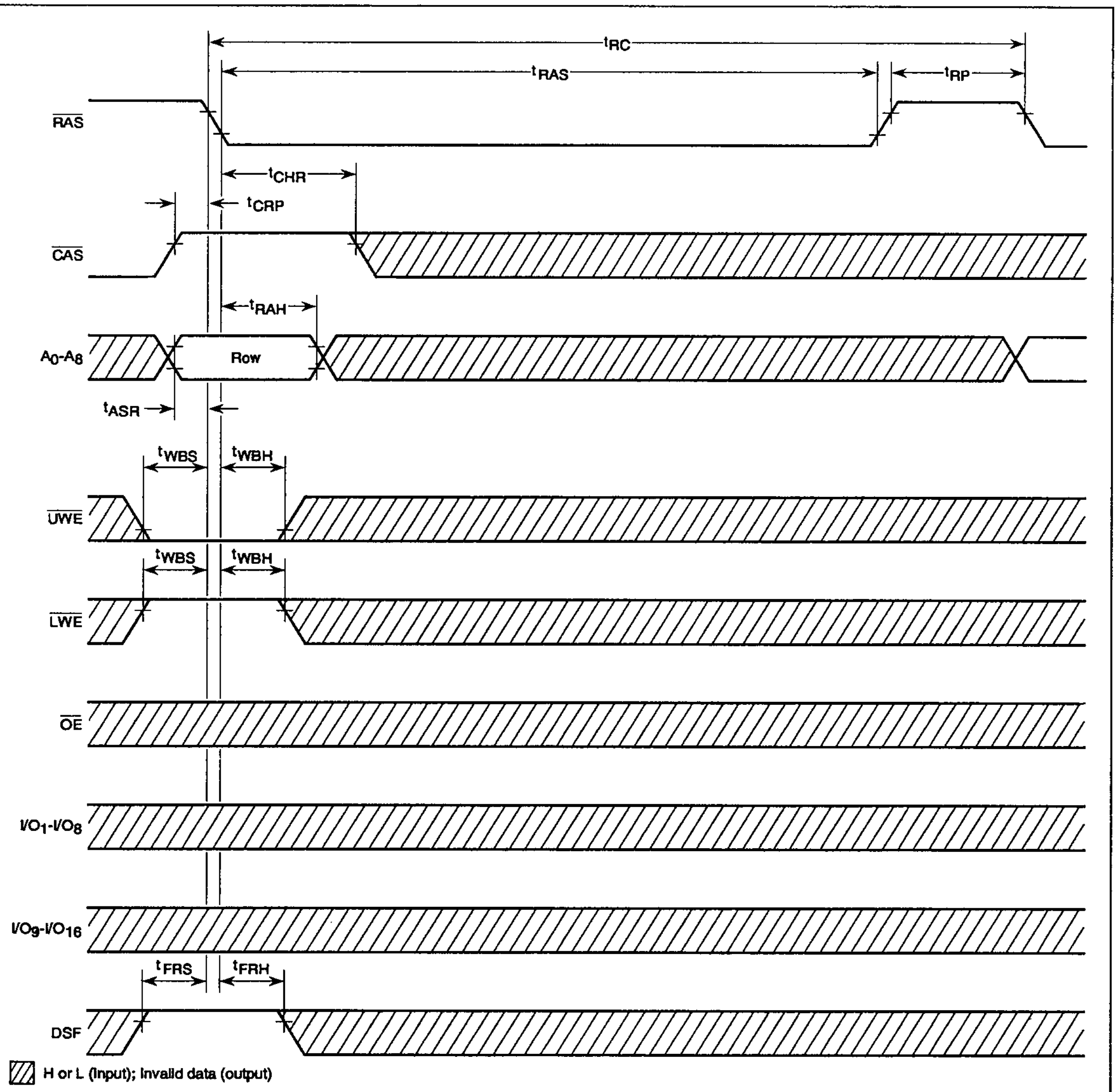
## Timing Waveforms (cont)

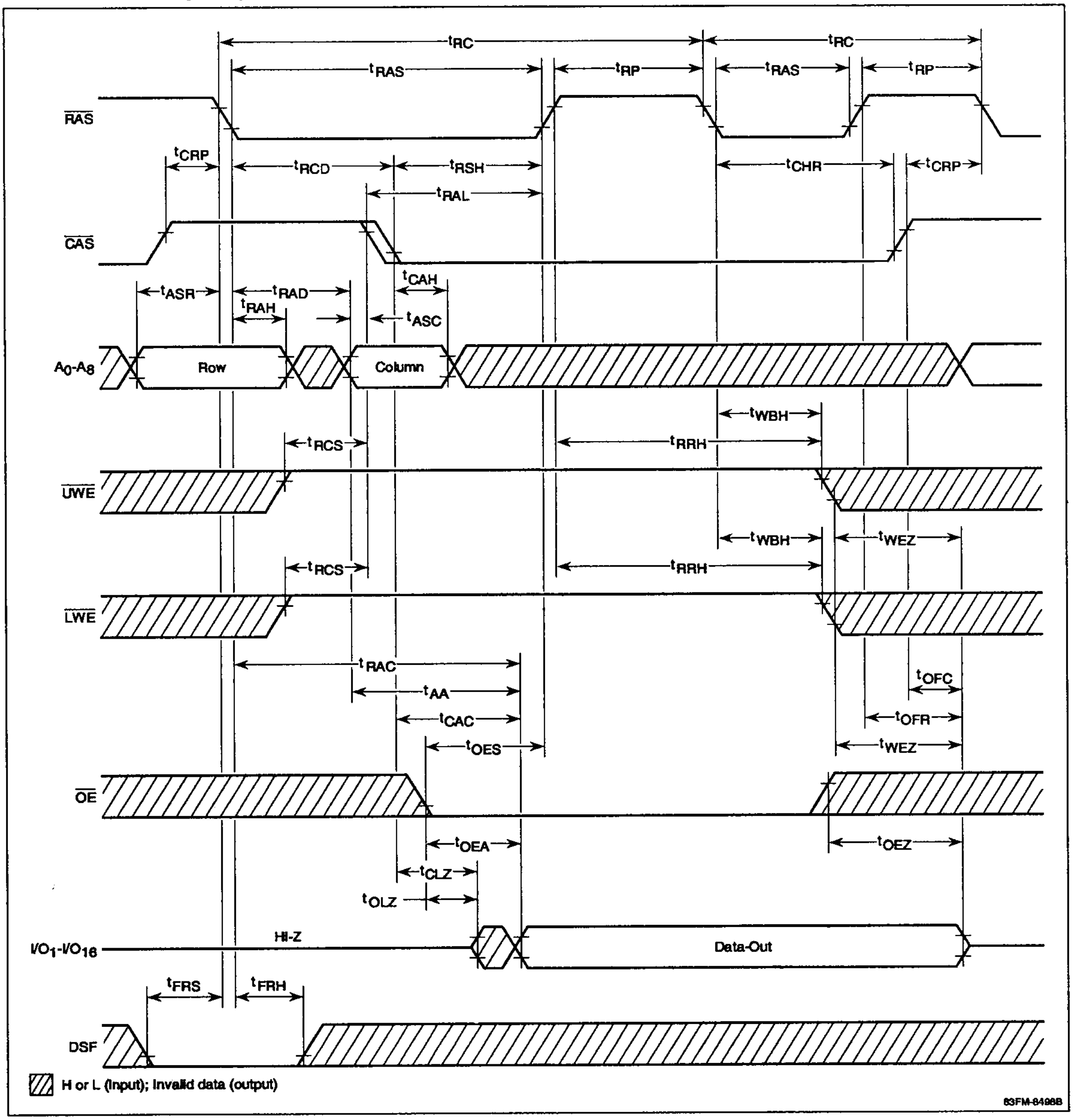
### *Flash-Write Cycle (Upper-byte, flash-write)*




**Note:** The lower-byte color register data is not written even if $\overline{CAS}$ and $\overline{LWE}$ go active later in the cycle.

## Timing Waveforms (cont)

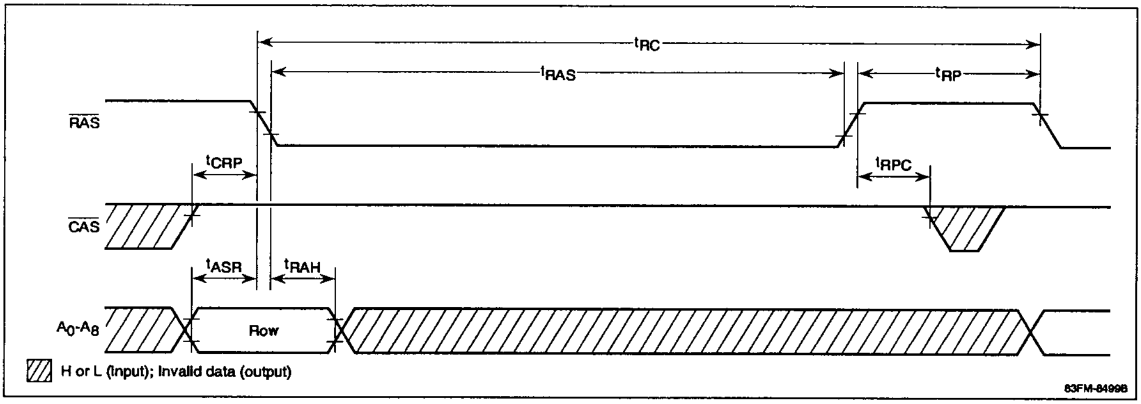
### *Hidden Refresh Cycle (With exended output)*



18m

## Timing Waveforms (cont)

### RAS-Only Refresh Cycle




### CAS Before RAS Refresh Cycle