# DAC-04/DAC-06

## TWO'S COMPLEMENT 10-BIT D/A CONVERTER

### FEATURES

- **Complete** ..... **Includes Reference and Op Amp**
- **Compact** ..... **Single 18-Pin DIP Package**
- **Bipolar Output** ..... **Two's Complement Coding**
- **Monotonicity Guaranteed**
- **Nonlinearity** ..... **±1 LSB**
- **Fast** ..... **1.5μs Settling Time**
- **Low Power Consumption** ..... **300mW Maximum**
- **TTL, CMOS Compatible Inputs**
- **125°C Tested Dice Available**

### GENERAL DESCRIPTION

The DAC-04 and DAC-06 are complete 10-Bit Two's Complement D/A Converters on a single 90 x 163 mil monolithic chip. All elements of a complete bipolar output Two's Complement DAC are included — precision voltage reference, current steering logic, current sources, R-2R resistor network, bipolar offset circuit and high speed internally compensated output op amp. Monotonicity guaranteed over the entire 0°C to +70°C temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The user may also easily implement One's Complement, Straight Offset Binary, or unipolar operation. The ±12V to ±18V power supply range, low power consumption, TTL and CMOS compatibility, wide logic input compatibility, and adaptable logic coding capability assure utility in a wide range of applications.

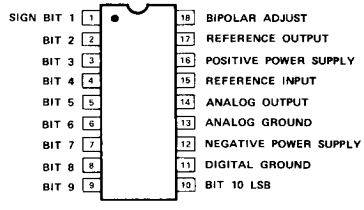
### ORDERING INFORMATION†

| PACKAGE 18 PIN HERMETIC DIP | | | |
|---|---|---|---|
| MONOTONICITY | MILITARY TEMP* | COMMERCIAL TEMP | |
| 10 | | DAC-06EX | |
| 9 | DAC-06BX | DAC-04BCX | DAC-06FX |
| 8 | DAC-06CX | DAC-04CCX | DAC-06GX |
| 7 | | DAC-04DDX | |

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

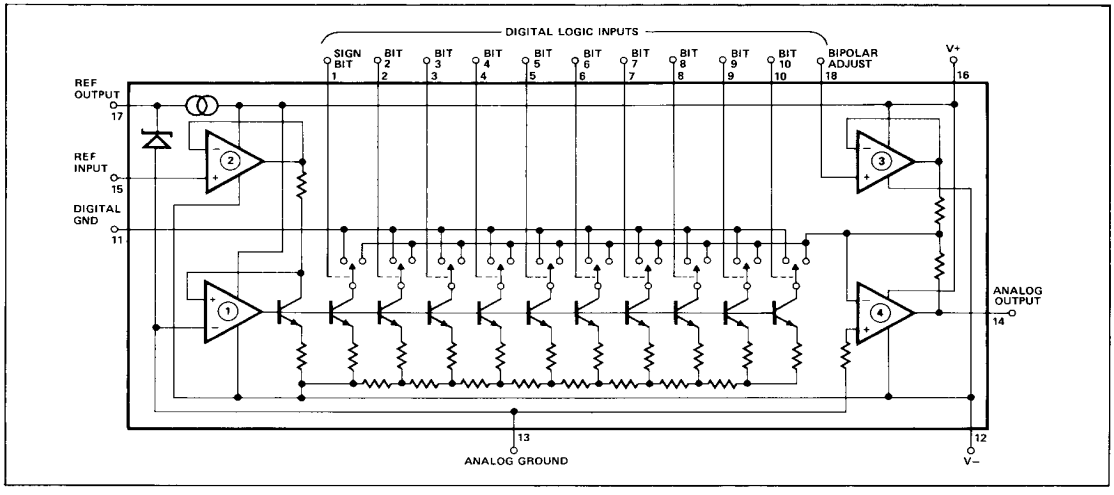
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

### PIN CONNECTIONS




18-PIN DIP (X-Suffix)

### SIMPLIFIED SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS (Note)

Operating Temperature Range
- DAC-06B,C ..... −55°C to +125°C
- DAC-04B,C,D, DAC-06E,F,G ..... 0°C to +70°C

DICE Junction Temperature ($T_j$) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
V+ Supply to Analog Ground ..... 0 to +18V
V− Supply to Analog Ground ..... 0 to −18V
Analog Ground to Digital Ground ..... 0 to ±0.5V
Logic Inputs to Digital Ground ..... −5V to (V+ −0.7)V
Internal Reference Output Current ..... 300μA
Reference Input Voltage ..... 0 to +10V
Bipolar Offset Input Voltage ..... 0 to +10V
Internal Power Dissipation ..... 500mW
Lead Soldering Temperature (60 sec) ..... 300°C
Output Short Circuit Duration ..... Indefinite
(Short circuit may be to ground or either supply)

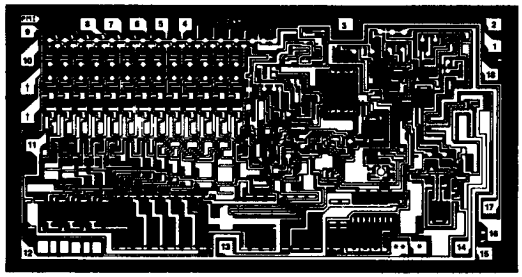
**NOTE:** Ratings apply to both DICE and packaged devices unless otherwise noted.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $-55°C \le T_A \le +125°C$ for DAC-06B & C; and $0°C \le T_A \le +70°C$ for DAC-04B, C & D and DAC-06E, F & G, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | | DAC-04 | DAC-06 | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Resolution | | | | All | All | 10 | — | 10 | Bits |
| | | | | | E | 10 | — | — | Bits |
| Monotonicity | | | | BC | B/F | 9 | — | — | Bits |
| | | | | CC | C/G | 8 | — | — | Bits |
| | | | | DD | | 7 | — | — | Bits |
| | | | | | E | ±0.1 | — | — | % FS |
| | | $T_A = 25°C$ | | | B/F | ±0.2 | — | — | % FS |
| | | | | | C/G | ±0.4 | — | — | % FS |
| | | | | BC | | ±0.1 | — | — | % FS |
| Nonlinearity | NL | | | CC | E | ±0.2 | — | — | % FS |
| | | $T_A$ = Full Temp | | | B/F | ±0.3 | — | — | % FS |
| | | | | DD | | ±0.4 | — | — | % FS |
| | | | | | C/G | ±0.5 | — | — | % FS |
| | | | | BC/CC | B | — | ±45 | ±90 | ppm/°C |
| | | Total Internal | | | E/F/G | — | ±45 | ±100 | ppm/°C |
| | | Ref Connected | | | C | — | ±60 | ±120 | ppm/°C |
| Full Scale Tempco | $TC_{V_{FS}}$ | | | DD | | — | ±60 | ±150 | ppm/°C |
| | | Zero Drift Ext | | BC/CC | All | — | ±30 | — | ppm/°C |
| | | Ref Applied. | | DD | | — | ±50 | — | ppm/°C |
| | | | | BC/CC | All | — | 1.5 | — | μs |
| Settling Time | $T_S$ | To ±1/2 LSB, 10V Step | | DD | | — | 2.5 | — | μs |
| | | Short Pin 18 to | $T_A = 25°C$ | | All | — | ±1 | ±5 | mV |
| Unipolar Zero Scale Output | $V_{ZS}$ | Ground (Note 1) | $T_A$ = Full Temp | | All | — | ±2 | ±10 | mV |
| | | | | All | | — | ±5 | — | mV |
| Bipolar Offset Voltage | BP Off | Connect Pins 15, 17 & 18 (Note 2) | | All | All | -5.0 | — | +2.5 | % Range |
| Full Range Output Voltage | $V_{FR}$ | Connect Pin 15 to 17 (Note 2) $R_L = 2k\Omega$ | | All | All | 10 | — | 11.5 | V |
| Reference Input Bias Current | $I_B$ | | | All | All | — | 100 | — | nA |
| Reference Input Impedance | $Z_{IN}$ | | | All | All | — | 200 | — | MΩ |
| Reference Input Slew Rate | SR | | | All | All | — | 1.5 | — | V/μs |
| Reference Output Voltage | $V_{REF}$ | | | All | All | — | 6.7 | — | V |
| | | Each Input | | All | | — | 1.0 | — | μA |
| Logic Input Current | $I_{IN}$ | −5V to (V+ −0.7)V | | | All | — | 1 | 10 | μA |
| Logic Input "0" | $V_{INL}$ | | | All | All | — | — | 0.8 | V |
| Logic Input "1" | $V_{INH}$ | | | All | All | 2.0 | — | — | V |
| | | | $T_A = 25°C$ | | All | — | ±0.02 | ±0.05 | % FS/V |
| | | | | BC/CC | | — | ±0.015 | ±0.1 | % FS/V |
| Power Supply Sensitivity | $P_{SS}$ | $V_S = \pm 12$ to $\pm 18V$ | $T_A$ = Full Temp | | All | — | ±0.02 | ±0.1 | % FS/V |
| | | | | DD | | — | ±0.015 | — | % FS/V |
| | | | | BC/CC | All | — | 7 | 10 | mA |
| | I+ | $T_A = 25°C$ | | DD | | — | 7 | 11.6 | mA |
| Supply Current | | | | BC,CC | All | — | −9 | −10 | mA |
| | I− | $T_A = 25°C$ | | DD | | — | −9 | −11.6 | mA |
| | | | | BC,CC | All | — | 250 | 300 | mW |
| Power Dissipation | $P_D$ | | $T_A = 25°C$ | DD | | — | 250 | 350 | mW |
| | | | $T_A$ = Full Temp | | All | — | — | 350 | mW |

**NOTES:**
1. May be operated in the 0 to +10V unipolar mode by shorting Pin 18 to Ground.
2. $V_{FR} = |V_{FR}+| + |V_{FR}-|$ and is trimmable to exactly 10V range with the circuit shown in typical applications.
3. Bipolar offset voltage is trimmable to exact two's or one's complement condition with the circuit shown in typical applications.

## DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



**DIE SIZE 0.163 × 0.090 inch**

**Refer to Section 2 for additional DICE information.**

1. BIT 1 MSB (SIGN BIT)
2. BIT 2
3. BIT 3
4. BIT 4
5. BIT 5
6. BIT 6
7. BIT 7
8. BIT 8
9. BIT 9
10. BIT 10 LSB
11. DIGITAL GROUND
12. V–
13. ANALOG GROUND
14. ANALOG OUTPUT
15. REF IN
16. V+
17. REF OUT
18. BIPOLAR ADJUST

**NOTE:**
Voltage Output Range programmable by connecting *(10V) to Analog Output for 10 volt range. Jumper from **(5V) to Analog Output sets device to 5 volt range.
† Two additional least significant bits are provided.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 125°C$ for DAC-04NT, GT and $T_A = 25°C$ for DAC-04N, G, GR, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC-04NT LIMIT | DAC-04N LIMIT | DAC-04GT LIMIT | DAC-04G LIMIT | DAC-04GR LIMIT | UNITS |
|---|---|---|---|---|---|---|---|
| Resolution | Bipolar Output | 12 | 12 | 12 | 12 | 12 | Bits Min |
| Monotonicity | | 10 | 9 | 9 | 8 | 7 | Bits Min |
| Nonlinearity | | ±0.2 | ±0.2 | ±0.4 | ±0.2 | ±0.4 | % FS Min |
| Bipolar Offset Voltage | Short Ref Input to Reference | +2.5 | +2.5 | +2.5 | +2.5 | +2.5 | V MAX |
| | Output and Bipolar Adjust | −5.0 | −5.0 | −5.0 | −5.0 | −5.0 | V Min |
| Power Supply Rejection | $V_S = \pm 12V$ to $\pm 18V$ | 0.1 | 0.1 | 0.1 | 0.1 | 0.15 | $\%V_{FS}$ Max |
| Power Dissipation | $I_{OUT} = 0$ | 350 | 300 | 350 | 300 | 350 | mW Max |
| Logic Input "0" | | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | V Max |
| Logic Input "1" | | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | V Min |
| Analog Output Voltage | Short Reference Input | 11.5 | 11.5 | 11.5 | 11.5 | 11.5 | V Max |
| | to Reference Output | 10.0 | 10.0 | 10.0 | 10.0 | 10.0 | V Min |

**NOTE:** For 25° C characteristics of DAC-04NT & GT, see DAC-04N & G characteristics respectively.

## TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and ±5V Full Scale Output, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | DAC-04NT TYP | DAC-04N TYP | DAC-04GT TYP | DAC-04G TYP | DAC-04GR TYP | UNITS |
|---|---|---|---|---|---|---|---|---|
| Full Scale Tempco | $TCV_{FS}$ | Internal Reference | ±60 | ±60 | ±60 | ±60 | ±90 | ppm/°C |
| Settling Time ($T_A = 25°C$) | $t_S$ | To ± 1/2 LSB 10 Volt Step | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | µs |
| Logic Input Current | | $T_A = 25°C$ | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | nA |

## TYPICAL APPLICATIONS

### ADJUSTNG FOR TWO'S COMPLEMENT CODING

1. Connect Full Scale Adjust and Bipolar Adjust Circuitry as shown in figure.
2. Turn all bits OFF ($V_{FS-}$) = 1000000000
3. Adjust Bipolar Pot for $V_{FS}$ at output ..... −5.000V
4. Turn all bits ON ($V_{FR+}$) − 0111111111
5. Adjust Full Scale Pot for desired $V_{FR+}$ value ..... +4.990V
6. Check Zero Scale Reading ($V_{ZS}$) − 0000000000 If this reading is outside desired $V_{ZS}$ range, readjust Bipolar Pot until the output reads 0.0000V.

### TWO'S COMPLEMENT CODING TABLE

| | INPUT MSB | | | | | | | | | LSB | IDEAL OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{FS+}$ −1LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +4.990V |
| $V_{FS+}$ −2LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | +4.980V |
| +1LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +0.010V |
| Zero | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000V |
| −1LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | −0.010V |
| $V_{FS-}$ +LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | −4.990V |
| $V_{FS-}$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | −5.000V |

### ADJUSTING FOR ONE'S COMPLEMENT CODING

1. Connect Full Scale Adjust and Bipolar Adjust Circuitry as shown in above figure.
2. Turn all bits OFF ($V_{FR-}$) − 1000000000
3. Adjust Bipolar Pot for $V_{FR-}$ at output ..... −5.0000V
4. Turn all bits ON ($V_{FR+}$) − 0111111111
5. Adjust Full Scale Pot for desired $V_{FR+}$ value ..... +5.0000V

### ONE'S COMPLEMENT CODING TABLE

| | INPUT MSB | | | | | | | | | LSB | IDEAL OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{FS+}$ −1LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +5.000V |
| $V_{FS+}$ −2LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | +4.990V |
| +0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +0.005V |
| −0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | −0.005V |
| $V_{FS-}$ +2LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | −4.990V |
| $V_{FS-}$ +1LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | −5.000V |

Note that two zero states will straddle (±1/2 LSB) the true zero. Therefore the DAC will give symmetrical outputs for both positive and negative full scale.

### REFERENCE OUTPUT

For best results, Reference Output current should not exceed 100μA.

### POWER SUPPLIES

The DAC-04 and DAC-06 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor. Chip users should connect the substrate to V−.

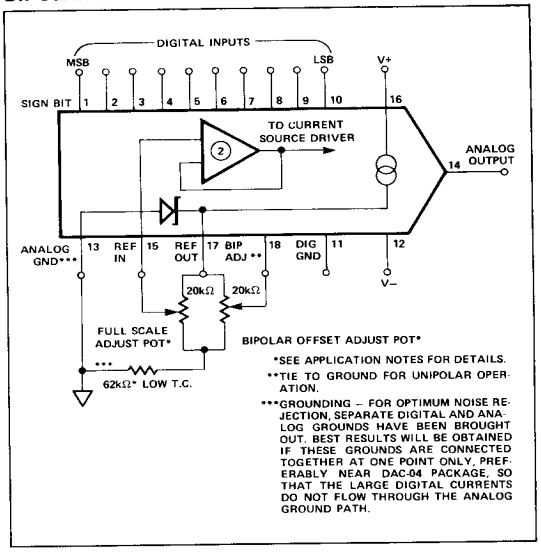
### GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the DAC-04 and DAC-06 package, so that large degital currents do not flow through the analog ground path.

### CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF.

### FULL SCALE OUTPUT RANGE AND BIPOLAR OFFSET ADJUSTMENT CIRCUIT




### EXTERNAL ADJUSTMENT NETWORK

Full Scale Output Range and Bipolar Offset may be adjusted by using the circuit shown in the figure above. Best results will be obtained when low tempco pots and resistors are used, or if pot and resistor tempcos match.

## TYPICAL APPLICATIONS

### IMPLEMENTING

Offset Binary coding is exactly the same as Two's Complement coding except that the most significant bit occurs in true, rather than inverted form and the output states are relabeled. To convert the DAC-04 and DAC-06 to Offset Binary code operation, simply place a logic inverter in series with the MSB input (Pin 1) and invert the MSB value shown in steps 2, 4 and 6 of the Two's Complement adjustment procedure shown above.

### OFFSET BINARY CODING TABLE

| | INPUT | | | | | | | | | | IDEAL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | MSB | | | | | | | | | LSB | OUTPUT |
| $V_{FS+}$ −1LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +4.990V |
| $V_{FS+}$ −2LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | +4.980V |
| ZERO | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.00 |
| ZERO 1LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | −0.005V |
| $V_{FS-}$ +1LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | −4.990V |
| $V_{FS-}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | −5.000V |

### INTERFACING WITH CMOS LOGIC

The DAC-04 and DAC-06 logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

In this special case, a diode should be placed in series with the CMOS driving device's $V_{DD}$ lead as shown in Figure 1. The diode limits $V_D$ to V+ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-06 requires either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

### CMOS LOGIC INTERFACE CIRCUIT