DAC-08B
High Speed, 8-Bit Monolithic Digital-to-Analog Converter

FEATURES

- **85 Nanoseconds settling time**
- **−10 to +18V compliance**
- **±4.5 to ±18V supply**
- **8-Bit resolution**
- **1- or 2-Quadrant multiplication**
- **Low cost**

GENERAL DESCRIPTION

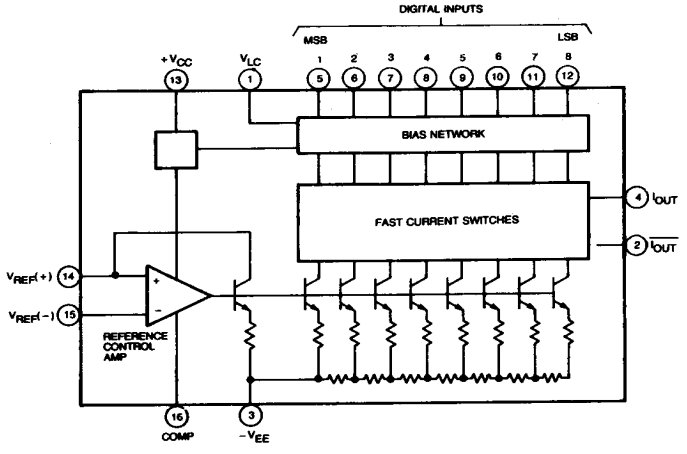
The DAC-08BC and DAC-08BM provide very high speed performance coupled with low cost and application flexibility. These units have guaranteed full 8-bit monotonicity with nonlinearity of 0.19% over the full operating temperature range. High-speed current steering switches achieve 85 nanoseconds settling time with a very low glitch for full-scale changes. A large output voltage compliance range (−10 to +18V) allows direct current to voltage conversion with just an output resistor, omitting the need for an operational amplifier in many cases.

The DAC-08 consists of 8 fast-switching current sources, a diffused R-2R resistor ladder, a bias circuit, and a reference control amplifier. The diffused resistor ladder gives excellent temperature tracking, resulting in a gain temperature coefficient of 10 ppm/°C. The monolithic fabrication results in excellent linearity and tempco, fast output settling and low cost. Linearity is ±½ LSB.

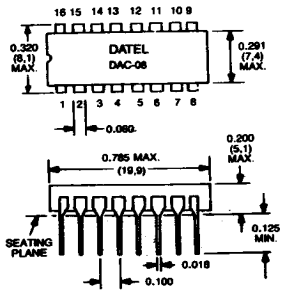
An external reference current of 2 mA nominal programs the scale factor of the DAC. This reference current can also be varied, resulting in one or two quadrant multiplying operation. The output voltage can be unipolar or bipolar dependent upon the connection of the two complementary output sink currents.

DAC-08 applications include fast A/D converters, waveform generators, audio encoder and attenuators; CRT display drivers, and high-speed modems.

Power supply requirements are ±4.5V to ±18V. Operating temperature range is 0°C to 70°C for the DAC-08BC and −55°C to +125°C for the DAC-08BM. These models have equivalent specifications and pinouts to industry standard DAC-08's.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	THRESHOLD CONTROL (VLC)
2	$\overline{I_{OUT}}$
3	VEE
4	IOUT
5	BIT 1 IN (MSB)
6	BIT 2 IN
7	BIT 3 IN
8	BIT 4 IN
9	BIT 5 IN
10	BIT 6 IN
11	BIT 7 IN
12	BIT 8 IN (MSB)
13	VCC
14	VREF+
15	VREF−
16	COMPENSTION

ABSOLUTE MAXIMUM RATINGS	
V_{CC} Supply to V_{EE} Supply	36V
Digital Input Voltage	$-V_{EE}$ to $-V_{EE}$ plus 36V
V_{LC}	$-V_{EE}$ to $+V_{CC}$
Reference Input Voltage	$-V_{EE}$ to $+V_{CC}$
Reference Input Current	5.0 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, $V_S = \pm 15V$, $I_{REF} = 2.0$ mA unless otherwise noted.

INPUTS	
Resolution	8 Bits
Coding, Unipolar Output	Straight Binary
Coding, Bipolar Output	Offset Binary
Input Logic Level, Bit ON ("1")	+2.0V minimum at +10.0 μA
Input Logic Level, Bit OFF("0")	+0.8V maximum at −10.0 μA[1]
Nominal Reference Current	2.0 mA
Reference Bias Current	−1.0 μA
Reference Input Slew Rate	8 mA/μsec.
OUTPUTS	
Output Current, $I_{REF} = 2.0$ mA	1.99 mA ±0.05 mA[2]
Output Current Range, $V_{EE} = -5V$	0 to 2.1 mA
Output Current Range, $V_{EE} = -7$ to −18V	0 to 4.2 mA
Output Current, all bits OFF	±0.2 μA typical ±2.0 μA maximum
Full-Scale Symmetry	±1.0 μA typical ±8.0 μA maximum
Output Voltage Compliance	−10 to +18V
PERFORMANCE	
Relative Accuracy	±½ LSB (±0.19%) maximum
Nonlinearity	±½ LSB (±0.19%) maximum
Differential Nonlinearity	±½ LSB (±0.19%)
Full-Scale Tempco	±10 ppm/°C typical ±50 ppm/°C maximum
Settling Time, 2 mA to ½ LSB	85 nsec. typical 150 nsec. maximum
Propagation Delay	60 nsec. maximum
Power Supply Sensitivity, $I_{REF} = 1$ mA	±0.002%/%
POWER REQUIREMENTS	
V_{CC}	+4.5V to +18V
V_{EE}	−4.5V to −18V
Power Supply Current, $I_{REF} = 1.0$ mA V = ±5V	+3.8, −5.8 mA maximum
Power Supply Current, $I_{REF} = 2.0$ mA V = +5V, −15V	+3.8, −7.8 mA maximum
V = ±15V	+3.8, −7.8 mA maximum
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
DAC-08BC	0°C to +70°C
DAC-08BM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package	16 Pin Dip

FOOTNOTES

1. For TTL, DTL Interface, V_{LC} = 0V. For other digital interfaces see TECHNICAL NOTE 3.
2. I_{OUT} (Pin 4) + I_{OUT} (Pin 2) = Output Current

TECHNICAL NOTES

1. The DAC-08 series is a multiplying D/A converter in which the output current is a product of the digital word and the input reference current. Excellent performance is obtained for I_{REF} from 4.0 mA to 4.0 μA. Monotonic operation is maintained from 4.0 mA to 100 μA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \quad (I_{REF} \text{ is current at Pin 14})$$

2. **Reference Amplifier Set-up.** If a regulated power supply is used as the reference, a resistor divider should be used with the junction by-passed to ground with a 0.1 μf capacitor. TTL logic supplies are not recommended to be used as the reference. AC and dc reference applications will require the reference amplifier to be compensated using a capacitor (C_C) from pin 16 to V_{EE}. For fixed reference application (dc), a 0.01 μF capacitor is recommended. For AC reference applications, the value of C_C depends on the impedance present at pin 14. For R_{REF} values of 1.0, 2.5 and 5.0 KΩ, minimum values of C_C are 15, 37 and 75 pf respectively. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin. See Graph on Reference Input Frequency Response. Low R_{REF} values enable small C_C achieving highest throughput on V_{REF}. If pin 14 is driven by a high impedance such as a transistor current source, the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{REF} = 1.0 KΩ and C_C = 15 pf, the reference amplifier slews at 4.0 mA/microsecond, enabling a transition from I_{REF} = 0 to I_{REF} = 2.0 mA in 500 nanoseconds.
3. **Interfacing Various Logic Families.** The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. A large input swing capability allows adjustable logic threshold voltage and 200 μA maximum source current on pin 1. Mimimum input logic swing and minimum logic threshold voltage is given by V_{EE} + (I_{REF} x 1.0 KΩ) + 2.5V. Logic threshold is adjusted by appropriate voltage at V_{LC}. The Interfacing Various Logic Families Diagram shows appropriate connections. Fastest settling times are obtained when V_{LC} sees a low impedance. Use 0.01 μF by-pass capacitors whenever possible.
4. **Analog Output Currents.** Both true and complemented output sink currents are provided, $I_O + \overline{I_O} = I_{FS}$. Both outputs can be used simultaneously. If one of the outputs is not required, it must be connected to ground or a point capable of sourcing I_{FS}. **Do not leave unused output pin (I_O or $\overline{I_O}$) open.** The compliance voltage is the voltage swing on output pin without affecting DAC accuracy. Positive compliance is 36V above V_{EE} and is independent of V+. Negative compliance is V_{EE} + (I_{REF} x 1 KΩ) +2.5V.
5. **Settling Time.** The DAC-08 is capable of extremely fast settling times, typically 85 nanoseconds at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance. The output capacitance of the DAC including the package is approximately 15 pf, therefore the output RC time constant dominates at $R_L > 500\ \Omega$.

   Settling time remains essentially constant for I_{REF} values down to 1.0 mA, with gradual increases for lower I_{REF} values. The switching transients (glitches) are very low and may be further reduced by small capacitive loads at the output. Settling time will be increased slightly.

TECHNICAL NOTES (Cont'd)

6. **Power Supplies.** The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. For example, operation at −4.5V with $I_{REF} = 2$ mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network. It is recommended that V_{CC} and V_{EE} always be bypassed to ground with at least 0.1 μf capacitors.

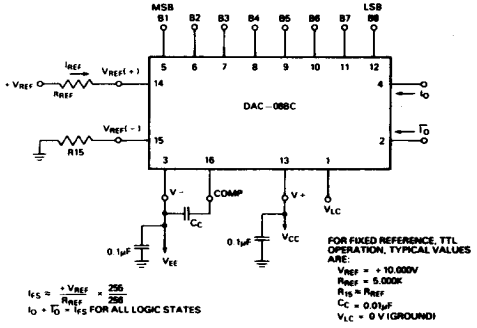
   Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible, as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

   Power consumption may be calculated as follows:
   $P_d = (I+)(V+) + (I-)(V-) + (2\ I_{REF})(V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

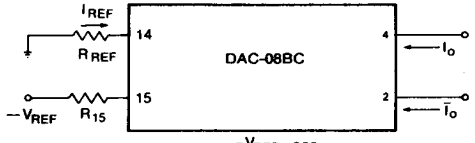
7. **Temperature Performance.** For most applications, a +10.0V reference is recommended for optimum full scale temperature coefficient performance. Full scale trimming may be accomplished by adjusting I_{REF} (changing value of R_{REF}). R_{REF} and R_L should be selected for similar temperature coefficient to minimize accuracy error. Setting time of the DAC decreases approximately 10% at −55°C and increases 15% at +125°C.

APPLICATION DIAGRAMS

BASIC POSITIVE REFERENCE OPERATION



BASIC NEGATIVE REFERENCE OPERATION

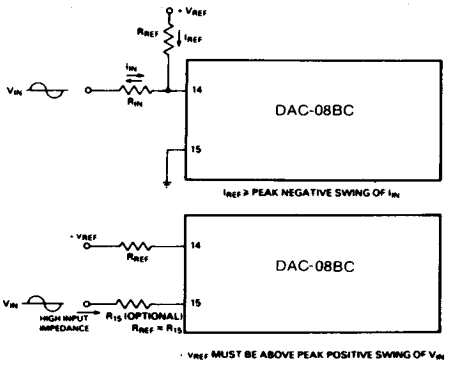


$$I_{FS} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

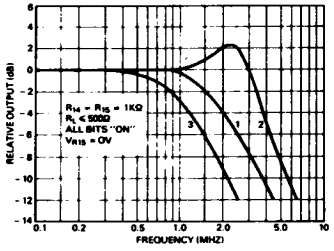
$(R_{15} = R_{REF})$

APPLICATION DIAGRAMS (Cont'd)

ACCOMMODATING BIPOLAR REFERENCES

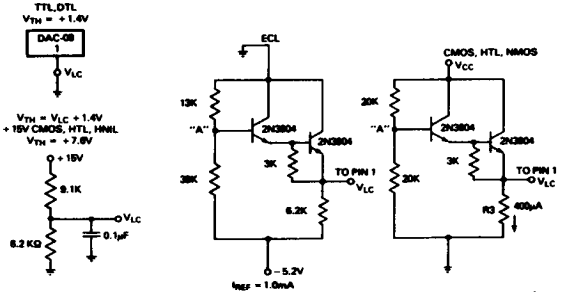


REFERENCE INPUT FREQUENCY RESPONSE

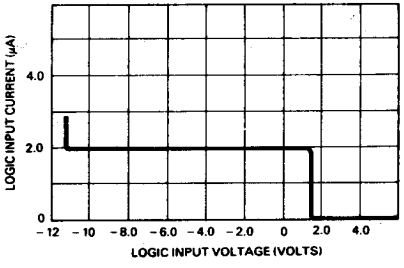


CURVE 1: C_C = 15pF, V_{IN} = 2.0V_{p-p} CENTERED AT +1.0V.
CURVE 2: C_C = 15pF, V_{IN} = 50mV_{p-p} CENTERED AT +200mV.
CURVE 3: C_C = 0pF, V_{IN} = 100mV_{p-p} CENTERED AT 0V AND APPLIED THRU 50Ω CONNECTED TO PIN 14. +2.0V APPLIED TO R_{14}.

INTERFACING VARIOUS LOGIC FAMILIES

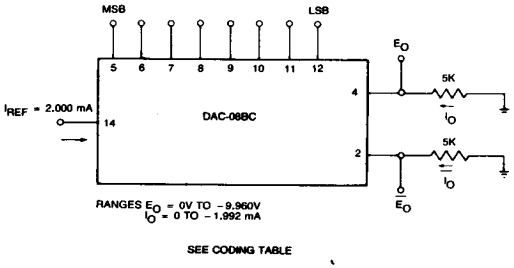


LOGIC INPUT CURRENT VS. INPUT VOLTAGE

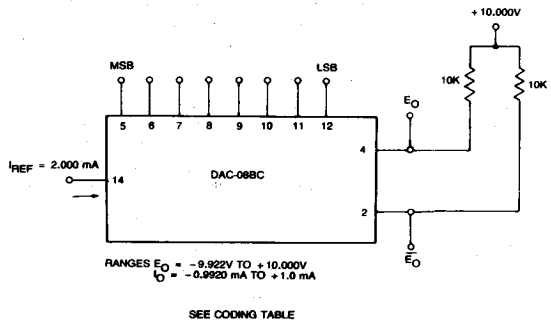


APPLICATION DIAGRAMS (Cont'd)

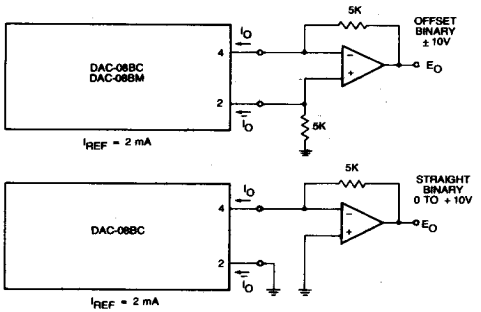
BASIC UNIPOLAR NEGATIVE OPERATION



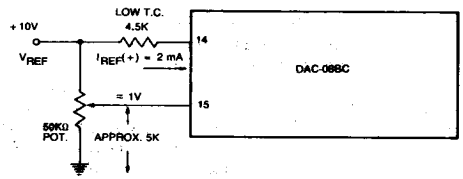
BASIC BIPOLAR OUTPUT OPERATION



VOLTAGE OUTPUT OPERATION



RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT



CALIBRATION AND CODING TABLES

CALIBRATION PROCEDURE

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.
2. **Zero and Offset Adjustments**
   For unipolar operation, set all digital inputs to "0" and adjust the output amplifier zero adjustment for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust the offset adjustment for the negative full-scale voltage shown in the Coding Table.
3. **Gain Adjustment**
   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust the gain adjustment for the positive full-scale voltage shown in the DAC-08B Coding Table.

UNIPOLAR OPERATION—STRAIGHT BINARY CODING
For 5k load resistors at pins 2 and 4

INPUT CODE	E_O	$\overline{E}_O$	I_O	$\overline{I}_O$
1111 1111	−9.961	0.000	1.992	0.000
1110 0000	−8.750	−1.211	1.750	0.242
1100 0000	−7.500	−2.461	1.500	0.492
1000 0000	−5.000	−4.961	1.000	0.992
0100 0000	−2.500	−7.461	0.500	1.492
0000 0001	−0.039	−9.922	0.008	1.984
0000 0000	0.000	−9.961	0.000	1.992

BIPOLAR OPERATION—OFFSET BINARY CODING
For 10k load resistors from pins 2 and 4 to +10V.

INPUT CODE	E_O	$\overline{E}_O$
1111 1111	− 9.922	+10.000
1110 0000	− 7.500	+ 7.578
1100 0000	− 5.000	+ 5.078
1000 0000	0.000	+ 0.078
0100 0000	+ 5.000	− 4.922
0000 0001	+ 9.922	− 9.844
0000 0000	+10.000	− 9.922

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	PACKAGE
DAC-08BC	0°C to +70°C	Plastic
DAC-08BM	−55°C to +125°C	Ceramic