LH155L

96-segment and 73-common Outputs LCD Driver IC with A Built-in RAM

DESCRIPTION

The LH155L is an LCD driver with a built-in RAM suitable for driving medium/small scale dot-matrix LCD panels, and which is capable of being directly connected to the bus line of a microcomputer. The LH155L stores in the RAM the 8-bit parallel or serial display data transferred from the microcomputer and generates LCD drive signals. Since the LH155L features a bit-map type LCD driver that one bit of data in the display RAM corresponds to one dot in the LCD, there is a lot of freedom in displaying. The LH155L has 96 segment outputs and 73 common outputs in a single chip, making it possible to create an LCD system with the fewest number of the chips. The LH155L enables an LCD system for battery-operated, hand-carrying information equipment by securing lower power consumption and wider operating voltage range.
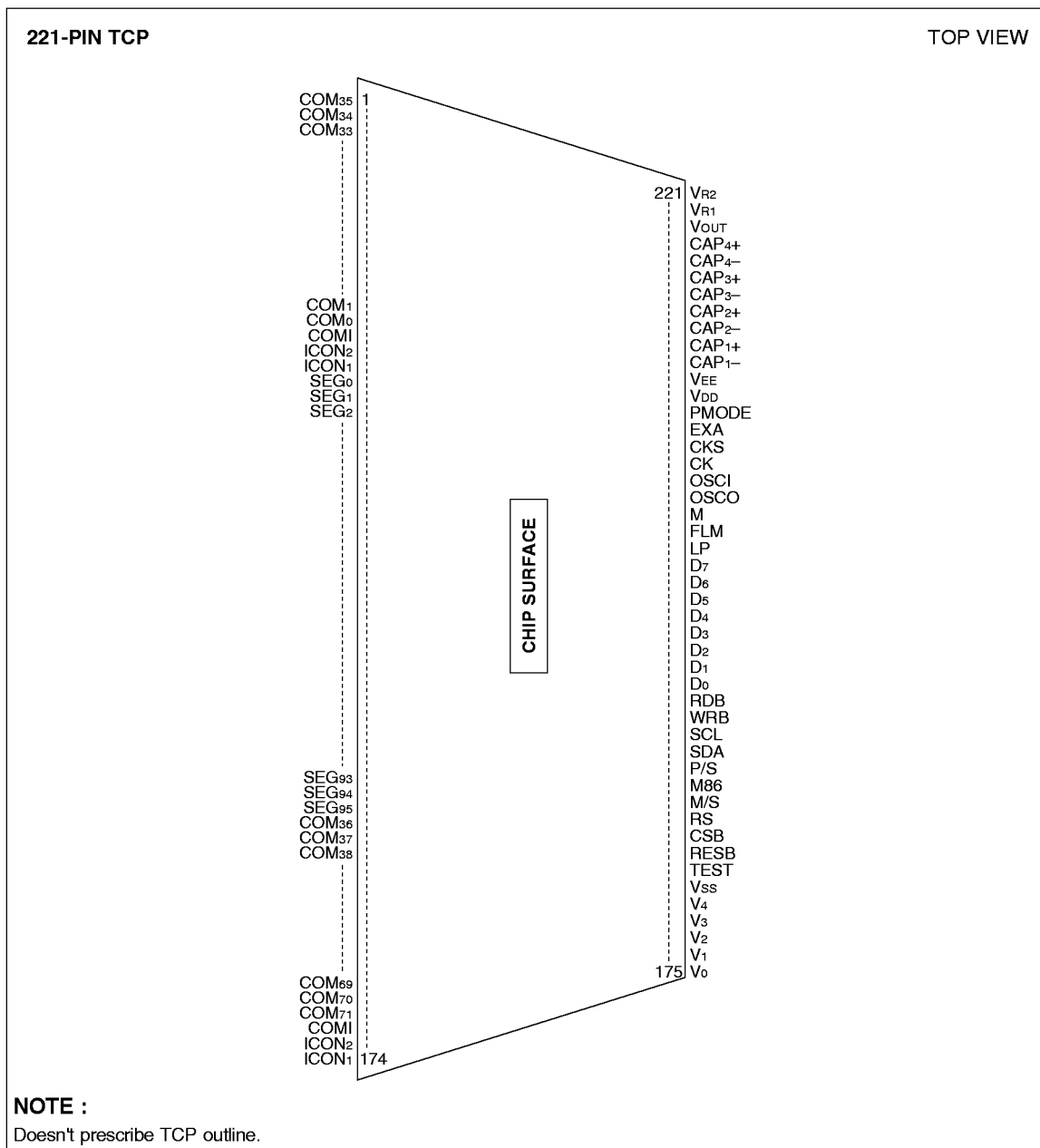
FEATURES

- LCD display by graphic display RAM
  - Normal mode : RAM data "0"→not lighted,
                              RAM data "1"→lighted
  - Reverse mode: RAM data "1"→not lighted,
                              RAM data "0"→lighted
- Display RAM memory capacity :
  96 x 85 = 8 160 bits
- General 8-bit MPU interface : Possible to directly connect 80-family and 68-family MPUs to bus line
- Possible to make serial interface
- Ratio of display duty cycle :
  1/49 or 1/73 (selectable by command)
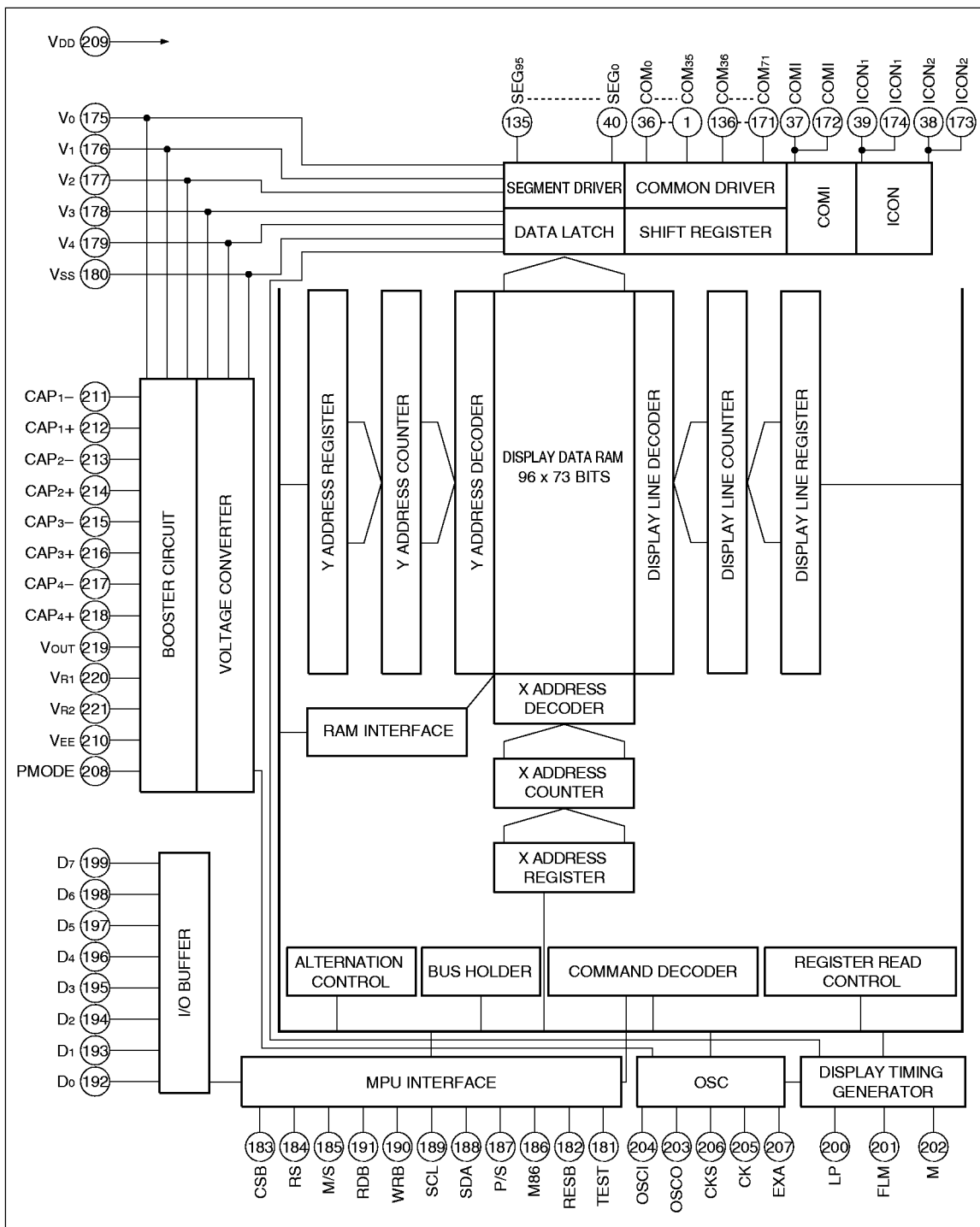- 96-bit automatic transfer from display RAM to display data latch

- Abundant command functions
  - Display data read/write
  - Setting up LCD alternating signal cycle
  - Setting up display starting-line : per line
  - Display ON/OFF
  - Display control of normal and reverse modes
  - Increment control of display RAM address
  - Write control of read modifying
  - Internal register read
  - Power saving mode
- LCD drive power circuit
  - Built-in booster circuit : Three, four, or five times voltage boost is possible
  - Built-in voltage converter : Generates LCD drive voltages (V_0, V_1, V_2, V_3 and V_4) based on the boosted voltage
  - Built-in power bias ratio : 1/7, 1/8 or 1/9 bias (selectable by command)
  - Built-in electronic volume : Controllable in 32 steps
  - Supply voltages
    Logic system : +1.8 to +3.3 V
    LCD drive system : +5.0 to +15.5 V
- Operating temperature : −30 to +85 ˚C
- Package : 221-pin TCP (Tape Carrier Package)

PIN CONNECTIONS

221-PIN TCP   TOP VIEW

COM35 1
COM34
COM33

221 V_{R2}
V_{R1}
V_{OUT}
CAP4+
CAP4−
CAP3+
CAP3−
COM1   CAP2+
COM0   CAP2−
COMI   CAP1+
ICON2   CAP1−
ICON1 V_{EE}
SEG0 V_{DD}
SEG1   PMODE
SEG2   EXA
CKS
CK
OSCI
OSCO
M
CHIP SURFACE   FLM
LP
D7
D6
D5
D4
D3
D2
D1
D0
RDB
WRB
SCL
SDA
SEG93   P/S
SEG94   M86
SEG95   M/S
COM36   RS
COM37   CSB
COM38   RESB
TEST
V_{SS}
V_4
V_3
V_2
175 V_1
175 V_0
COM69
COM70
COM71
COMI
ICON2
ICON1 174

NOTE :

Doesn't prescribe TCP outline.

BLOCK DIAGRAM

VDD (209)

V0 (175)
V1 (176)
V2 (177)
V3 (178)
V4 (179)
VSS (180)

SEG95 (135) ---- SEG0 (40) COM0 (36) COM0 (1) COM35 (136) COM36 (171) COM71 (37) COMI (172) COMI (39) ICON1 (174) ICON1 (38) ICON2 (173) ICON2

SEGMENT DRIVER | COMMON DRIVER | COMI | ICON

DATA LATCH | SHIFT REGISTER

CAP1– (211)
CAP1+ (212)
CAP2– (213)
CAP2+ (214)
CAP3– (215)
CAP3+ (216)
CAP4– (217)
CAP4+ (218)
VOUT (219)
VR1 (220)
VR2 (221)
VEE (210)
PMODE (208)

BOOSTER CIRCUIT

VOLTAGE CONVERTER

Y ADDRESS REGISTER

Y ADDRESS COUNTER

Y ADDRESS DECODER

DISPLAY DATA RAM
96 x 73 BITS

DISPLAY LINE DECODER

DISPLAY LINE COUNTER

DISPLAY LINE REGISTER

X ADDRESS DECODER

RAM INTERFACE

X ADDRESS COUNTER

X ADDRESS REGISTER

D7 (199)
D6 (198)
D5 (197)
D4 (196)
D3 (195)
D2 (194)
D1 (193)
D0 (192)

I/O BUFFER

ALTERNATION CONTROL | BUS HOLDER | COMMAND DECODER | REGISTER READ CONTROL

MPU INTERFACE | OSC | DISPLAY TIMING GENERATOR

(183) CSB
(184) RS
(185) M/S
(191) RDB
(190) WRB
(189) SCL
(188) SDA
(187) P/S
(186) M86
(182) RESB
(181) TEST
(204) OSCI
(203) OSCO
(206) CKS
(205) CK
(207) EXA
(200) LP
(201) FLM
(202) M

1. PIN DESCRIPTION

1.1. Power Supply Pins

SYMBOL	I/O	DESCRIPTION
V_{DD}	Power Supply	Power supply pin for logic, connected to +1.8 to +3.3 V.
V_{SS}	Power Supply	Ground pin, connected to 0 V.
V_0 V_1 V_2 V_3 V_4	Power Supply	Bias power supply pins for LCD drive voltage. • When using an external power supply, convert impedance by using resistance-division of LCD drive power supply or operational amplifier before adding voltage to the pins. • When using the external power supply, maintain the following power supply conditions. $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$ • When the power supply circuit is ON at master operation, LCD drive voltages of V_0 to V_4 are generated by the internal booster circuit and voltage converter. • When using the internal power supply, be sure to connect each capacitor between V_0 to V_4 and V_{SS}.

1.2. LCD Power Supply Circuit Pins

SYMBOL	I/O	DESCRIPTION
CAP1+	O	Connecting pin for the internal booster's capacitor + side. The capacitor is connected between CAP1− and CAP1+.
CAP1−	O	Connecting pin for the internal booster's capacitor − side. The capacitor is connected between CAP1+ and CAP1−.
CAP2+	O	Connecting pin for the internal booster's capacitor + side. The capacitor is connected between CAP2− and CAP2+.
CAP2−	O	Connecting pin for the internal booster's capacitor − side. The capacitor is connected between CAP2+ and CAP2−.
CAP3+	O	Connecting pin for the internal booster's capacitor + side. The capacitor is connected between CAP3− and CAP3+.
CAP3−	O	Connecting pin for the internal booster's capacitor − side. The capacitor is connected between CAP3+ and CAP3−.
CAP4+	O	Connecting pin for the internal booster's capacitor + side. The capacitor is connected between CAP4− and CAP4+.
CAP4−	O	Connecting pin for the internal booster's capacitor − side. The capacitor is connected between CAP4+ and CAP4−.
V_{EE}	Power Supply	Voltage supply pin for generating boosted voltage in the internal booster circuit. Usually the same voltage level as V_{DD}.
V_{OUT}	Power Supply/O	Output pin of boosted voltage in the internal booster circuit. The capacitor must be connected between V_{SS} and V_{OUT}.
V_{R1} V_{R2}	I	Used as input pins for voltage converter. Voltage must be input between the V_{EE} and V_{OUT} pins by voltage divided by resistors.

SYMBOL	I/O	DESCRIPTION
PMODE	I	Pin for controlling LCD power supply. A combination of PMODE pin and ON/OFF command of power supply (PON) enables selection of a specific drive operation.

1.3. System Bus Pins

SYMBOL	I/O	DESCRIPTION
D_7-D_0	I/O	8-bit bi-directional data bus, connected to 8-bit MPU data bus.
CSB	I	Chip selection input pin that decoded address buss signal is input.
RS	I	Distinguishes display RAM data/commands of D_7 to D_0 data transferred from MPU. 0 : The data of D_7 to D_0 show the display RAM data. 1 : The data of D_7 to D_0 show the command data.
RESB	I	Initialized by setting to "L". The reset signals of the system are normally input. Reset operation is performed in accordance with RESB signal level.

RDB
(E)
	I	• In connecting to 80-family MPU :
		  This RDB is a pin for connecting the RDB signal of 80-family MPU. When the signal enters in the "L" state, the data bus of this IC turns to the "output" state.
		• In connecting to 68-family MPU :
		  This RDB becomes a pin for connecting the enable clock signal of 68-family MPU. When the signal enters in the "H" state, the data bus of this IC turns to the "active" state.

WRB
(R/W)
	I	• In connecting to 80-family MPU :
		  This WRB is a pin for connecting the WRB signal of 80-family MPU, and when WRB signal is "L", this pin is "active".
		  The data bus signal is input at the rising edge of WRB signal.
		• In connecting to 68-family MPU :
		  This WRB becomes a pin for connecting the R/W signal of controlling read/write of 68-family MPU.
		  R/W = "H" : Read
		  R/W = "L" : Write

M86	I	MPU interface-type shift pin. M86 = "H" : 68-family interface M86 = "L" : 80-family interface Fixed to either "H" or "L".
SDA	I	Serial-data input pin at time of serial interface selection.
SCL	I	Serial clock pin at time of serial interface selection. Used to shift the SDA data by using the rising edge of SCL. Used to convert into 8-bit data by using the 8th clock at the rising edge of SCL in serial-to-parallel data processing. After data-transferring, or when making no access, be sure to set to "L".

SYMBOL	I/O	DESCRIPTION
P/S	I	Used to shift between parallel interface and serial interface. | P/S	Chip selection	Data identification	Data	Read/Write	Serial clock
---	---	---	---	---	---
H	CSB	RS	D_7 to D_0	RDB, WRB	–
L	CSB	RS	SDA	Write only	SCL	 P/S = "H" for parallel input. Fix SDA and SCL pins to either "H" or "L". P/S = "L" for serial input. Fix D_7 to D_0 pins to High-Z, RDB and WRB pins to either "H" or "L".
TEST	I	For testing. Fix to "L".

1.4. LCD Drive Circuit Signals

SYMBOL	I/O	DESCRIPTION
LP	I/O	The latching signal of display data to count up the display line counter at the rising, and to output the LCD drive signals at the falling. M/S = "H" : Output for master mode M/S = "L" : Input for slave mode
FLM	I/O	I/O pin for LCD synchronous signals (first line marker). When FLM pin is set to "H", the display starting line address is preset in the display line counter. M/S = "H" : Output for master mode M/S = "L" : Input for slave mode
M	I/O	I/O pin for alternating signals of LCD drive output. M/S = "H" : Output for master mode M/S = "L" : Input for slave mode
M/S	I	Used to select either master or slave mode operation. | M/S	State	OSC	P.S.Circuit	LP	FLM	M
---	---	---	---	---	---	---
H	Master	Enabled	Enabled	Output	Output	Output
L	Slave	Disabled	Disabled	Input	Input	Input	 Fix to "H" or "L" at this pin.

SEG0-SEG95	O	Segment output pins for LCD drive.
		According to the data of the display RAM data,
		  non-lighted at "0", lighted at "1" (Normal mode)
		  non-lighted at "1", lighted at "0" (Reverse mode)
		and, by a combination of M signal and display data, one signal level among V_0, V_2, V_3, and V_{SS} is selected.

SYMBOL	I/O	DESCRIPTION
COM0-COM71	O	Common output pins for LCD drive. By a combination of the scanning data and M signals, one signal level among V_0, V_1, V_4 and V_{SS} is selected.<table><tr><th>Data</th><th>M</th><th>Output level</th></tr><tr><td>H</td><td>H</td><td>V_{SS}</td></tr><tr><td>L</td><td>H</td><td>V_1</td></tr><tr><td>H</td><td>L</td><td>V_0</td></tr><tr><td>L</td><td>L</td><td>V_4</td></tr></table>
COMI	O	Common output pin for marker display.
ICON1	O	Common output pin for icon display.
ICON2	O	Data output pin for icon display.

1.5. Pins for Oscillation Circuit

SYMBOL	I/O	DESCRIPTION
OSCI OSCO	I O	Feedback-resistance connecting pin for the internal oscillation circuit.
EXA	I	Input pin of icon clock.
CK	I	Input pin of display master clock at master mode. When using CK pin as an input of the master clock, fix OSCI pin to V_{SS}. When using the internal oscillation circuit as the display master clock, fix CK pin to V_{SS}.
CKS	I	Selection input pin of display master clock at master mode. CKS = "H" : Input the external clock to CK pin. CKS = "L" : The internal oscillation circuit by using OSCI and OSCO pins is used.

∗ Master clock : Clock for oscillation circuit or external clock.
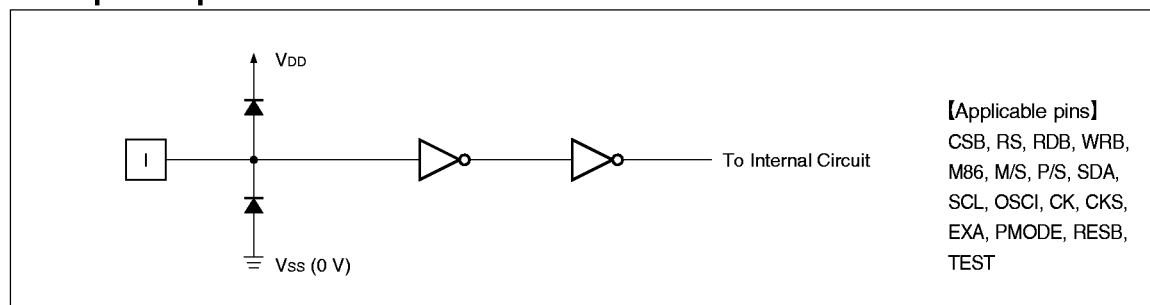
1.6. Input/Output Circuits

【Applicable pins】
CSB, RS, RDB, WRB,
M86, M/S, P/S, SDA,
SCL, OSCI, CK, CKS,
EXA, PMODE, RESB,
TEST
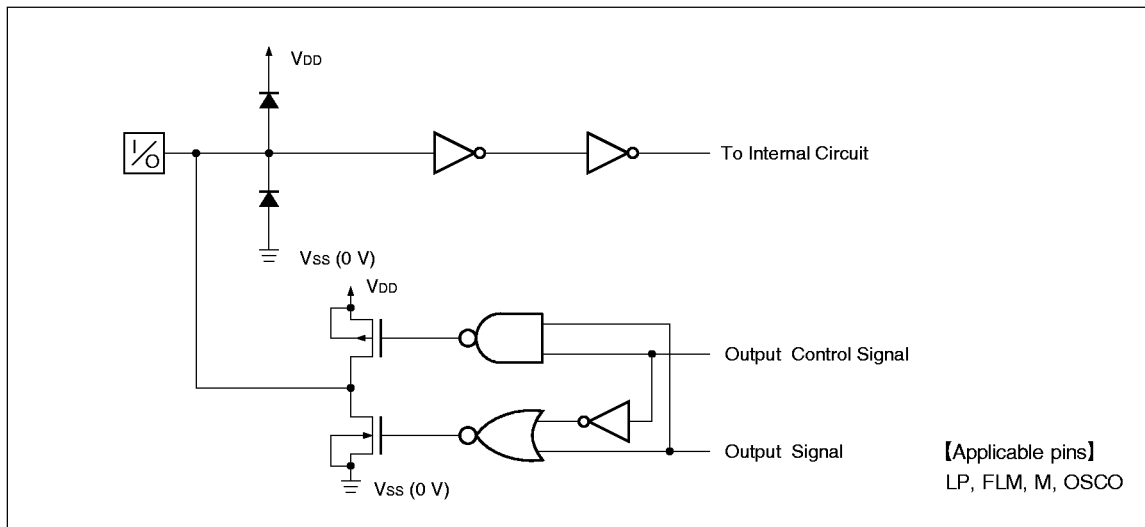
Fig. 1   Input Circuit

Fig. 2 Input/Output Circuit (1)
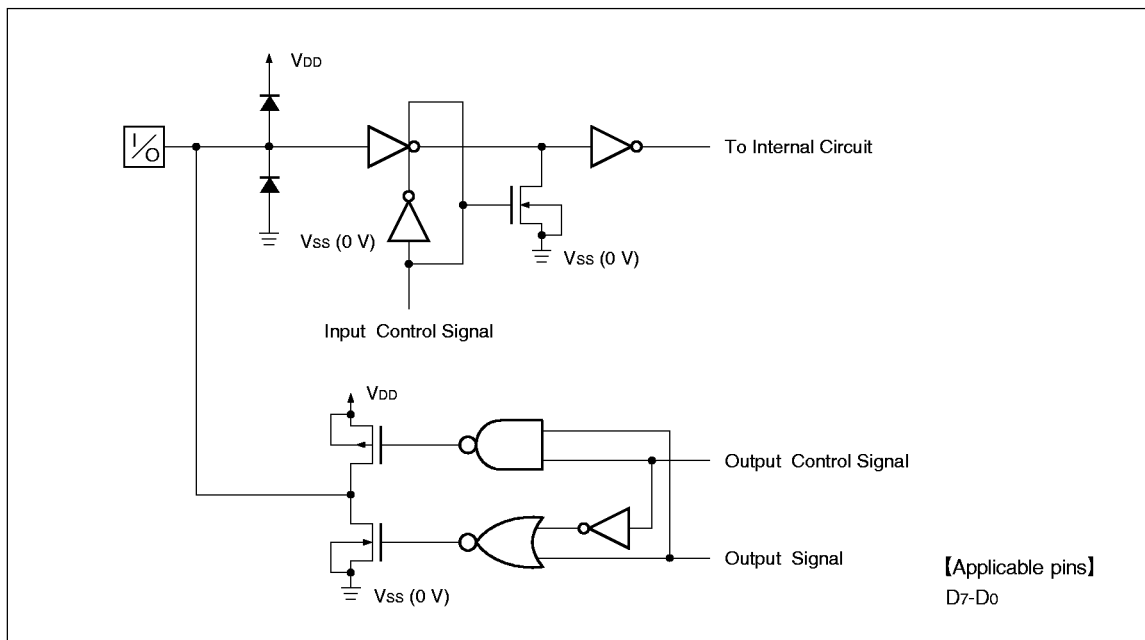
Fig. 3 Input/Output Circuit (2)
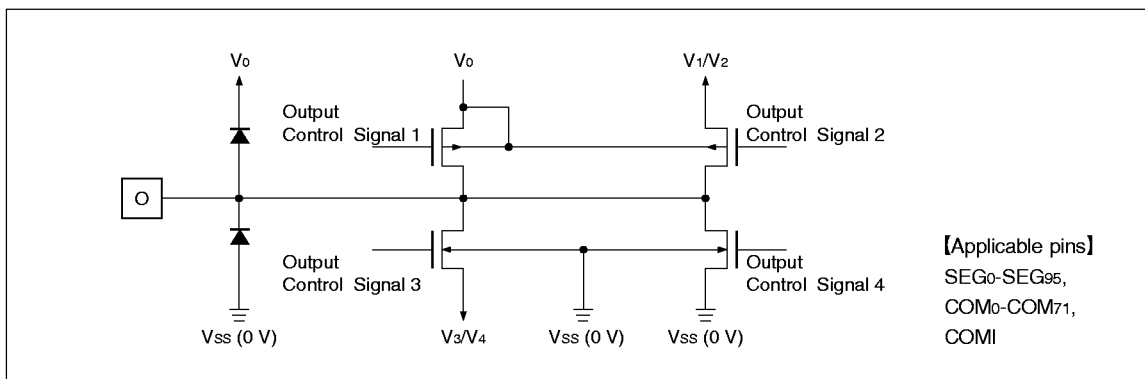
Fig. 4   LCD Drive Output Circuit

2. FUNCTIONAL DESCRIPTION

2.1. MPU Interface

2.1.1. INTERFACE TYPE SELECTION

The LH155L transfers data through 8-bit parallel I/O (D_7 to D_0) or serial data input (SDA, SCL).
The selection between parallel interface and serial interface is made by setting the state of P/S pin to "H" or "L".

When selecting serial interface, data-reading cannot be performed, but data-writing can.

P/S	I/F TYPE	CSB	RS	RDB	WRB	M86	SDA	SCL	DATA
H	Parallel	CSB	RS	RDB	WRB	M86	–	–	D_7 to D_0
L	Serial	CSB	RS	–	–	–	SDA	SCL	–

2.1.2. PARALLEL INPUT

The LH155L can transfer data in parallel by directly connecting 8-bit MPU to the data bus when parallel interface is selected with P/S pin.

As an 8-bit MPU, either 80-family MPU interface or 68-family MPU interface is selected with M86 pin.

M86	MPU TYPE	CSB	RS	RDB	WRB	DATA
H	68-family MPU	CSB	RS	E	R/W	D_7 to D_0
L	80-family MPU	CSB	RS	RDB	WRB	D_7 to D_0

2.1.3. DATA IDENTIFICATION

The LH155L can identify the data of 8-bit data bus
by combinations of RS, RDB and WRB signals.

RS	68-FAMILY	80-FAMILY		FUNCTION
	R/W	RDB	WRB	
1	1	0	1	Reads from internal register
1	0	1	0	Writes to internal register
0	1	0	1	Reads from display data RAM
0	0	1	0	Writes to display data RAM

2.1.4. SERIAL INTERFACE

The serial interface of LH155L can accept inputs of
SDA and SCL in the chip selection state (CSB =
"L"). When not in the chip selection state, the
internal shift register and counter are reset to their
initial condition.

Serial data SDA are input sequentially in order of
D_7 to D_0 at the rising edge of serial clock (SCL)
and are converted into 8-bit parallel data (by serial
to parallel conversion) at the rising edge of the 8th
serial clock, being processed in accordance with
the data. The identification whether the serial data
inputs (SDA) are display data or commands is
judged by input to RS pin.

RS = "L" : Display data
RS = "H" : Commands

After completing 8-bit data transferring, or when
making no access, be sure to set serial clock input
(SCL) to "L".

Protection of SDA and SCL signals against external
noise should be taken in actual wiring. To prevent
the successive recognition errors of transferring
data from external noise, release the chip selection
state (CSB = "H") at every completion of 8-bit data
transferring.
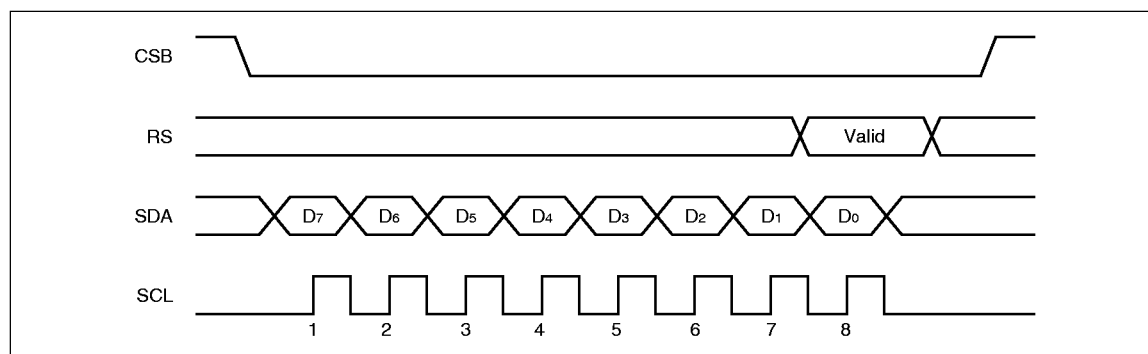
2.2. Access to Display RAM and Internal Register

The LH155L makes access to display RAM, and internal register by data bus D_7 to D_0, chip selection CSB pin, display RAM/register shifting RS pin, and read/write control RDB and WRB pins. When CSB is at "H", it is in non-selective state and cannot access display RAM and internal registers. When making access to them, set CSB to "L".

The access to either display RAM or internal registers can be shifted by RS input.

 RS = "L" : Display RAM data
 RS = "H" : Internal command register

The data of 8-bit data bus D_7 to D_0 are written by write-operation after address setting through MPU. The timing of write is at the rising of WRB for 80-family MPU and at the falling of E for 68-family MPU respectively.

Write is internally processed by intermediately placing the bus holder in the internal data bus. During data writing from MPU, the data are temporally held in the bus holder, then they are written by the time of the next cycle.

Since the read sequence of display RAM data is limited, note that when address set is made, the designated address data are not output to read command immediately after the address set, but are output when the second data are read, resulting in requiring one time dummy read.

Dummy read is always required one time after address set and write cycle.

Data Write Operation
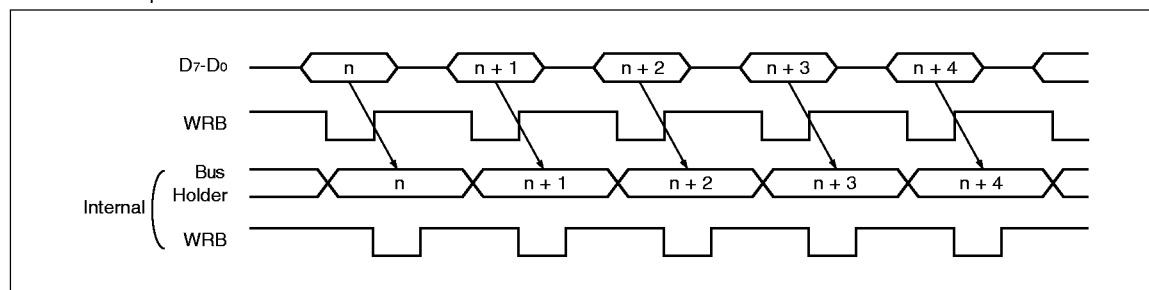
Data Read Operation
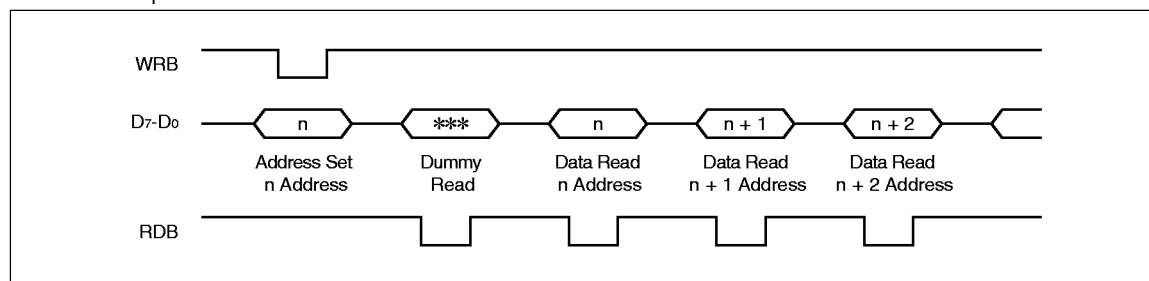
2.3. Read of Internal Register

The LH155L reads not only display RAM, but also the internal registers. Read addresses (0_H, 2_H-E_H) are allotted to each internal register. In reading the internal registers, the addresses of internal registers allotted to read are written in the registers for internal register read and then are read.
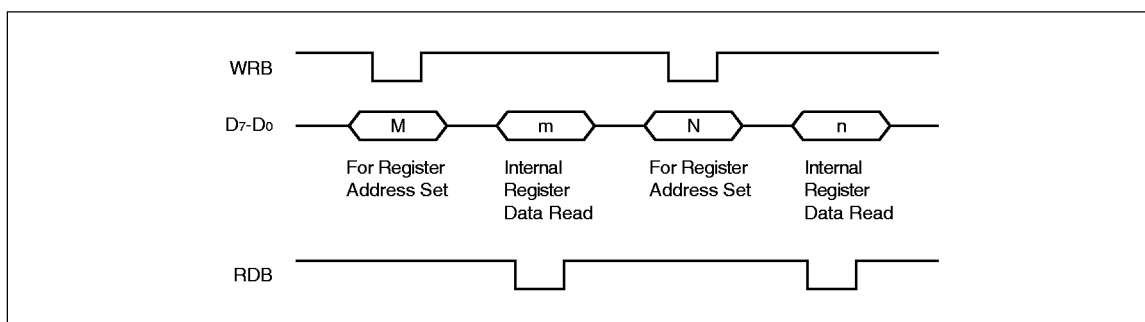
2.4. Display Starting Line Register

This register is for determining display starting line (usually the most upper line) corresponding to COM_0 when displaying the display data RAM.

The register is also used in picture-scrolling. The 7-bit display starting address is set in this register by display starting line setting command.

The register is preset every timing of FLM signal variation in the display line counter. The line counter counts up being synchronized with LP input and generates line addresses which sequentially read out 96-bit data from display RAM to LCD drive circuit.

2.5. Addressing of Display RAM

Display RAM consists of 96 x 85 bits memory, and enables access in 8-bit unit to an address specified by X address and Y address from MPU.

It is possible to set up the addresses X and Y so that they can increment automatically with the address control register. The increment is made every time display RAM is read or written from MPU. (See **Section 4. "COMMAND FUNCTION".**) Though the X direction side is selected by X address while the Y direction side by Y address, $0C_H$-FF_H in the X address are inhibited and do not have the X address set in these addresses.

In the Y direction side, the 96-bit display data are internally read into the display data latch circuit at the rising of LP every one line cycle, and are output from the display data latch circuit at the falling of LP.

55_H-FF_H in the Y address are inhibited and do not have the Y address set in these addresses.

When FLM signals being output in one frame cycle are at "H", the values in the display starting line register are preset in the line counter and the line counter counts up at the falling of LP signals. The display line address counter is synchronized with each timing signal of the LCD system to operate and is independent of address counters X and Y.

2.6. Display RAM Data and LCD

One bit of display RAM data corresponds to one dot of LCD. Normal display and reverse display by REV register are set up as follows.

• Normal display (REV = 0) :
   RAM data = "0"; not lighted
   RAM data = "1"; lighted
• Reverse display (REV = 1) :
   RAM data = "0"; lighted
   RAM data = "1"; not lighted

2.7. Segment Display Output Order/ Reverse Set Up

The order of display outputs, SEG_0 to SEG_{95} can be reversed by reversing access to display RAM from MPU by using REF register, to lessen the limitation on placing IC when composing an LCD module.

2.8. Relationship between Display RAM and Address

(Configuration of display starting line address "00H" is operated.)

X address →

Y address ↓

REF	1	X = 0BH		X = 0AH			X = 00H
	0	X = 00H		X = 01H			X = 0BH

SWAP	1	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0
	0	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D4	D5	D6	D7

Line address / Display starting line

Line address		Common Output
00H	00H	COM0
01H	01H	COM1
02H	02H	COM2
03H	03H	COM3
04H	04H	COM4
05H	05H	COM5
06H	06H	COM6
07H	07H	COM7
08H	08H	COM8
09H	09H	COM9
0AH	0AH	COM10
0BH	0BH	COM11
0CH	0CH	COM12
0DH	0DH	COM13
0EH	0EH	COM14
0FH	0FH	COM15
45H	45H	COM69
46H	46H	COM70
47H	47H	COM71
51H	51H	
52H	52H	
53H	53H	
54H		COMI

Segment Output: SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7 SEG8 SEG9 SEG10 SEG11 SEG12 SEG13 SEG14 SEG15 ... SEG88 SEG89 SEG90 SEG91 SEG92 SEG93 SEG94 SEG95

2.9. Display Timing Generator

The display timing generator generates a timing clock necessary for internal operation and timing pulses (LP, FLM, and M) by inputting the master clock CK or by the oscillation circuit of OSCI and OSCO.

By setting up master/slave mode (M/S), the state of timing pulse pins and the timing generator changes.

Display Timing Pulse Pins and Timing Generator State

M/S PIN	MODE	LP PIN	M PIN	FLM PIN	STATE OF TIMING GENERATOR
L	Slave	Input	Input	Input	Stop of LP, M, FLM generation circuit
H	Master	Output	Output	Output	Operating state

2.10. Signal Generation to Display Line Counter, and Display Data Latching Circuit

Both the clock to the line counter and latching signals to display data latching circuit from the display clock (LP) are generated.

Synchronized with the display clock, the line addresses of display RAM are generated and 96-bit display data are latched to display-data latching circuit to output to the LCD drive circuit (SEG output).

Readout of the display data to the LCD drive circuit is completely independent of MPU. Therefore, a MPU that has no relationship the readout operation of the display data can access it.

2.11. Generation of The Alternating Signal (M) and The Synchronous Signal (FLM)

LCD alternating signal (M) and synchronous signal (FLM) are generated by the display clock (LP). The FLM generates alternated drive waveform to the LCD drive circuit. Normally, the FLM generates alternated drive waveform every frame unit (M-signal level is reversed every one frame).

But by setting up data (n − 1) in an n-line reverse register and n-line alternating command (NLIN) at "H", n-line reverse waveform is generated.

When the LH155L is used in multi-chip, the signals of LP, FLM, and M must be sent from master side in the slave operation.

2.12. Display Data Latching Circuit

Display data latching circuit temporally latches display data that is output display data to LCD drive circuit from display RAM every one common period. Normal display/reverse display, display ON/OFF, and display all ON commands are operated by controlling data in the latch. And no data within display RAM changes.

2.13. Output Timing of LCD Driver

Display timing at normal mode, 1/73 duty
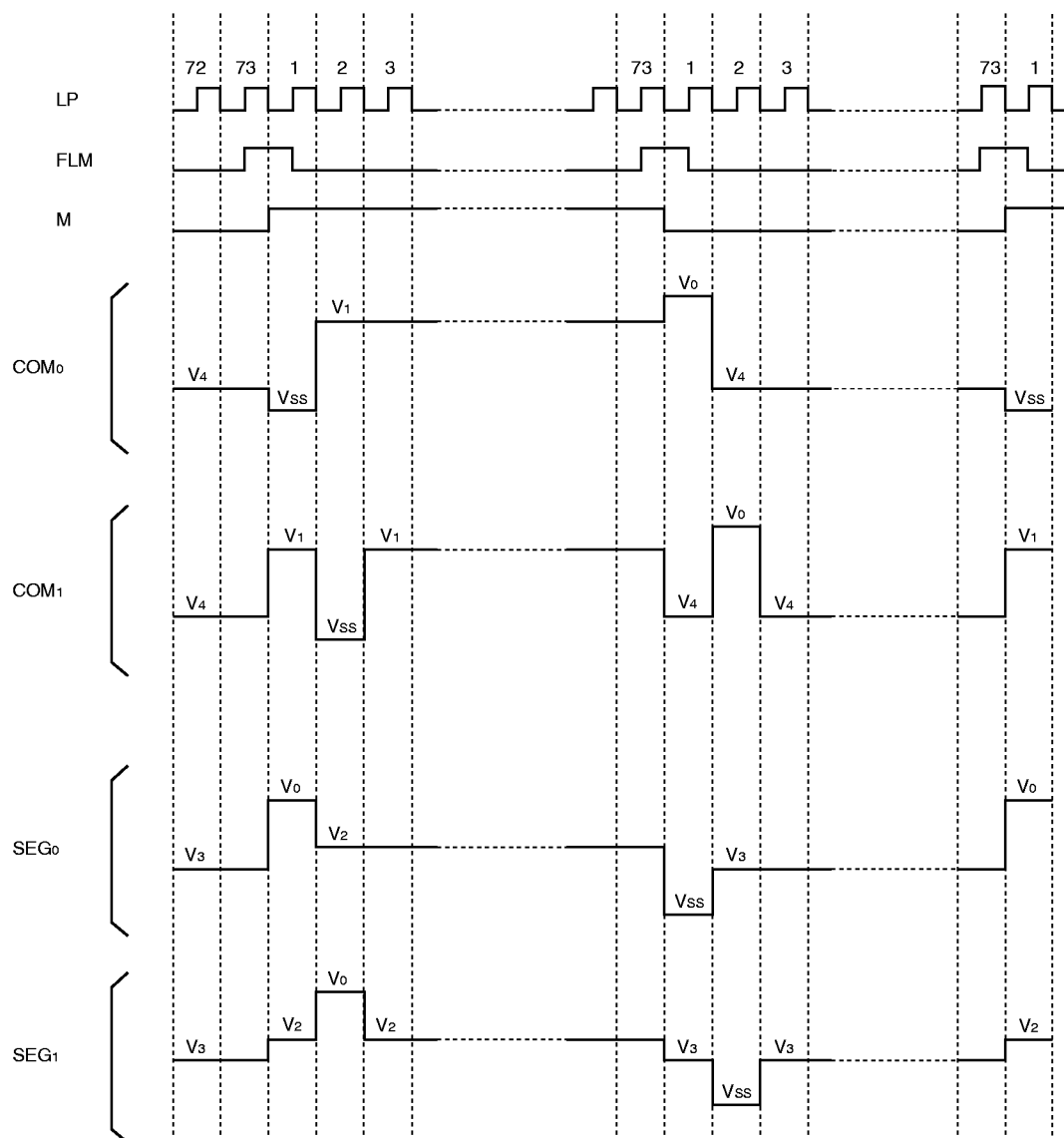
2.14. LCD Drive Circuit

This drive circuit generates 4 levels of LCD drive voltage. The circuit has 96 segment outputs and 73 common outputs and outputs combined display data and M signal. One of the common outputs, COMI is for marker display only. A common drive circuit that has a shift register sequentially outputs common scan signals.

2.15. Oscillation Circuit

The frequency of this CR oscillator is controlled by the feedback resistor R_F.

The output from this oscillator is used as the timing signal source of the display and the boosting clock to the booster circuit. This is valid only in the master operation mode.

During the slave operation mode, maintain OSCI pin at V_{SS} and OSCO pin open (NC).

When in the master operation mode and if external clock is used, maintain OSCI pin at V_{SS} and OSCO pin open (NC), and feed the clock to CK pin.

The duty cycle of the external clock must be 50%.

The CKS pin selects either internal oscillation circuit or external clock.

CKS	MASTER MODE		SLAVE MODE	
	OSC	External Clock (CK)	OSC	External Clock (CK)
L	Enabled	Disabled	Disabled	Disabled
H	Disabled	Enabled	Disabled	Disabled

2.16. Power Supply Circuit

This circuit supplies voltages necessary to drive an LCD. This circuit is valid only in the master operation mode. The circuit consists of booster circuit and voltage converter.

Boosted voltage from the booster circuit is fed to the voltage converter which converts this high input voltage into V_0, V_1, V_2, V_3 and V_4 which are used to drive the LCD. This internal power supply should not be used to drive a large LCD panel containing many pixels or a large LCD panel that has large capacity consisting of more than one chip.

Otherwise, display quality will degrade considerably. Instead, use an external power supply.

This internal power supply is controlled by the power supply circuit ON/OFF command (PON).

When the internal power supply is turned off, the booster circuit and voltage converter are also turned off.

When using the external power supply, turn off the internal power supply, disconnect pins CAP1+, CAP1−, CAP2+, CAP2−, CAP3+, CAP3−, CAP4+, CAP4−, V_{OUT}, V_{EE}, V_{R1} and V_{R2}, and keep PMODE pin at V_{SS}. Then, feed external LCD drive voltages to pins V_0, V_1, V_2, V_3 and V_4. This circuit can be changed by the state of PMODE pin.

PON	PMODE	BOOSTER CIRCUIT	VOLTAGE CONVERTER	EXTERNAL VOLTAGE INPUT	NOTE
0	0	Disabled	Disabled	V_0, V_1, V_2, V_3, V_4	1
0	1	Disabled	Disabled	V_0, V_1, V_2, V_3, V_4	1
1	0	Enabled	Enabled	−	
1	1	Disabled	Enabled	V_{OUT}, V_{R1}, V_{R2}	2

NOTES :

1. Because the booster circuit and voltage converter are not functioning, disconnect pins CAP1+, CAP1−, CAP2+, CAP2−, CAP3+, CAP3−, CAP4+, CAP4−, V_{OUT}, V_{EE}, V_{R1}, and V_{R2}.
   Apply external LCD drive voltages to corresponding pins.
2. Because the booster circuit is not functioning, disconnect pins CAP1+, CAP1−, CAP2+, CAP2−, CAP3+, CAP3−, CAP4+, CAP4−, V_{OUT}, V_{EE}, V_{R1}, and V_{R2}.
   Derive the voltage source to be supplied to the voltage converter from V_{OUT} pin and then output LCD drive voltage to V_{R1}, and V_{R2} pins. The voltage level at V_{R1} and V_{R2} pins must be $V_{R2} \leq V_{R1} \leq V_{OUT}$.

2.17. Booster Circuit

Placing capacitor C_1 across CAP1+ and CAP1− and across CAP2+ and CAP2− and across CAP3+ and CAP3− and across CAP4+ and CAP4− boosts the voltage coming from V_{EE} and V_{SS} five times and outputs the boosted voltage to V_{OUT} pin.

Placing C_1 across CAP1+ and CAP1− and across CAP2+ and CAP2− and across CAP3+ and CAP3− and shorting together pins CAP3+ and CAP4+ limits the output on V_{OUT} pin to four times the input voltage.

Since the booster circuit uses the clock derived from the internal oscillation circuit or external clock as the boosting clock, the internal oscillation circuit must be enabled, or if external clock is selected, it must be fed to CK pin.

The output level at the V_{OUT} pin does not exceed the recommended maximum operating voltage (15.5 V) when the voltage is boosted. If this value is exceeded, the operation of the LH155L is not covered by warranty.

V_{OUT} = 12 V ——————

V_{EE} = 3 V ——————

V_{SS} = 0 V ——————

When Boosted Four Times

V_{OUT} = 15 V ——————

V_{EE} = 3 V ——————

V_{SS} = 0 V ——————

When Boosted Five Times
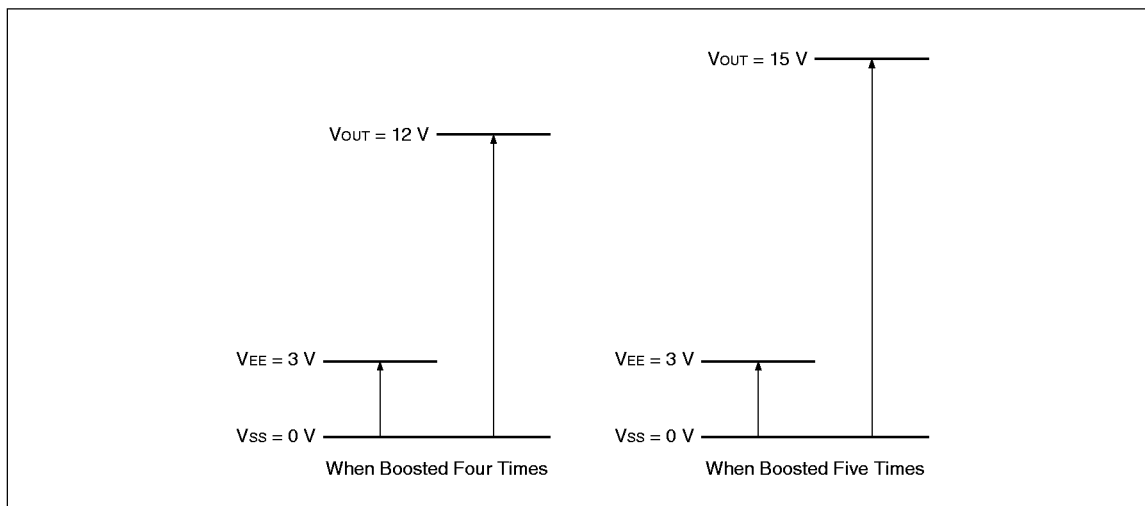
2.18. Voltage Control Circuit

The boosted voltage at the V_{OUT} pin is connected to the V_{R1} and V_{R2} pins and then the LCD drive voltages (V_0, V_1, V_2, V_3 and V_4) are generated via the voltage converter. The input level at the V_{R1} and V_{R2} must meet the electric potential condition of $V_{R1} \geq V_{R2}$. The internal electronic volume divides the electric potential between the V_{R1} and V_{R2} into 32 segments.

Since the V_{R1} and V_{R2} pins have high input impedance, the input voltage levels at the V_{R1} and V_{R2} are determined by the resistance ratio of R_1, R_2, and R_3. The current flowing between the V_{OUT} and V_{SS} pins is determined by the combined resistance of R_1, R_2, and R_3. Therefore, R_1, R_2, and R_3 must be selected in accordance with the above current as well as the input voltage levels at the V_{R1} and V_{R2}.

The boosted voltage at the V_{OUT} pin originates from the voltage supplied at the V_{EE} pin. Thus, the DC path current generated with R_1, R_2, and R_3 connected between the V_{OUT} and V_{SS} pins is supplied as current at the V_{EE} pin. The electric current value, five times larger than the DC path current generated between the V_{OUT} and V_{SS} pins when the voltage is boosted five times, is added as supply current at the V_{EE} pin (four times larger current is added for four times voltage). Take sufficient care that the input levels at the V_{R1} and V_{R2} pins do not fluctuate with external noise (connect capacitor C_3).
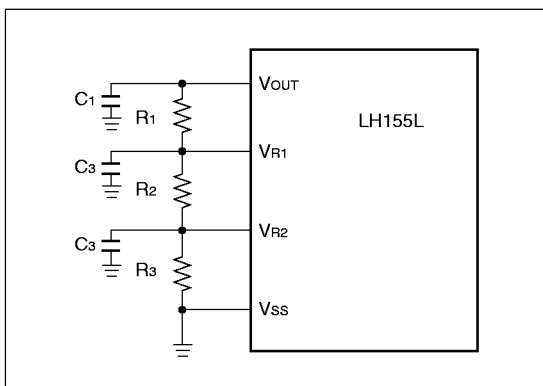
Example of Voltage Control Circuit

2.19. Electronic Volume

The voltage converter incorporates an electronic volume, which allows the LCD drive voltage level V_0 to be controlled with a command and also allows the tone of LCD to be controlled.

If 5-bit data is stored in the register of the electronic volume, one level can be selected among 32 voltage values for the LCD drive voltage V_0.

The voltage control range of the electronic volume is determined by the input voltage levels at the V_{R1} and V_{R2}. This means that the voltage range of (V_{R1} to V_{R2}) is the controllable voltage range of the electronic volume.

The electric potential relation between the V_{R1} and V_{R2} pins must be $V_{R1} \geq V_{R2}$. The input voltage levels at the V_{R1} and V_{R2} pins must be selected in accordance with the voltage levels to be obtained with the electronic volume.

2.20. LCD Drive Voltage Generation Circuit

The voltage converter contains the voltage generation circuit. The LCD drive voltages other than V_0, that is, V_1, V_2, V_3 and V_4, are obtained by dividing V_0 through a resistor network. The LCD drive voltage from LH155L is biased at 1/7, 1/8 or 1/9.

When using the internal power supply, connect a stabilizing capacitor C_2 to each of pins V_0 to V_4.

The capacitance of C_2 should be determined while observing the LCD panel to be used. In this case, connect a capacitor C_3 to stabilize input voltage to V_{R1} and V_{R2}. A value of C_3 can be defined selectively.

2.21. Example of Power Supply Circuit Connection

When Using The External Power Supply   When Using The Internal Power Supply

Recommended values

C1	2.0 to 5.0 μF (B)*
C2	2.0 to 5.0 μF (B)*
C3	0.01 to 0.1 μF
RF	2 MΩ
R1 + R2 + R3	2.0 to 4.0 MΩ

∗ B characteristics must be used with C1 and C2.

20
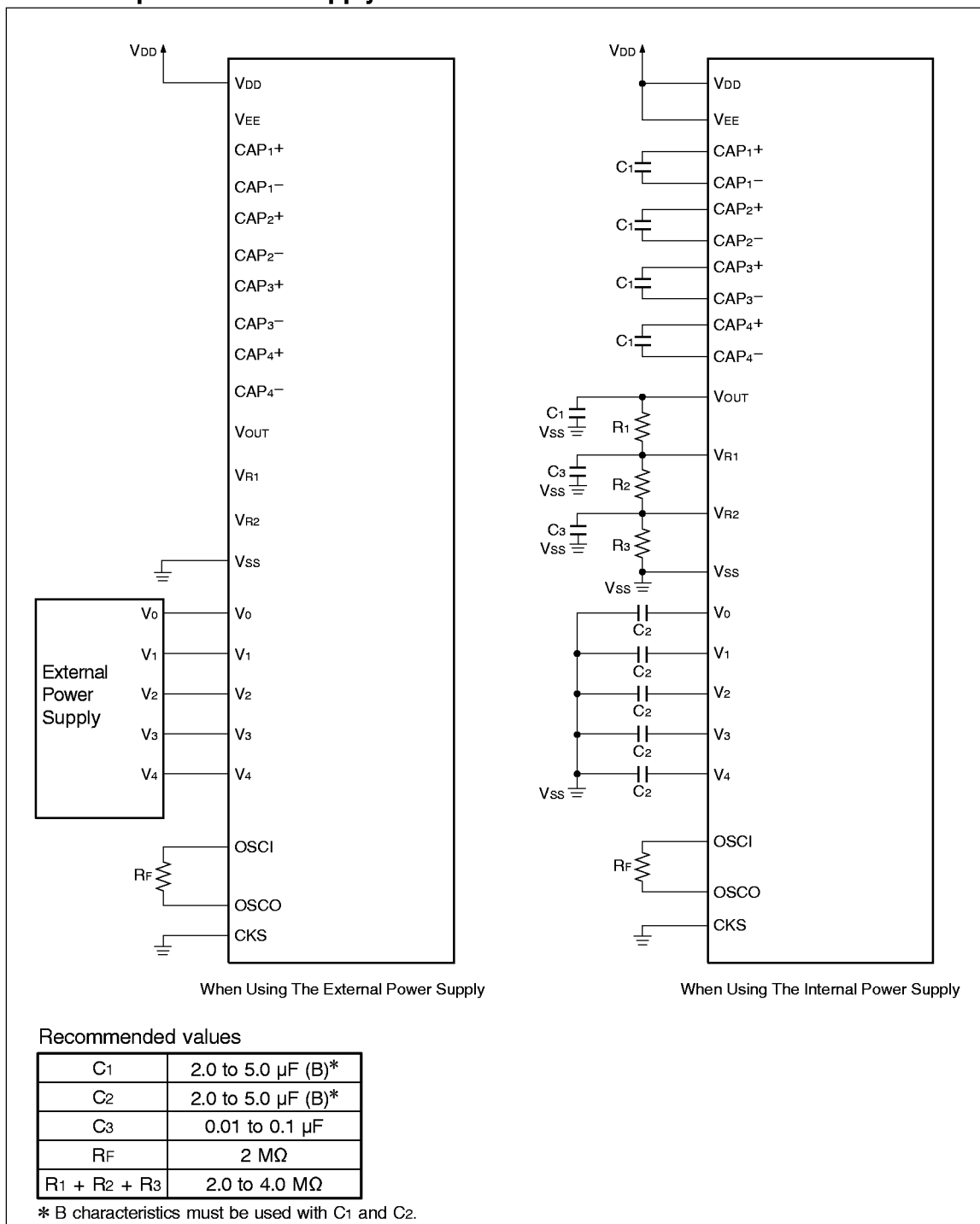
2.22. Initialization

The LH155L is initialized by setting RESB pin to "L".
Normally, RESB pin is initialized together with MPU
by connecting to the reset pin of MPU.
When power is ON, be sure to reset operation.

PARAMETER	INITIAL STATE
Display RAM	Not fixed
X-address	00_H set
Y-address	00_H set
Display starting line	Set at the first line (0_H)
Display ON/OFF	Display OFF
Display normal/reverse	Normal
Display duty	1/73
n-line alternating	Every frame unit
Common shift direction	COM0→COM71
Increment mode	Increment OFF
REF mode	Normal
Data SWAP mode	OFF
Register in electronic volume	(1, 1, 1, 1, 1)
Power supply	OFF

3. PRECAUTIONS

**Precautions when connecting or disconnecting
the power supply**

This IC may be permanently damaged by a high
current which may flow if voltage is supplied to the
LCD drive power supply while the logic system
power supply is floating. The details are as follows.

① When using an external power supply
● When connecting the power supply
   After connecting the logic system power supply,
   make reset operation and then apply external
   LCD drive voltages to corresponding pins. (V_0,
   V_1, V_2, V_3, V_4 or V_{OUT}, V_{R1} and V_{R2})
● When disconnecting the power supply
   After executing HALT command, disconnect
   external LCD drive voltages and then disconnect
   the logic system power supply.

② When using the internal power supply
● When connecting the power supply
   After connecting the logic system power supply,
   make reset operation and then execute PON
   command.
● When disconnecting the power supply
   After executing HALT command, disconnect the
   logic system power supply.

It is advisable to connect the serial resistor (50 to
100 Ω) or fuse to the LCD drive power V_{OUT} or V_0
of the system as a current limiter. Set up a suitable
value of the resistor in consideration of the display
grade.

4. COMMAND FUNCTION

4.1. Command Function Table

INSTRUCTION	CODE					CODE								FUNCTION
	CSB	RS	WRB	RDB	RE	D7	D6	D5	D4	D3	D2	D1	D0	
Display data write	0	0	0	1	0	WRITE DATA								Writes to display RAM.
Display data read	0	0	1	0	0	READ DATA								Reads from display RAM.
X address set (Lower) [0H]	0	1	0	1	0	0	0	0	0	X Address				Sets X direction address in display RAM.
Y address set (Lower) [2H]	0	1	0	1	0	0	0	1	0	Y Address				Sets of Y direction address in display RAM.
Y address set (Upper) [3H]	0	1	0	1	0	0	0	1	1	*	Y Address			Sets Y direction address in display RAM.
Display starting line set (Lower) [4H]	0	1	0	1	0	0	1	0	0	Display Starting Line				Sets line address of RAM making COM0 display.
Display starting line set (Upper) [5H]	0	1	0	1	0	0	1	0	1	*	Display Starting Line			Sets line address of RAM making COM0 display.
n-line alternating set (Lower) [6H]	0	1	0	1	0	0	1	1	0	Alternating Line				Sets the number of alternating reverse line.
n-line alternating set (Upper) [7H]	0	1	0	1	0	0	1	1	1	*	Alternating Line			Sets the number of alternating reverse line.
Display control (1) set [8H]	0	1	0	1	0	1	0	0	0	SHIFT	ICON	ALLON	ON/OFF	①
Display control (2) set [9H]	0	1	0	1	0	1	0	0	1	REV	NLIN	SWAP	REF	②
Increment control set [AH]	0	1	0	1	0	1	0	1	0	0	AIM	AYI	AXI	③
Power control (1) set [BH]	0	1	0	1	0	1	0	1	1	EXA	HALT	PON	ACL	④
Electronic volume set	0	1	0	1	0	1	1	0	1	DVL3	DVL2	DVL1	DVL0	Sets electronic volume. (Lower)
[DH]	0	1	0	1	1	1	1	0	1	*	*	*	DVL4	Sets electronic volume. (Upper)
Power control (2) set [EH]	0	1	0	1	0	1	1	1	0	*	DU0	BS1	BS0	Sets bias ratio. Sets duty ratio.
RE set [FH]	0	1	0	1	0/1	1	1	1	1	*	*	TEST	RE	Sets RE flag.
Address set for internal register read	0	1	0	1	0	1	1	0	0	Address for Register Read				Sets address of internal register for reading.
Internal register read	0	1	1	0	0	*	*	*	*	Read Data				Reads out internal register.

① SHIFT : Common shift direction, ICON : Icon display ON, ALLON : All display ON, ON/OFF : Display ON/OFF control

② REV : Display normal/reverse, NLIN : n-line reverse ON, SWAP : Data for display swap, REF : Segment output for display normal/reverse

③ AIM : Increment mode selection, AYI : Y increment, AXI : X increment

④ EXA : Icon clock IN/OUT, HALT : HALT ON, PON : Power supply circuit ON, ACL : Reset operation

* mark means "Don't care".

Parenthesis [ ] shows address for internal register read.

Do not use TEST command for IC testing.

The LH155L has a lot of commands, as shown in the list of commands, and each command is explained in detail as follows.

Data codes and command codes are defined as follows and the execution of commands must be made in the chip selection state (CSB = "L").

(For example X address)

RS	D7	D6	D5	D4	D3	D2	D1	D0
*	0	0	0	0	AX3	AX2	AX1	AX0

Command Codes	Data Codes

* RS = "0" : RAM data access (Refer to **Sections 4.2. and 4.3.**.)
  RS = "1" : Register access (Refer to **Sections 4.4. through 4.17.**.)
  The undefined command codes are inhibited.

4.2. Data Write to Display RAM

D7	D6	D5	D4	D3	D2	D1	D0
Display RAM Write Data								

CSB	RS	WRB	RDB	RE
0	0	0	1	0

The display RAM data of 8-bit are written in the designated X and Y addresses.

4.3. Data Read to Display RAM

D7	D6	D5	D4	D3	D2	D1	D0
Display RAM Read Data								

CSB	RS	WRB	RDB	RE
0	0	1	0	0

The 8-bit contents of display RAM designated in X and Y addresses are read out.
Immediately after data are set in X and Y addresses, dummy read is necessary one time.

4.4. X Address Register Set

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : AX3 to AX0 = 0H, read address : 0H)

Addresses of display RAM's X direction are set. The values of AX3 to AX0 are usable up to 00H-0BH, but 0CH-FFH are inhibited. When the register setting of SEG output normal/reverse is REF = "0", the data of AX3 to AX0 are addressed to display RAM as they are.
When REF = "1", the data of 0BH-(AX3 to AX0)H are addressed to the display RAM.

4.5. Y Address Register Set

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	WRB	RE
0	0	1	0	AY3	AY2	AY1	AY0		0	1	0	1	0

(At the time of reset : AY3 to AY0 = 0H, read address : 2H)

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
0	0	1	1	*	AY6	AY5	AY4		0	1	0	1	0

* mark means "Don't care".
(At the time of reset : AY6 to AY4 = 0H, read address : 3H)

Addresses of display RAM's Y direction are set. In data-setting, lower place and upper place are divided with 4 bits and 3 bits respectively. When data are set, lower place should be set first and upper place should be set second.

The values of AY6 to AY0 are usable up to 00H-54H, but 55H-FFH are inhibited.
The addresses of (AY6 to AY0) = 54H are display RAM area for marker display.

4.6. Display Starting Line Register Set

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
0	1	0	0	LA3	LA2	LA1	LA0		0	1	0	1	0

(At the time of reset : LA3 to LA0 = 0H, read address : 4H)

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
0	1	0	1	*	LA6	LA5	LA4		0	1	0	1	0

* mark means "Don't care".
(At the time of reset : LA6 to LA4 = 0H, read address : 5H)

The display line address is required to designate, and the designated address becomes the display line of COM0.

The display of LCD is displayed from the designated display starting line address to the increment direction of the line address.

LA6	LA5	LA4	LA3	LA2	LA1	LA0	LINE ADDRESS
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
1	0	1	0	0	1	1	83

4.7. n-line Alternating Register Set

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
0	1	1	0	N3	N2	N1	N0		0	1	0	1	0

(At the time of reset : N3 to N0 = 0$_H$, read address : 6$_H$)

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
0	1	1	1	*	N6	N5	N4		0	1	0	1	0

* mark means "Don't care".
(At the time of reset : N6 to N4 = 0$_H$, read address : 7$_H$)

The reverse line number of LCD alternated drive is required to be set in the register.
The line number possible to be set is 2 to 72 lines. The values set up by the n-line alternating register become enabled when the n-line alternated drive command is ON (NLIN = "1").
When the n-line alternated drive command is OFF (NLIN = "0"), an alternated drive waveform which reverses by frame cycle is generated.

N6	N5	N4	N3	N2	N1	N0	REVERSE LINE NUMBER
0	0	0	0	0	0	0	–
0	0	0	0	0	0	1	2
1	0	0	0	1	1	1	72

4.8. Alternating Timing

(1) At The Time of n-line Alternating OFF (in case of 1/73 duty display)
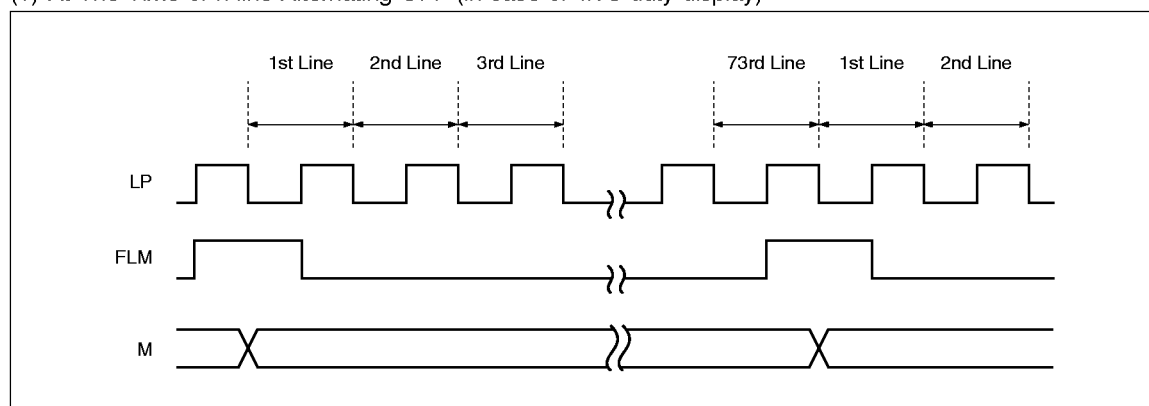
(2) At The Time of n-line Alternating ON
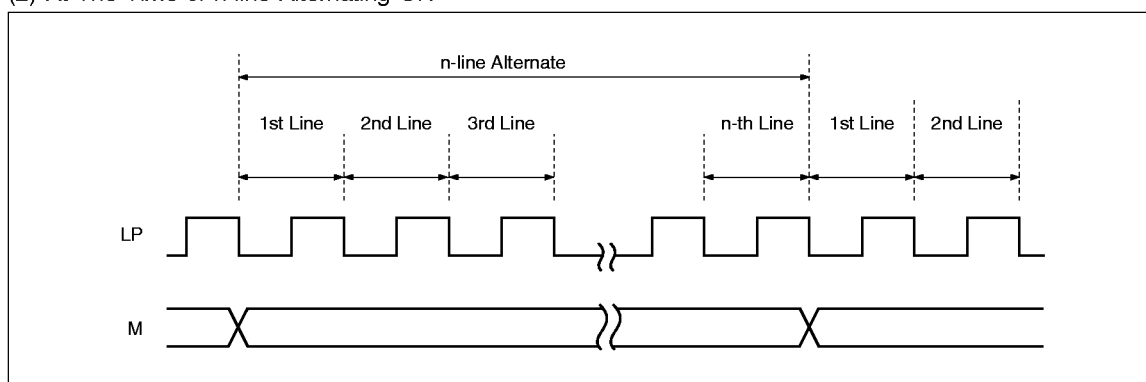
4.9. Display Control (1) Register Set

D7	D6	D5	D4	D3	D2	D1	D0	CSB	RS	WRB	RDB	RE
1	0	0	0	SHIFT	ICON	ALLON	ON/OFF	0	1	0	1	0

(At the time of reset : (SHIFT, ICON, ALLON, ON/OFF) = 0_H, read address : 8_H)

Various controls of display are set up.

(1) ON/OFF Command
To control ON/OFF of display.
ON/OFF = "0" : Display OFF
ON/OFF = "1" : Display ON

(2) ALLON Command
Regardless of the data of the display RAM, all the displays are ON.
This command has priority over display normal/reverse commands.
ALLON = "0" : Normal display
ALLON = "1" : All displays lighted.

(3) ICON Command
To control ON/OFF of the icon display.
ICON = "0" : Display OFF
ICON = "1" : Display ON

(4) SHIFT Command
The shift direction of display scanning data in the common drive output is selected.
SHIFT = "0" : $COM_0 \rightarrow COM_{71}$ shift-scan
SHIFT = "1" : $COM_{71} \rightarrow COM_0$ shift-scan

4.10. Display Control (2) Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	REV	NLIN	SWAP	REF

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : (REV, NLIN, SWAP, REF) = 0H, read address : 9H)

Various controls of display are set up.

(1) REF Command

When MPU accesses to display RAM, the relationship between X address and write data is normalized or reversed.
Therefore, the order of segment drive output can be reversed by register setting, to lessen the limitation on placing IC when composing an LCD module.

REF	ACCESS FROM MPU		INTERNAL ACCESS		CORRESPONDING
	X ADDRESS	D7-D0	X ADDRESS	D7-D0	SEG OUTPUT
0	nH	D0 (LSB) | D7 (MSB)	nH	(LSB) | (MSB)	SEG (8 x nH) output | SEG (8 x nH + 7) output
1	nH	D0 (LSB) | D7 (MSB)	0BH-nH	(MSB) | (LSB)	SEG (8 x (0BH − nH) + 7) output | SEG (8 x (0BH − nH)) output

(2) SWAP Command

When data to display RAM are written, the write data are swapped.

SWAP = "0" : Normal mode. In data-writing, the data of D7 to D0 can be written to the display RAM.

SWAP = "1" : SWAP mode ON. In data-writing, the swapped data of D7 to D0 can be written to the display RAM.

	SWAP = "0"	SWAP = "1"
EXTERNAL DATA	D7 D6 D5 D4 D3 D2 D1 D0	D7 D6 D5 D4 D3 D2 D1 D0
INTERNAL DATA	d7 d6 d5 d4 d3 d2 d1 d0	d0 d1 d2 d3 d4 d5 d6 d7

(3) NLIN Command

The ON/OFF control of n-line alternated drive is performed.

NLIN = "0" : n-line alternated drive OFF. By using frame cycle, the alternating signals (M) are reversed.

NLIN = "1" : n-line alternated drive ON. According to data set up in n-line alternating register, the alternation is made.

(4) REV Command

Corresponding to the data of display RAM, the lighting or not-lighting of the display is set up.

REV = "0" : When RAM data are at "H", LCD at ON voltage (normal).

REV = "1" : When RAM data are at "L", LCD at ON voltage (reverse).

4.11. Increment Control Register Set

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
1	0	1	0	0	AIM	AYI	AXI		0	1	0	1	0

(At the time of reset : (AIM, AYI, AXI) = 0H, read address : AH)

The increment mode is set up when accessing the display RAM.
By AIM, AYI and AXI registers, the setting-up of increment operation/non-operation for the X-address counter and the Y-address counter every write access or every read access to the display RAM is possible.
In setting to this control register, the increment operation of address can be made without setting successive addresses for writing data or for reading data to display RAM from MPU. After setting this register, be sure to set the X and Y address registers.
Because it is not assuring the data of X and Y address registers after setting increment control registers, the increment control of X and Y addresses by AIM, AYI and AXI registers is as follows.

AIM	SELECTION OF INCREMENT TIMING	REFERENCE
0	When writing to display RAM or reading from display RAM	①
1	Only when writing to display RAM (read modify)	②

① This is effective when subsequently writing and reading the successive address areas.

② This is effective in the case that, after reading and writing the successive address areas for every address, the read data are modified to write.

AYI	AXI	SELECTION OF INCREMENT ADDRESS	REFERENCE
0	0	Increment is not made	①
0	1	X address automatic increment	②
1	0	Y address automatic increment	③
1	1	X and Y addresses cooperative, automatic increment	④

① Regardless of AIM, no increment for X and Y addresses.

② According to the setting-up of AIM, increment or decrement for only X address.

In accordance with the REF conditions of SEG normal/reverse output setting register, X address becomes as follows.

• At REF = "0" (normal output), increment by loop of

$$00_H \longrightarrow 0B_H$$
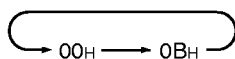
• At REF = "1" (reverse output), decrement by loop of

$$0B_H \longrightarrow 00_H$$
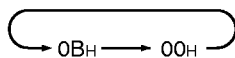
③ According to the setting-up of AIM, increment for only Y address.

Regardless of REF, increment by loop of

$$00_H \longrightarrow 53_H$$ for Y address.
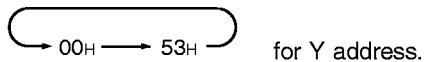
④ According to the setting-up of AIM, cooperative variation for X and Y addresses.

When the access of X address is made up to $0B_H$, Y address increment occurs.

• At REF = "0" (normal output)

$$00_H \longrightarrow 0B_H \longrightarrow 00_H \longrightarrow 01_H$$
$$00_H \longrightarrow 0B_H \longrightarrow 01_H \longrightarrow 02_H$$
$$\vdots$$
$$00_H \longrightarrow 0B_H \longrightarrow 52_H \longrightarrow 53_H$$
$$00_H \longrightarrow 0B_H \longrightarrow 53_H \longrightarrow 00_H$$
(X address)   (Y address)
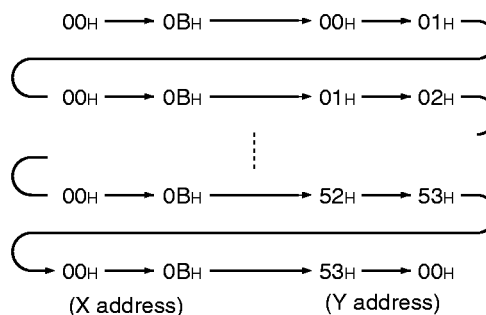
vary in the above loops.

• At REF = "1" (reverse output)

$$0B_H \longrightarrow 00_H \longrightarrow 00_H \longrightarrow 01_H$$
$$0B_H \longrightarrow 00_H \longrightarrow 01_H \longrightarrow 02_H$$
$$\vdots$$
$$0B_H \longrightarrow 00_H \longrightarrow 52_H \longrightarrow 53_H$$
$$0B_H \longrightarrow 00_H \longrightarrow 53_H \longrightarrow 00_H$$
(X address)   (Y address)
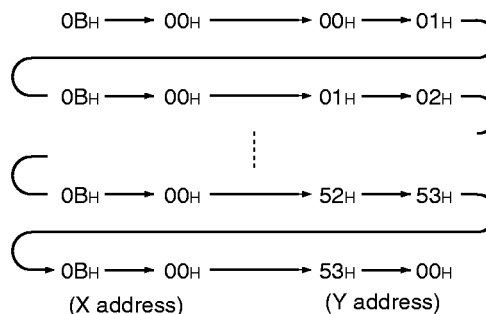
vary in the above loops.

4.12. Power Control (1) Register Set

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
1	0	1	1	EXA	HALT	PON	ACL		0	1	0	1	0

(At the time of reset : (EXA, HALT, PON, ACL) = 0H, read address : BH)

(1) ACL Command

The internal circuit can be initialized. This command is enabled only at master operation mode.

ACL = "0" : Normal operation

ACL = "1" : Initialization ON

If the power control register is read out immediately after executing ACL command (ACL = 1), the D0 bit is in the state of "1".

Therefore, if the reset operation is internally started, the D0 bit becomes "0".

In executing ACL command, the internal reset signals are internally generated by using display master clock (oscillation by OSCI and OSCO, or clock input at CK pin).

Therefore, after executing ACL command, allow a waiting period having at least a two-cycle portion of the master clock before the next processing is made.

(2) PON Command

The internal power supply circuit is set ON/OFF.

PON = "0" : Power supply circuit OFF

PON = "1" : Power supply circuit ON

At PON = "1", the booster circuit and voltage converter function.

In accordance with the setting conditions of PMODE pin, the operation circuit part changes. See Table in Section 2.16. for details.

(3) HALT Command

The conditions of power-saving are set ON/OFF by this command.

HALT = "0" : Normal operation

HALT = "1" : Power-saving operation

When setting in the power-saving state, the supply current can be reduced to a value near to that of the standby current.

The internal conditions at power-saving are as follows.

(a) The oscillation circuit and power supply circuit are stopped.

(b) The LCD drive is stopped, and outputs of the segment driver and common driver are Vss level.

(c) The clock input from CK pin is inhibited.

(d) The contents of display RAM data are maintained.

(e) The operation mode maintains the command execution state before executing power-saving command.

(4) EXA Command

Clock for icon display external/internal

EXA = "0" : Internal clock

EXA = "1" : External clock from EXA pin

4.13. Electronic Volume Register Set

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
1	1	0	1	DVL3	DVL2	DVL1	DVL0		0	1	0	1	0

(At the time of reset : (DVL3 to DVL0) = F_H, read address : B_H)

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
1	1	0	1	*	*	*	DVL4		0	1	0	1	1

* mark means "Don't care".

(At the time of reset : (DVL4) = 1_H, read address : D_H)

The LCD drive voltage V0 output from the internal power supply circuit can be controlled and the display tone on the LCD can be also controlled.
The LCD drive voltage V0 takes one out of 32 voltage values by setting a 5-bit data register.
If the electronic volume is not used, specify (1, 1, 1, 1, 1) in the 5-bit data register, and V_{R1} and V_{R2} pins are shorted. After the LH155L is reset, the 5-bit data register is automatically set to (1, 1, 1, 1, 1).

DVL4	DVL3	DVL2	DVL1	DVL0	V0
0	0	0	0	0	Smaller
1	1	1	1	1	Larger

4.14. Power Control (2) Register Set

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
1	1	1	0	*	DU0	BS1	BS0		0	1	0	1	0

* mark means "Don't care".

(At the time of reset : (DU0, BS1, BS0) = 0_H, read address : E_H)

(1) BS Command
Command for bias setting. Setting BS1 or BS0, the bias ratio 1/7, 1/8 or 1/9 is selectable.

BS1	BS0	BIAS RATIO
0	0	1/9
0	1	1/8
1	0	1/7
1	1	Prohibition

(2) DUTY Command
Command for duty setting. Select duty ratio below.

DU0	DUTY RATIO
0	1/73
1	1/49

4.15. RE Register Set

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
1	1	1	1	*	*	TEST	RE		0	1	0	1	0/1

* mark means "Don't care".
(At the time of reset : (RE) = 0H, read address : FH)

Command for RE flag setting.
Do not use TEST command, because this command
is for IC testing.

4.16. Address Set for Internal Register Read

D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
1	1	0	0	RA3	RA2	RA1	RA0		0	1	0	1	0

(At the time of reset : (RA3, RA2, RA1, RA0) = CH)

When data set up in the internal registers are read out, set the read address allotted to each register by this command before executing the read command of the internal registers.
For example, when the data of the command register in the display control (1) are read out, set the values of (RA3, RA2, RA1 and RA0) = 8H.
Refer to the functional description of each command or the list of commands for the read address allotted to each command register.

4.17. Internal Register Read

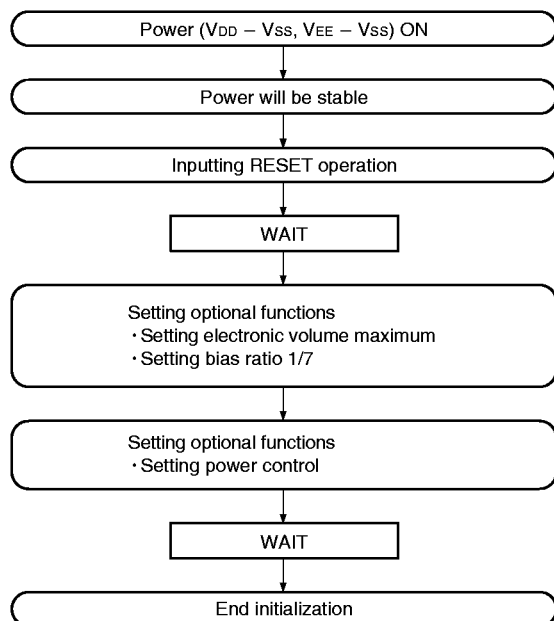| D7	D6	D5	D4	D3	D2	D1	D0		CSB	RS	WRB	RDB	RE
*	*	*	*	Internal Register Read Data					0	1	1	0	0

* mark means "Don't care".

Command for reading out the data of the internal
registers. When this command is executed, the
read address in the internal registers to be read
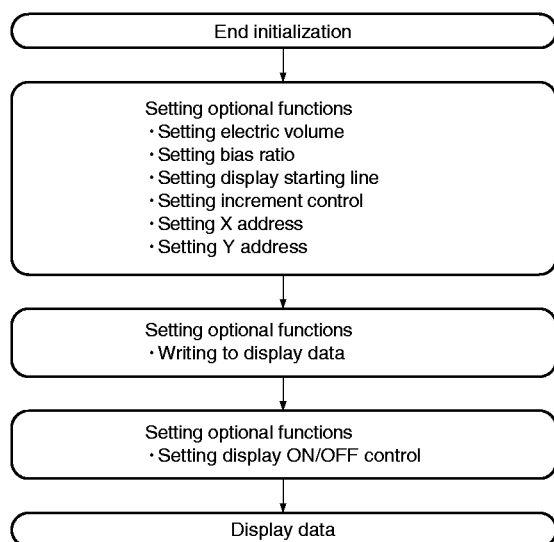must be preset.

4.18. Example of Setting Commands
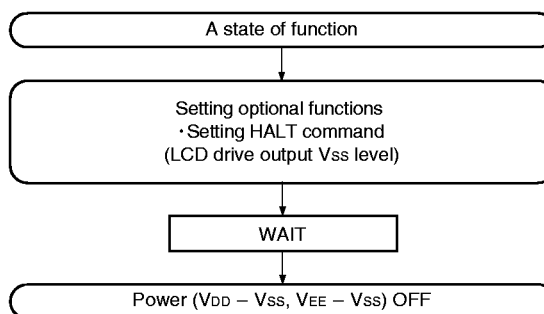
(1) Initialization

```
╭─────────────────────────────────────────╮
│  Power (VDD − Vss, VEE − Vss) ON          │
╰─────────────────────────────────────────╯
                    │
╭─────────────────────────────────────────╮
│        Power will be stable               │
╰─────────────────────────────────────────╯
                    │
╭─────────────────────────────────────────╮
│      Inputting RESET operation            │
╰─────────────────────────────────────────╯
                    │
┌─────────────────────────┐
│          WAIT            │
└─────────────────────────┘
                    │
╭─────────────────────────────────────────╮
│  Setting optional functions               │
│  · Setting electronic volume maximum      │
│  · Setting bias ratio 1/7                 │
╰─────────────────────────────────────────╯
                    │
╭─────────────────────────────────────────╮
│  Setting optional functions               │
│  · Setting power control                  │
╰─────────────────────────────────────────╯
                    │
┌─────────────────────────┐
│          WAIT            │
└─────────────────────────┘
                    │
╭─────────────────────────────────────────╮
│         End initialization                │
╰─────────────────────────────────────────╯
```

If V_{DD} and V_{EE} voltages are not same, connect the logic system power supply (V_{DD}) first.

(2) Display Data

```
╭─────────────────────────────────────────╮
│         End initialization                │
╰─────────────────────────────────────────╯
                    │
╭─────────────────────────────────────────╮
│  Setting optional functions               │
│  · Setting electric volume                │
│  · Setting bias ratio                     │
│  · Setting display starting line          │
│  · Setting increment control              │
│  · Setting X address                      │
│  · Setting Y address                      │
╰─────────────────────────────────────────╯
                    │
╭─────────────────────────────────────────╮
│  Setting optional functions               │
│  · Writing to display data                │
╰─────────────────────────────────────────╯
                    │
╭─────────────────────────────────────────╮
│  Setting optional functions               │
│  · Setting display ON/OFF control         │
╰─────────────────────────────────────────╯
                    │
╭─────────────────────────────────────────╮
│           Display data                    │
╰─────────────────────────────────────────╯
```

(3) Power OFF

```
╭─────────────────────────────────────────╮
│        A state of function                │
╰─────────────────────────────────────────╯
                    │
╭─────────────────────────────────────────╮
│  Setting optional functions               │
│  · Setting HALT command                   │
│  (LCD drive output Vss level)             │
╰─────────────────────────────────────────╯
                    │
┌─────────────────────────┐
│          WAIT            │
└─────────────────────────┘
                    │
╭─────────────────────────────────────────╮
│  Power (VDD − Vss, VEE − Vss) OFF         │
╰─────────────────────────────────────────╯
```

If V_{DD} and V_{EE} voltages are not same, disconnect the booster circuit power supply (V_{EE}) first. After V_{EE}, V_{OUT}, V_0, V_1, V_2, V_3 and V_4 voltages are below LCD ON voltage (threshold voltage for liquid crystal turns on), disconnect the logic system power supply (V_{DD}).

5. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3 to $+4.0$	V	
Supply voltage (2)	V_{EE}	V_{EE}	-0.3 to $+4.0$	V	
Supply voltage (3)	V_{OUT}	V_{OUT}	-0.3 to $+16.0$	V	
Supply voltage (4)	V_{R1}, V_{R2}	V_{R1}, V_{R2}	-0.3 to $+16.0$	V	
Supply voltage (5)	V_0	V_0	-0.3 to $+16.0$	V	1, 2
Supply voltage (6)	$V_1, V_2,$ V_3, V_4	V_1, V_2, V_3, V_4	-0.3 to $V_0 + 0.3$	V	
Input voltage	V_I	D_7-D_0, CSB, RS, M/S, M86, RDB, WRB, CK, CKS, OSCI, LP, FLM, M, SDA, SCL, P/S, RESB, EXA, PMODE, TEST	-0.3 to $V_{DD} + 0.3$	V	
Storage temperature	T_{STG}		-45 to $+125$	$^\circ$C	

NOTES :

1. $T_A = +25$ $^\circ$C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

6. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{DD}	V_{DD}	$+1.8$		$+3.3$	V	1
	V_{EE}	V_{EE}	$+2.4$		$+3.3$	V	2
Operating voltage	V_0	V_0	$+5.0$		$+15.5$	V	3
	V_{OUT}	V_{OUT}			$+15.5$	V	
	V_{R1}, V_{R2}	V_{R1}, V_{R2}	$+5.0$		$+15.5$	V	4
Operating temperature	T_{OPR}		-30		$+85$	$^\circ$C	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. When using the booster circuit, power supply, V_{EE} at the primary circuit must be used within the above-described range. If the drive voltage of LCD panel can be boosted by utilizing the voltage level of V_{DD}, usually connect this pin to V_{DD} power supply.
3. Ensure that voltages are set such that $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$.
4. The operating range is adjusted by the external circuit constructed between V_{OUT} and V_{R1}, V_{R2}. The electric potential relation between the V_{R1}, V_{R2} and V_{OUT} pins must be $V_{R2} \leq V_{R1} \leq V_{OUT}$.

7. ELECTRICAL CHARACTERISTICS

7.1. DC Characteristics

(Unless otherwise specified, V_{SS} = 0 V, V_{DD} = +1.8 to +3.3 V, T_{OPR} = −30 to +85 °C)

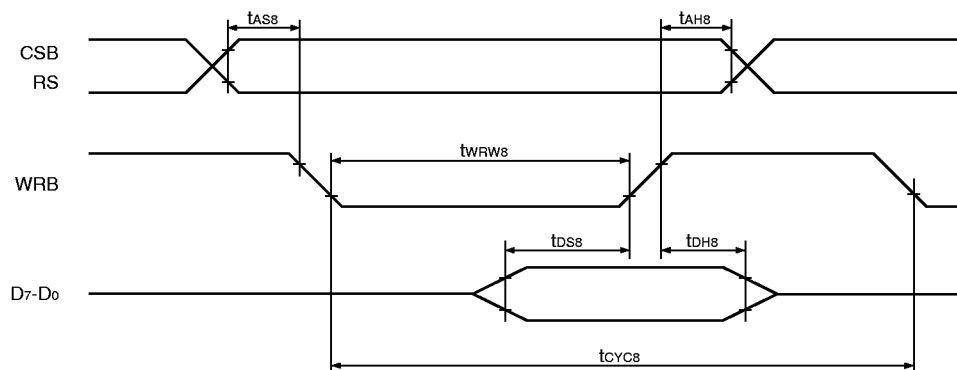| PARAMETER	SYMBOL	CONDITIONS		APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}			D_7-D_0, CSB, RS, M/S, M86, RDB, WRB, CK, CKS, OSCI,	0		$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}			LP, FLM, M, SDA, SCL, P/S, RESB, EXA, PMODE	$0.8V_{DD}$		V_{DD}	V	
Output "Low" voltage	V_{OL}	I_{OL} = 0.4 mA		D_7-D_0, LP, FLM, M			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.4 mA			V_{DD} − 0.4			V	
Input leakage current	I_{LI}	V_I = V_{SS} or V_{DD}		CSB, RS, M/S, M86, RDB, WRB, CK, CKS, OSCI, SDA, SCL, P/S, RESB, EXA, PMODE	−10		10	µA	
Output leakage current	I_{LO}	V_I = V_{SS} or V_{DD}		D_7-D_0, LP, FLM, M	−10		10	µA	1
LCD drive output ON resistance	R_{ON}	|ΔV_{ON}| = 0.5 V	V_0 = 10 V	SEG0-SEG95, COM0-COM71, COMI			4	kΩ	2
			V_0 = 6 V				6		
Standby current	I_{STB}	CK = 0 V	V_{DD} = 3 V	V_{DD}			10	µA	3
		CS = V_{DD}	V_{DD} = 2 V				5		
Supply current (1)	I_{DD1}	During sleep mode	V_{DD} = 3 V	V_{DD}			10	µA	4
			V_{DD} = 2 V				5		
Supply current (2)	I_{DD2}	During hold mode	V_{DD} = 3 V	V_{DD}, V_{EE}			300	µA	5
			V_{DD} = 2 V				200		
Supply current (3)	I_{DD3}	During active mode	V_{DD} = 3 V	V_{DD}			300	µA	6
		f_{CYC} = 100 kHz	V_{DD} = 2 V				200		
Oscillation frequency	f_{OSC}	R_F = 2.0 MΩ±2%	V_{DD} = 3 V	OSCO		36		kHz	7
			V_{DD} = 2 V			30			
Reset ("L") pulse width	t_{RW}			RESB	10			µs	

NOTES :

1. Applied when D_7 to D_0, LP, FLM, and M are in the high impedance state.
2. Resistance when 0.5 V is applied between each output pin and each power supply (V_0, V_1, V_2, V_3, V_4). Applied when power is supplied at power bias ratio of 1/9 in the external power supply mode.
3. Current at the V_{DD} pin when the master clock stops, the chip is not selected (CSB = V_{DD}), and no load is used. All circuits stop.
4. Sleep mode supply current.
   Stops internal oscillation clock, using external EXA signal. Without using booster circuits. Display OFF.
   ICON display ON. No load.

5. Applied when no access is made by the MPU when the internal oscillation circuit (R_F = 2.0 MΩ) and power supply circuit (PMODE = "L") are used. Boosting five times is used. The electronic volume is preset (the code is "1 1 1 1 1").
   The display is OFF and the LCD drive pin is not loaded.
   Measuring conditions : V_{DD} = V_{EE}, V_{R1} = V_{R2}, C_1 = C_2 = 2.2 µF, R_1 + R_2 + R_3 = 4 MΩ.
6. Active mode supply current.
   Using internal oscillation clock.
   Writing at f_{CYC} the graphic display data which are reversed every one bit. No load.
7. Oscillation frequency when connecting a feedback resistor (R_F) of 2.0 MΩ between OSCI and OSCO.

7.2. AC Characteristics
7.2.1. SYSTEM BUS READ/WRITE TIMING (80-FAMILY MPU)

(Write Timing)

(80-family Write Timing Characteristics)   (V_{DD} = 2.7 to 3.3 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH8}		CSB	30		ns
Address setup time	t_{AS8}		RS	0		ns
System cycle time	t_{CYC8}		WRB	220		ns
Write pulse width	t_{WRW8}			100		ns
Data setup time	t_{DS8}		D7-D0	70		ns
Data hold time	t_{DH8}			30		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 2.4 to 2.7 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH8}		CSB	30		ns
Address setup time	t_{AS8}		RS	0		ns
System cycle time	t_{CYC8}		WRB	300		ns
Write pulse width	t_{WRW8}			150		ns
Data setup time	t_{DS8}		D7-D0	100		ns
Data hold time	t_{DH8}			30		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

(V_{DD} = 1.8 to 2.4 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH8}		CSB	50		ns
Address setup time	t_{AS8}		RS	20		ns
System cycle time	t_{CYC8}		WRB	500		ns
Write pulse width	t_{WRW8}			200		ns
Data setup time	t_{DS8}		D7-D0	150		ns
Data hold time	t_{DH8}			50		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

(Read Timing)

(80-family Read Timing Characteristics)   (V$_{DD}$ = 2.7 to 3.3 V, T$_{OPR}$ = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t$_{AH8}$		CSB	30		ns
Address setup time	t$_{AS8}$		RS	0		ns
System cycle time	t$_{CYC8}$		RDB	400		ns
Read pulse width	t$_{RDW8}$			200		ns
Read data output delay	t$_{RDD8}$	C$_L$ = 15 pF	D$_7$-D$_0$		170	ns
Read data hold time	t$_{RDH8}$			10		ns
Input signal rise and fall time	t$_R$, t$_F$		All of above pins		15	ns

(V$_{DD}$ = 2.4 to 2.7 V, T$_{OPR}$ = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t$_{AH8}$		CSB	30		ns
Address setup time	t$_{AS8}$		RS	0		ns
System cycle time	t$_{CYC8}$		RDB	600		ns
Read pulse width	t$_{RDW8}$			300		ns
Read data output delay	t$_{RDD8}$	C$_L$ = 15 pF	D$_7$-D$_0$		250	ns
Read data hold time	t$_{RDH8}$			10		ns
Input signal rise and fall time	t$_R$, t$_F$		All of above pins		30	ns

(V$_{DD}$ = 1.8 to 2.4 V, T$_{OPR}$ = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t$_{AH8}$		CSB	50		ns
Address setup time	t$_{AS8}$		RS	20		ns
System cycle time	t$_{CYC8}$		RDB	800		ns
Read pulse width	t$_{RDW8}$			400		ns
Read data output delay	t$_{RDD8}$	C$_L$ = 15 pF	D$_7$-D$_0$		350	ns
Read data hold time	t$_{RDH8}$			10		ns
Input signal rise and fall time	t$_R$, t$_F$		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V$_{DD}$ voltage.

7.2.2. SYSTEM BUS READ/WRITE TIMING (68-FAMILY MPU)

(Write Timing)

(68-family Write Timing Characteristics)   (V_{DD} = 2.7 to 3.3 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	30		ns
Address setup time	t_{AS6}		RS	0		ns
System cycle time	t_{CYC6}		E	220		ns
Enable pulse width	t_{EW6}			100		ns
Data setup time	t_{DS6}		D7-D0	70		ns
Data hold time	t_{DH6}			30		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 2.4 to 2.7 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	30		ns
Address setup time	t_{AS6}		RS	0		ns
System cycle time	t_{CYC6}		E	300		ns
Enable pulse width	t_{EW6}			150		ns
Data setup time	t_{DS6}		D7-D0	100		ns
Data hold time	t_{DH6}			30		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

(V_{DD} = 1.8 to 2.4 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	50		ns
Address setup time	t_{AS6}		RS	20		ns
System cycle time	t_{CYC6}		E	500		ns
Enable pulse width	t_{EW6}			200		ns
Data setup time	t_{DS6}		D7-D0	150		ns
Data hold time	t_{DH6}			50		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

(Read Timing)

(68-family Read Timing Characteristics)　　　　　　　　　　$(V_{DD} = 2.7$ to 3.3 V, $T_{OPR} = -30$ to $+85$ °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	30		ns
Address setup time	t_{AS6}		RS	0		ns
System cycle time	t_{CYC6}		E	400		ns
Enable pulse width	t_{EW6}		E	200		ns
Read data output delay	t_{RDD6}	$C_L = 15$ pF	D_7-D_0		170	ns
Read data hold time	t_{RDH6}	$C_L = 15$ pF	D_7-D_0	10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

$(V_{DD} = 2.4$ to 2.7 V, $T_{OPR} = -30$ to $+85$ °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	30		ns
Address setup time	t_{AS6}		RS	0		ns
System cycle time	t_{CYC6}		E	600		ns
Enable pulse width	t_{EW6}		E	300		ns
Read data output delay	t_{RDD6}	$C_L = 15$ pF	D_7-D_0		250	ns
Read data hold time	t_{RDH6}	$C_L = 15$ pF	D_7-D_0	10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

$(V_{DD} = 1.8$ to 2.4 V, $T_{OPR} = -30$ to $+85$ °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	50		ns
Address setup time	t_{AS6}		RS	20		ns
System cycle time	t_{CYC6}		E	800		ns
Enable pulse width	t_{EW6}		E	400		ns
Read data output delay	t_{RDD6}	$C_L = 15$ pF	D_7-D_0		350	ns
Read data hold time	t_{RDH6}	$C_L = 15$ pF	D_7-D_0	10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

7.2.3. SERIAL INTERFACE TIMING
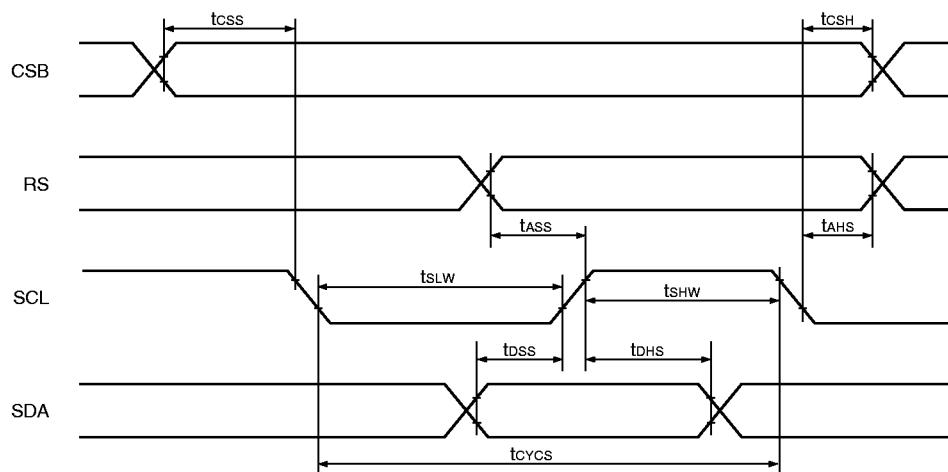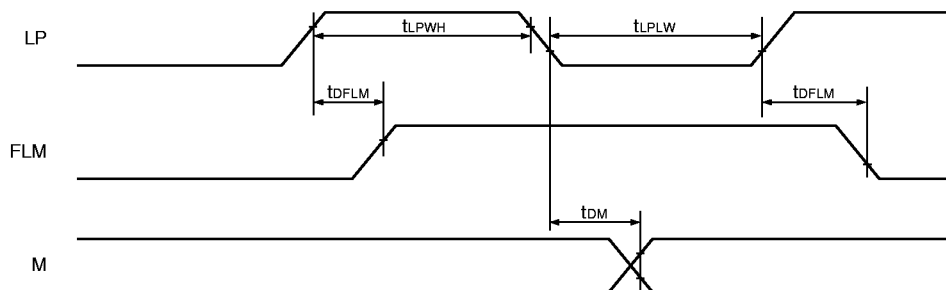

(V$_{DD}$ = 2.4 to 3.3 V, T$_{OPR}$ = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Serial clock period	t$_{CYCS}$			1 000		ns
SCL "H" pulse width	t$_{SHW}$		SCL	400		ns
SCL "L" pulse width	t$_{SLW}$			400		ns
Address setup time	t$_{ASS}$		RS	80		ns
Address hold time	t$_{AHS}$			80		ns
Data set up time	t$_{DSS}$		SDA	400		ns
Data hold time	t$_{DHS}$			400		ns
CSB to SCL time	t$_{CSS}$		CSB	80		ns
CSB hold time	t$_{CSH}$			80		ns
Input signal rise and fall time	t$_R$, t$_F$		All of above pins		30	ns

(V$_{DD}$ = 1.8 to 2.4 V, T$_{OPR}$ = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Serial clock period	t$_{CYCS}$			2 000		ns
SCL "H" pulse width	t$_{SHW}$		SCL	800		ns
SCL "L" pulse width	t$_{SLW}$			800		ns
Address setup time	t$_{ASS}$		RS	160		ns
Address hold time	t$_{AHS}$			160		ns
Data set up time	t$_{DSS}$		SDA	800		ns
Data hold time	t$_{DHS}$			800		ns
CSB to SCL time	t$_{CSS}$		CSB	160		ns
CSB hold time	t$_{CSH}$			160		ns
Input signal rise and fall time	t$_R$, t$_F$		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V$_{DD}$ voltage.

7.2.4. DISPLAY CONTROL TIMING

Input Timing Characteristics (Slave Mode)   (V_{DD} = 2.4 to 3.3 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
LP "H" pulse width	t_{LPHW}		LP	80		µs
LP "L" pulse width	t_{LPLW}			80		µs
FLM delay time	t_{DFLM}		FLM	−1.0	1.0	µs
M delay time	t_{DM}		M	−1.0	1.0	µs
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 1.8 to 2.4 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
LP "H" pulse width	t_{LPHW}		LP	80		µs
LP "L" pulse width	t_{LPLW}			80		µs
FLM delay time	t_{DFLM}		FLM	−1.0	1.0	µs
M delay time	t_{DM}		M	−1.0	1.0	µs
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

Output Timing Characteristics (Master Mode)   (V_{DD} = 2.4 to 3.3 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
FLM delay time	t_{DFLM}	C_L = 15 pF	FLM	10	1 000	ns
M delay time	t_{DM}		M	10	1 000	ns

(V_{DD} = 1.8 to 2.4 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
FLM delay time	t_{DFLM}	C_L = 15 pF	FLM	10	2 000	ns
M delay time	t_{DM}		M	10	2 000	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

7.2.5. MASTER CLOCK INPUT TIMING
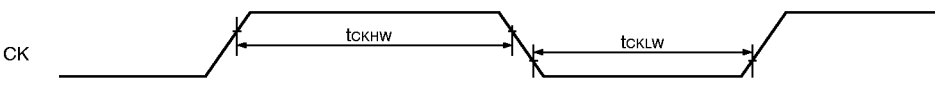
$(V_{DD} = 2.4$ to 3.3 V, $T_{OPR} = -30$ to $+85$ °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PIN	MIN.	MAX.	UNIT
CK "H" pulse width	t_{CKHW}			10	32	μs
CK "L" pulse width	t_{CKLW}		CK	10	32	μs
Input signal rise and fall time	t_R, t_F				15	ns

$(V_{DD} = 1.8$ to 2.4 V, $T_{OPR} = -30$ to $+85$ °C)

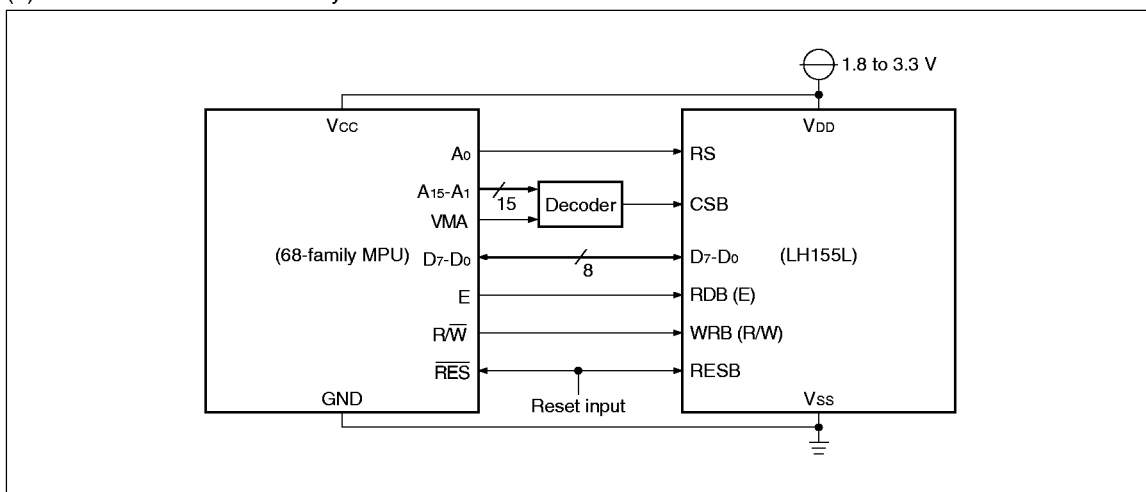| PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PIN	MIN.	MAX.	UNIT
CK "H" pulse width	t_{CKHW}			10	32	μs
CK "L" pulse width	t_{CKLW}		CK	10	32	μs
Input signal rise and fall time	t_R, t_F				30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

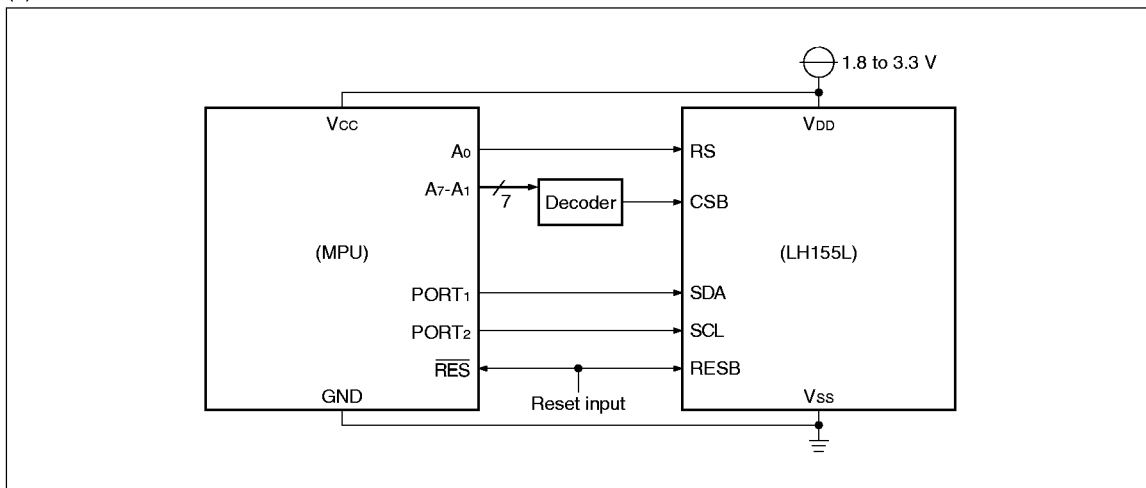## 8. CONNECTION EXAMPLES OF REPRESENTATIVE APPLICATIONS

(a) Connection to The 80-family MPU
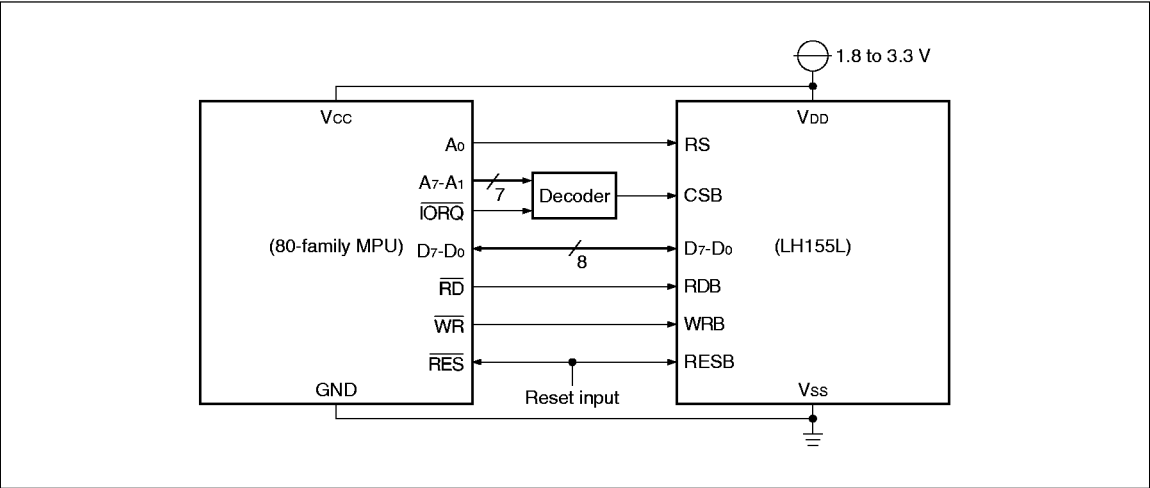
(b) Connection to The 68-family MPU

(c) Connection to The MPU with Serial Interface

∗ When connecting multiple LH155Ls, input to each CSB pin by varying the decoder conditions of address signals.

9. PACKAGE   (Unit : mm)

UPILEX is a trademark of UBE INDUSTRIES, LTD..

LH155LF