440GR

Preliminary Data Sheet

Power PC 440GR Embedded Processor

Features

- PowerPC® 440 processor core operating up to 667MHz with 32KB I-cache and D-cache with parity checking.
- Selectable processor:bus clock ratios of N:1, N:2.
- Dual bridged Processor Local Buses (PLBs) with 64- and 128-bit widths.
- Double Data Rate (DDR) Synchronous DRAM (SDRAM) interface operating up to 133MHz with ECC.
- DMA support for external peripherals, internal UART and memory.
- PCI V2.2 interface (3.3V only). Thirty-two bits at up to 66MHz.
- Programmable interrupt controller supports interrupts from a variety of sources.
- Programmable General Purpose Timers (GPT).
- Two Ethernet 10/100Mbps half- or full-duplex interfaces. Operational modes supported are MII, RMII, and SMII with packet reject.
- Up to four serial ports (16750 compatible UART).
- External peripheral bus (16-bit data) for up to six devices with external mastering.
- Two IIC interfaces (one with boot parameter read capability).
- NAND Flash interface.
- SPI interface.
- General Purpose I/O (GPIO) interface.
- JTAG interface for board level testing.
- Boot from PCI memory, NOR Flash on the extrenal peripheral bus, or NAND Flash on the NAND Flash interface.
- Available in RoHS compliant lead-free package.

Description

Designed specifically to address high-end embedded applications, the PowerPC 440GR (PPC440GR) provides a high-performance, low- power solution that interfaces to a wide range of peripherals and incorporates on-chip power management features.

This chip contains a high-performance RISC processor, DDR SDRAM controller, PCI bus interface, control for external ROM and peripherals, DMA with scatter-gather support, Ethernet ports, serial ports, IIC interfaces, SPI interface, NAND Flash interface, and general purpose I/O.

Technology: CMOS Cu-11, 0.13µm.

Package: 35mm, 456-ball enhanced plastic ball grid array (E-PBGA).

Typical power (estimated): Less than 2.5W at 533MHz, 2.3W at 400MHz.

Supply voltages required: 3.3V, 2.5V, 1.5V.

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Ordering and PVR Information

For information on the availability of the following parts, contact your local AMCC sales office.

Product Name	Order Part Number (see **Notes:**)	Package	Revision Level	PVR Value	JTAG ID
PPC440GR	PPC440GR-3pbfffCx	35mm, 456 ball, PBGA	A	0x422218D3	0x2A950049
PPC440GR	PPC440GR-3pbfffCx	35mm, 456 ball, PBGA	B	0x422218D4	0x2A950049

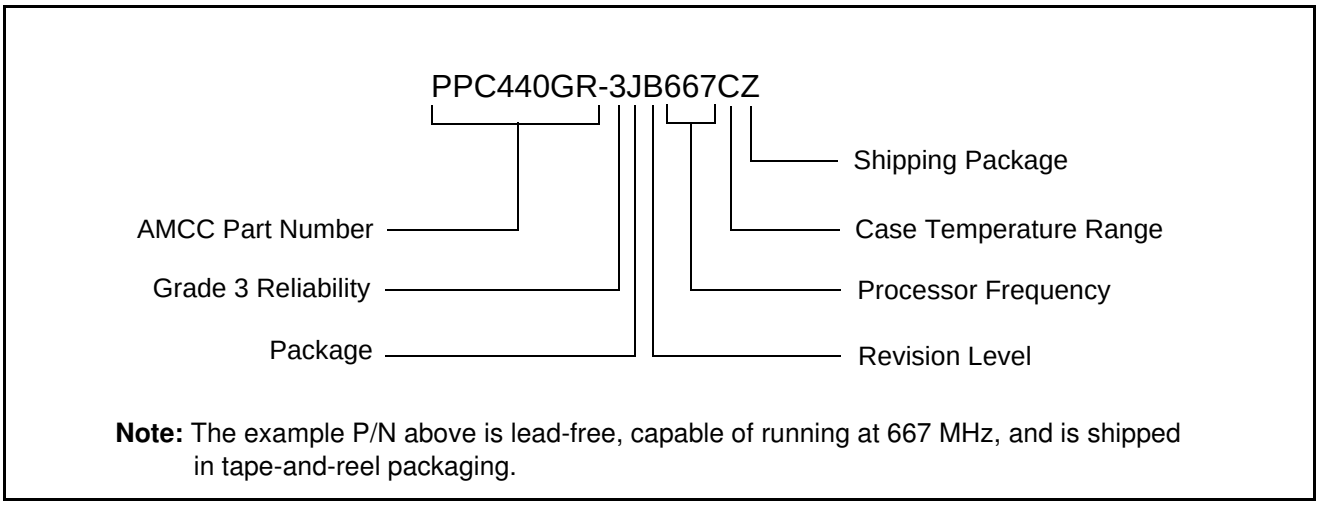
Notes:

1. p = Module Package type
   B = E-PBGA and contains lead.
   J = E-PBGA and is lead-free (RoHS compliant).
2. b = Chip revision level
   A = Revision level A (1.0)
   B = Revision level B (1.1)
3. fff = Processor frequency
   333 = 333MHz
   400 = 400MHz
   533 = 533MHz
   667 = 667MHz
4. C = Case temperature range:
   -40°C to +100°C for 333MHz, 400MHz, and 533MHz parts
   -40°C to +85°C for 667MHz parts
5. x = Shipping package type
   Z = tape-and-reel
   Blank = tray

Each part number contains a revision code. This is the die mask revision number and is included in the part number for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only). Refer to the *PPC440GR User's Manual* for details on accessing these registers.

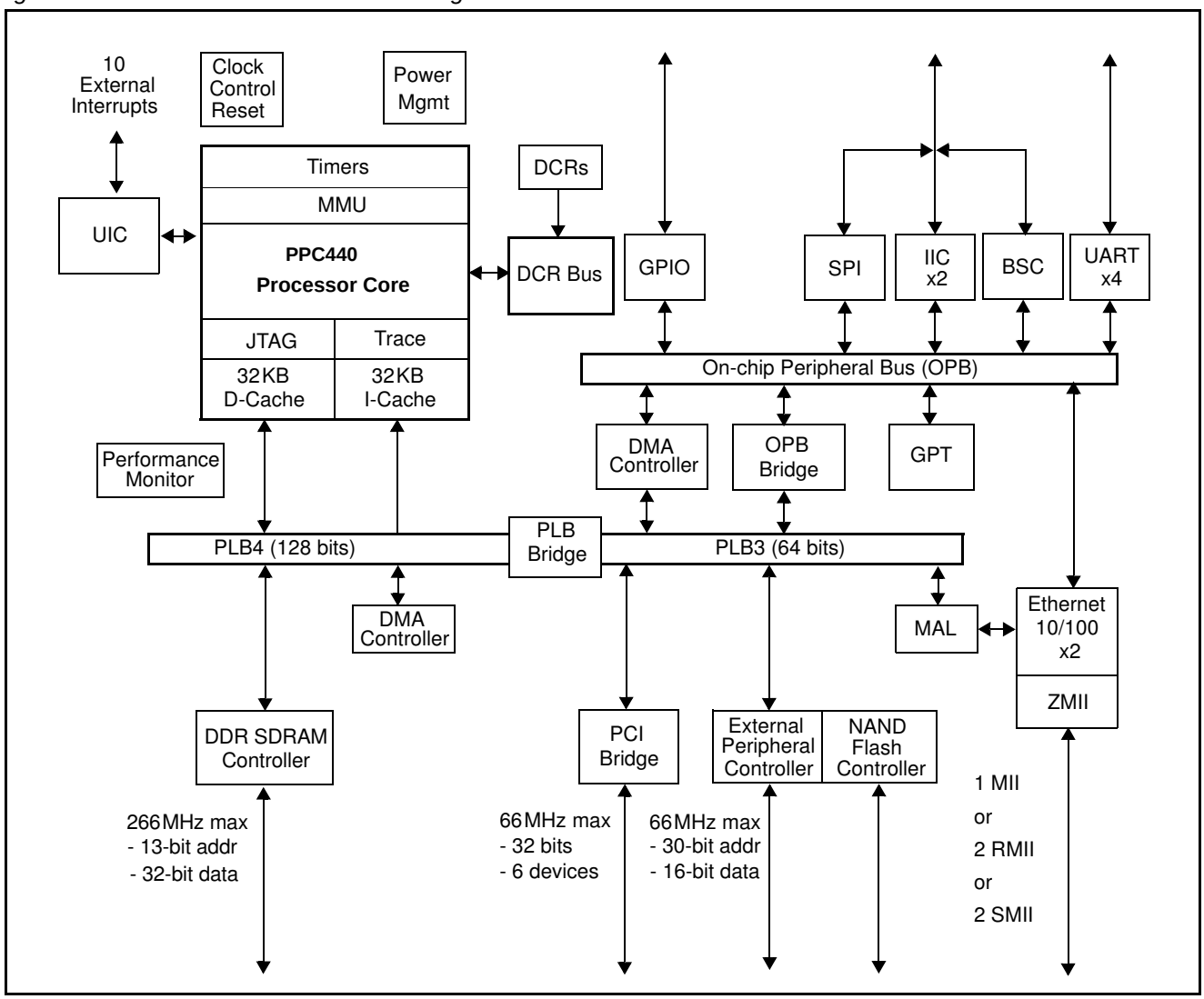
Figure 1. Order Part Number Key



Note: The example P/N above is lead-free, capable of running at 667 MHz, and is shipped in tape-and-reel packaging.

Block Diagram

Figure 2. PPC440GR Functional Block Diagram



The PPC440GR is a system on a chip (SOC) using IBM CoreConnect Bus™ Architecture.

Address Maps

The PPC440GR incorporates two address maps. The first is a fixed processor System Memory Address Map. This address map defines the possible contents of various address regions which the processor can access. The second is the DCR Address Map for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the PPC440GR processor through the use of **mtdcr** and **mfdcr** instructions.

Table 1. System Memory Address Map (Sheet 1 of 2)

Function	Sub Function	Start Address	End Address	Size
Local Memory[1]	DDR SDRAM	0 0000 0000	0 3FFF FFFF	1GB
	Reserved	0 4000 0000	0 7FFF FFFF	
EBC	EBC	0 8000 0000	0 9FFF FFFF	512MB
PCI	PCI Memory	0 A000 0000	0 DFFF FFFF	1GB
	Reserved	0 E000 0000	0 E7FF FFFF	
	PCI I/O	0 E800 0000	0 E800 FFFF	64KB
	Reserved	0 E801 0000	0 E87F FFFF	
	PCI I/O	0 E880 0000	0 EBFF FFFF	56MB
	Reserved	0 EC00 0000	0 EEBF FFFF	
	Configuration Registers	0 EEC0 0000	0 EEC0 0007	8B
	Reserved	0 EEC0 0008	0 EECF FFFF	
	PCI Interrupt Ack / Special Cycle	0 EED0 0000	0 EED0 0003	4B
	Reserved	0 EED0 0004	0 EF3F FFFF	
	Local Configuration Registers	0 EF40 0000	0 EF40 003F	64B
	Reserved	0 EF40 0040	0 EF4F FFFF	

Table 1. System Memory Address Map (Sheet 2 of 2)

Function	Sub Function	Start Address	End Address	Size
Internal Peripherals	Reserved	0 EF50 0000	0 EF5F FFFF	
	General Purpose Timer	0 EF60 0000	0 EF60 00FF	256B
	Reserved	0 EF60 0100	0 EF60 02FF	
	UART0	0 EF60 0300	0 EF60 0307	8B
	Reserved	0 EF60 0308	0 EF60 03FF	
	UART1	0 EF60 0400	0 EF60 0407	8B
	Reserved	0 EF60 0408	0 EF60 04FF	
	UART2	0 EF60 0500	0 EF60 0507	8B
	Reserved	0 EF60 0508	0 EF60 05FF	
	UART3	0 EF60 0600	0 EF60 0607	8B
	Reserved	0 EF60 0608	0 EF60 06FF	
	IIC0	0 EF60 0700	0 EF60 071F	32B
	Reserved	0 EF60 0720	0 EF60 07FF	
	IIC1	0 EF60 0800	0 EF60 081F	32B
	Reserved	0 EF60 0820	0 EF60 08FF	
	SPI	0 EF60 0900	0 EF60 0906	6B
	Reserved	0 EF60 0907	0 EF60 09FF	
	OPB Arbiter	0 EF60 0A00	0 EF60 0A3F	64B
	Reserved	0 EF60 0A40	0 EF60 0AFF	
	GPIO0 Controller	0 EF60 0B00	0 EF60 0B7F	128B
	Reserved	0 EF60 0B80	0 EF60 0BFF	
	GPIO1 Controller	0 EF60 0C00	0 EF60 0C7F	128B
	Reserved	0 EF60 0C80	0 EF60 0CFF	
	Ethernet PHY ZMII	0 EF60 0D00	0 EF60 0D0F	16B
	Reserved	0 EF60 0D10	0 EF60 0DFF	
	Ethernet 0 Controller	0 EF60 0E00	0 EF60 0EFF	256B
	Ethernet 1 Controller	0 EF60 0F00	0 EF60 0FFF	256B
	Reserved	0 EF60 1000	0 EFFF FFFF	
EBC		0 F000 0000	0 FFDF FFFF	254MB
Boot space (EBC Bank 0 and PCI)		0 FFE0 0000	0 FFFF FFFF	2MB

Notes:

1. DDR SDRAM can be located anywhere in the Local Memory area of the memory map.
2. EBC and PCI are relocatable, but this map reflects the suggested configuration.

Table 2. DCR Address Map (4KB of Device Configuration Registers)

Function	Start Address	End Address	Size
Total DCR Address Space[1]	000	3FF	1KW (4KB)[1]
By function:			
Reserved	000	00B	12W
Clocking Power On Reset	00C	00D	2W
System DCRs	00E	00F	2W
Memory Controller	010	011	2W
External Bus Controller	012	013	2W
Reserved	014	015	2W
PLB 128 Performance Monitor	016	017	2W
Reserved	018	01F	8W
PLB 128 to PLB 64 Bridge Out	020	02F	16W
PLB 64 to PLB 128 Bridge In	030	03F	16W
Reserved	040	06F	64W
PLB 64 Arbiter	070	08F	16W
PLB 128 Arbiter	080	08F	16W
PLB 64 to OPB Bridge Out	090	09F	16W
Reserved	0A0	0A7	8W
OPB to PLB 64 Bridge In	0A8	0AF	8W
Power Management	0B0	0B7	8W
Reserved	0B8	0BF	8W
Interrupt Controller 0	0C0	0CF	16W
Interrupt Controller 1	0D0	0DF	16W
Clock, Control, and Reset	0E0	0EF	16W
Reserved	0F0	0FF	16W
DMA to PLB 64 Controller	100	13F	64W
Reserved	140	17F	64W
Ethernet MAL	180	1FF	128W
Reserved	200	2FF	512W
DMA to PLB 128 Controller	300	33F	64W
Reserved	340	3FF	512W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register. One kiloword (1024W) equals 4KB (4096 B).

PowerPC 440 Processor Core

The PowerPC 440 processor core is designed for high-end applications: RAID controllers, SAN, iSCSI, routers, switches, printers, set-top boxes, etc. It implements the Book E PowerPC embedded architecture and uses the 128-bit version of IBM's on-chip CoreConnect Bus Architecture.

Features include:

- Up to 667 MHz operation
- PowerPC Book E architecture
- 32 KB I-cache, 32 KB D-cache
  - UTLB Word Wide parity on data and tag address parity with exception force
- Three logical regions in D-cache: locked, transient, normal
- D-cache full line flush capability
- 41-bit virtual address, 36-bit (64 GB) physical address
- Superscalar, out-of-order execution
- 7-stage pipeline
- 3 execution pipelines
- Dynamic branch prediction
- Memory management unit
  - 64-entry, full associative, unified TLB with optional parity
  - Separate instruction and data micro-TLBs
  - Storage attributes for write-through, cache-inhibited, guarded, and big or little endian
- Debug facilities
  - Multiple instruction and data range breakpoints
  - Data value compare
  - Single step, branch, and trap events
  - Non-invasive real-time trace interface
- 24 DSP instructions
  - Single cycle multiply and multiply-accumulate
  - 32 x 32 integer multiply
  - 16 x 16 -> 32-bit MAC

Internal Buses

The PowerPC 440GR features four standard on-chip buses: two Processor Local Buses (PLBs), one On-Chip Peripheral Bus (OPB), and the Device Control Register Bus (DCR). The high performance, high bandwidth cores such as the PowerPC 440 processor core, the DDR SDRAM memory controller, and the PCI bridge connect to the PLBs. The primary OPB hosts lower data rate peripherals. The daisy-chained DCR provides a lower bandwidth path for passing status and control information between the processor core and the other on-chip cores.

Features include:

- PLB 128 (PLB4)
  - 128-bit implementation of the PLB architecture
  - Separate and simultaneous read and write data paths
  - 36-bit address
  - Simultaneous control, address, and data phases
  - Four levels of pipelining
  - Byte-enable capability supporting unaligned transfers
  - 32- and 64-byte burst transfers
  - 133MHz, maximum 4.25GB/s (simultaneous read and write)
  - Processor:bus clock ratios of N:1 and N:2
- PLB 64 (PLB3)
  - 64-bit implementation of the PLB architecture
  - 32-bit address
  - 133MHz (1:1 ratio with PLB 128), maximum 1.1GB/s (no simultaneous read and write)
- OPB
  - 32-bit data path
  - 32-bit address
  - 66.66MHz
- DCR
  - 32-bit data path
  - 10-bit address

PCI Interface

The PCI interface allows connection of PCI devices to the PowerPC processor and local memory. This interface is designed to Version 2.2 of the PCI Specification and supports 32- bit PCI devices.

Reference Specifications:
- PowerPC CoreConnect Bus (PLB) Specification Version 3.1
- PCI Specification Version 2.2
- PCI Bus Power Management Interface Specification Version 1.1

Features include:
- PCI 2.2
  - Frequency to 66 MHz
  - 32-bit bus
- PCI Host Bus Bridge or an Adapter Device's PCI interface
- Internal PCI arbitration function, supporting up to six external devices, that can be disabled for use with an external arbiter
- Support for Message Signaled Interrupts
- Simple message passing capability
- Asynchronous to the PLB
- PCI Power Management 1.1
- PCI register set addressable both from on-chip processor and PCI device sides
- Ability to boot from PCI bus memory
- Error tracking/status
- Supports initiation of transfer to the following address spaces:
  - Single beat I/O reads and writes
  - Single beat and burst memory reads and writes
  - Single beat configuration reads and writes (type 0 and type 1)
  - Single beat special cycles

DDR SDRAM Memory Controller

The Double Data Rate (DDR) SDRAM memory controller supports industry standard discrete devices. Up to four 256 MB logical banks are supported in limited configurations. Global memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:
- Registered and non-registered industry standard discrete devices
- 32-bit memory interface with optional 8-bit ECC (SEC/DED)
- Sustainable 1.1 GB/s peak bandwidth at 133 MHz
- SSTL_2 logic
- 1 to 4 chip selects
- CAS latencies of 2, 2.5 and 3 supported
- DDR200/266 support
- Page mode accesses (up to eight open pages) with configurable paging policy
- Programmable address mapping and timing
- Hardware and software initiated self-refresh
- Power management (self-refresh, suspend, sleep)

External Peripheral Bus Controller (EBC)

Features include:
- Up to six ROM, EPROM, SRAM, Flash memory, and slave peripheral I/O banks supported
- Up to 66.66 MHz operation
- Burst and non-burst devices
- 16-bit byte-addressable data bus
- 30-bit address
- Peripheral Device pacing with external “Ready”
- Latch data on Ready, synchronous or asynchronous
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- External DMA Slave Support
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for own access and control

Ethernet Controller Interface

Ethernet support provided by the PPC440GR interfaces to the physical layer but the PHY is not included on the chip:
- One to two 10/100 interfaces running in full- and half-duplex modes
  - One full Media Independent Interface (MII) with 4-bit parallel data transfer
  - Two Reduced Media Independent Interfaces (RMII) with 2-bit parallel data transfer
  - Two Serial Media Independent Interfaces (SMII)
  - Packet reject support

DMA to PLB 64 Controller

This DMA controller provides a DMA interface between the OPB and the 64-bit PLB.

Features include:
- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 32-byte buffer
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 32-bit addressing
- Address increment or decrement
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

DMA to PLB 128 Controller

This DMA controller provides a DMA interface dedicated to the 128-bit PLB.

Features include:
- Support for memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers
- Scatter/gather capability
- 128-byte buffer with programmable thresholds

Serial Ports (UART)

Features include:
- Up to four ports in the following combinations:
  - One 8-pin
  - Two 4-pin
  - One 4-pin and two 2-pin
  - Four 2-pin
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16750 register set
- Complete status reporting capability
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA function on PLB 64

IIC Bus Interface

Features include:
- Two IIC interfaces provided
- Support for Philips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocols
- Programmable error recovery
- Includes an integrated boot-strap controller that is multiplexed with the second IIC interface

Serial Peripheral Interface (SPI/SCP)

The Serial Peripheral Interface (also known as the Serial Communications Port) is a full-duplex, synchronous, character-oriented (byte) port that allows the exchange of data with other serial devices. The SCP is a master on the serial port supporting a 3-wire interface (receive, transmit, and clock), and is a slave on the OPB.

Features include:
- Three-wire serial port interface
- Full-duplex synchronous operation
- SCP bus master
- OPB bus slave
- Programmable clock rate divider
- Clock inversion
- Reverse data
- Local data loop back for test

NAND Flash Controller

The NAND Flash controller provides a simple interface between the EBC and up to four separate external NAND Flash devices. It provides both direct command, address, and data access to the external device as well as a memory-mapped linear region that generates data accesses. NAND Flash device data appears on the peripheral data bus.

Features include:
- 1 to 4 banks supported on EBC
- Direct Interfacing to:
  - Discrete NAND Flash devices (up to 4 devices)
  - SmartMedia Card socket (22-pins)
- Device sizes 4MB–256MB supported
- (512 + 16)-B or (2K + 64)-B device page sizes supported
- Boot-from-NAND: Execute a linear sequence of boot code out of single page of first block (512B)
- Support DMA to allow direct, no-processor-intervention block copy from NAND Flash to SDRAM
- ECC provides single-bit error correction and double-bit error detection in each 256B of stored data
- Chip selects shared with EBC

General Purpose Timers (GPT)

Provides a separate time base counter and additional system timers in addition to those defined in the processor core.

Features include:
- 32-bit Time Base Counter driven by the OPB bus clock
- Seven 32-bit compare timers

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses.
- 64 GPIOs are multiplexed with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose.
- Each GPIO output is separately programmable to emulate an open drain driver (that is, drives to zero, tri-stated if output bit is 1).

Universal Interrupt Controller (UIC)

Two Universal Interrupt Controllers (UIC) are employed. They provide control, status, and communications necessary between the external and internal sources of interrupts and the on-chip PowerPC processor.

Note: Processor specific interrupts (for example, page faults) do not use UIC resources.

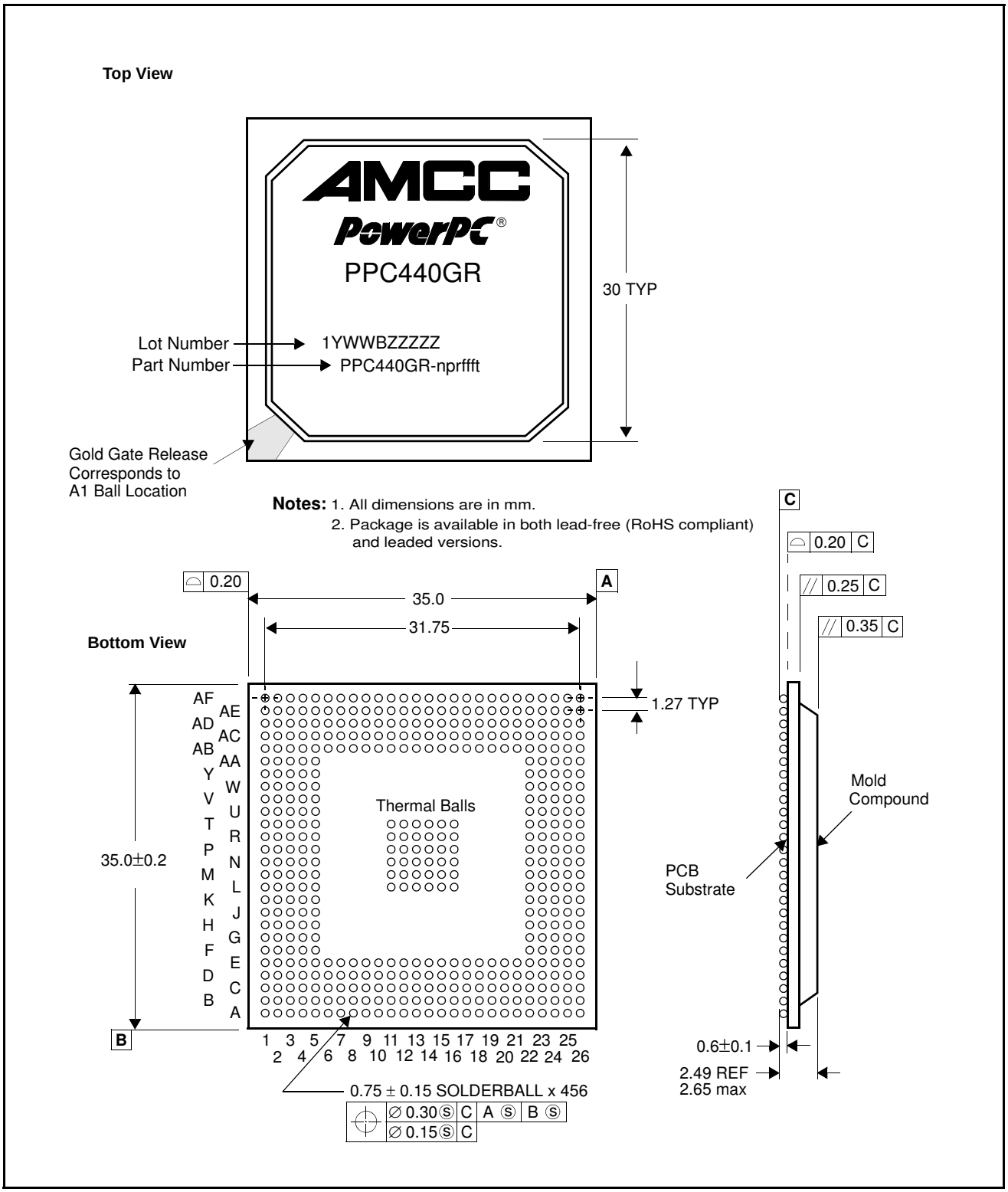
Features include:
- 10 external interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to the on-chip processor core
- Programmable interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

JTAG

Features include:
- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

Package Diagram

Figure 3. 35mm, 456-Ball E-PBGA Package



Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and alternate signals in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in "Signal Functional Description" on page 50 where the signals in the indicated interface group begin. In cases where signals in the same interface group (for example, Ethernet) have different names to distinguish variations in the mode of operation, the names are separated by a comma with the primary mode name appearing first. These signals are listed only once, and appear alphabetically by the primary mode name.

Table 3. Signals Listed Alphabetically (Sheet 1 of 24)

Signal Name	Ball	Interface Group	Page
AGND	AE17	Power	57
AV_{DD}	AD17		
BA0	AF03	DDR SDRAM	51
BA1	AF04		
$\overline{\text{BankSel0}}$	R04	DDR SDRAM	51
$\overline{\text{BankSel1}}$	R02		
$\overline{\text{BankSel2}}$	R01		
$\overline{\text{BankSel3}}$	N01		
BusReq[GPIO31]	AA23	External Master Peripheral	54
$\overline{\text{CAS}}$	J02	DDR SDRAM	51
ClkEn	AF05	DDR SDRAM	51
DM0	AE05	DDR SDRAM	51
DM1	AD07		
DM2	J01		
DM3	L03		
DM8	AF07		
[DMAAck0]IRQ8[GPIO47]	D18	External Slave Peripheral	53
[DMAAck1]IRQ4[GPIO44]	G25		
[DMAAck2]PerAddr06[GPIO01]	B06		
[DMAAck3]PerAddr03[GPIO04]	C07		
[DMAReq0]IRQ7[GPIO46]	B24	External Slave Peripheral	53
[DMAReq1]IRQ5[ModeCtrl]	AC12		
[DMAReq2]PerAddr07[GPIO00]	C08		
[DMAReq3]PerAddr04[GPIO03]	D08		
DQS0	AD09	DDR SDRAM	51
DQS1	AC08		
DQS2	K03		
DQS3	M04		
DQS8	AC06		
[DrvrInh1]RejectPkt	Y25	System	56
[DrvrInh2]$\overline{\text{Halt}}$	C25		

Table 3. Signals Listed Alphabetically (Sheet 2 of 24)

Signal Name	Ball	Interface Group	Page
ECC0	P02	DDR SDRAM	51
ECC1	N02		
ECC2	M01		
ECC3	M02		
ECC4	N03		
ECC5	N04		
ECC6	L02		
ECC7	M03		
EMCCD, EMC1RxErr[GPIO25][$\overline{\text{NFRdyBusy}}$]	AC16	Ethernet	52
EMCCrS, EMC0CrsDV[GPIO22]	AD15		
EMCDV, EMC1CrsDV[GPIO21][$\overline{\text{NFREn}}$]	AF17		
EMCMDClk	AE16		
EMCMDIO	AC18		
EMCRxClk	AF19		
EMCRxD0, EMC0RxD0, EMC0RxD[GPIO12]	AD19		
EMCRxD1, EMC0RxD1, EMC1RxD[GPIO13]	AE20		
EMCRxD2, EMC1RxD0[GPIO14]	AD18		
EMCRxD3, EMC1RxD1[GPIO15]	AC17		
EMCRxErr, EMC0RxErr[GPIO20]	AD16		
EMCTxClk, EMCRefClk	AC15		
EMCTxD0, EMC0TxD0, EMC0TxD[GPIO16]	AD14		
EMCTxD1, EMC0TxD1, EMC1TxD[GPIO17]	AF13		
EMCTxD2, EMC1TxD0[GPIO18][NFCLE]	AF14		
EMCTxD3, EMC1TxD1[GPIO19][NFALE]	AC14		
EMCTxEn, EMC0TxEn, EMCSync[GPIO24]	AF20		
EMCTxErr, EMC1TxEn[GPIO23][$\overline{\text{NFWEn}}$]	AF18		
[EOT0/TC0]IRQ9[GPIO48]	A19	External Slave Peripheral	53
[EOT1/TC1]IRQ6[GPIO45]	H23		
[EOT2/TC2]PerAddr05[GPIO02]	A05		
[EOT3/TC3]PerAddr02[GPIO05]	B04		
$\overline{\text{ExtAck}}$[GPIO30]	AA25	External Master Peripheral	54
$\overline{\text{ExtReq}}$[GPIO27]	AD26	External Master Peripheral	54
$\overline{\text{ExtReset}}$	B23	External Master Peripheral	54

Table 3. Signals Listed Alphabetically (Sheet 3 of 24)

Signal Name	Ball	Interface Group	Page
GND	A01		
GND	A02		
GND	A06		
GND	A09		
GND	A11		
GND	A16		
GND	A21		
GND	A26		
GND	B02		
GND	B25		
GND	B26		
GND	C03		
GND	C24		
GND	D04		
GND	D21		
GND	D23		
GND	E09	Power	57
GND	E14		
GND	E18		
GND	F01		
GND	F26		
GND	J05		
GND	J22		
GND	J26		
GND	L01		
GND	L04		
GND	L11		
GND	L13		
GND	L14		
GND	L16		
GND	L26		
GND	M12		
GND	M13		

Table 3. Signals Listed Alphabetically (Sheet 4 of 24)

Signal Name	Ball	Interface Group	Page
GND	M15		
GND	M25		
GND	N05		
GND	N11		
GND	N13		
GND	N14		
GND	N15		
GND	N16		
GND	P11		
GND	P12		
GND	P13		
GND	P14		
GND	P16		
GND	P22		
GND	R12		
GND	R14		
GND	R15		
GND	T01	Power	57
GND	T11		
GND	T13		
GND	T14		
GND	T16		
GND	T26		
GND	V05		
GND	V01		
GND	V22		
GND	AA01		
GND	AA26		
GND	AB09		
GND	AB13		
GND	AB18		
GND	AC01		
GND	AC04		
GND	AC07		
GND	AC23		

Table 3. Signals Listed Alphabetically (Sheet 5 of 24)

Signal Name	Ball	Interface Group	Page
GND	AD03	Power	57
GND	AD24		
GND	AE01		
GND	AE02		
GND	AE25		
GND	AF01		
GND	AF06		
GND	AF11		
GND	AF16		
GND	AF21		
GND	AF25		
GND	AF26		

Table 3. Signals Listed Alphabetically (Sheet 6 of 24)

Signal Name	Ball	Interface Group	Page
[GPIO00]PerAddr07[DMAReq2]	C08	System	56
[GPIO01]PerAddr06[DMAAck2]	B06		
[GPIO02]PerAddr05[EOT2/TC2]	A05		
[GPIO03]PerAddr04[DMAReq3]	D08		
[GPIO04]PerAddr03[DMAAck3]	C07		
[GPIO05]PerAddr02[EOT3/TC3]	B04		
[GPIO06]$\overline{\text{PerCS1}}$[$\overline{\text{NFCE1}}$]	C06		
[GPIO07]$\overline{\text{PerCS2}}$[$\overline{\text{NFCE2}}$]	A04		
[GPIO08]$\overline{\text{PerCS3}}$[$\overline{\text{NFCE3}}$]	B07		
[GPIO09]$\overline{\text{PerCS4}}$	B10		
[GPIO10]$\overline{\text{PerCS5}}$	A10		
[GPIO11]PerErr	E04		
[GPIO12]EMCRxD0, EMC0RxD0, EMC0RxD	AD19		
[GPIO13]EMCRxD1, EMC0RxD1, EMC1RxD	AE20		
[GPIO14]EMCRxD2, EMC1RxD0	AD18		
[GPIO15]EMCRxD3, EMC1RxD1	AC17		
[GPIO16]EMCTxD0, EMC0TxD0, EMC0TxD	AD14		
[GPIO17]EMCTxD1, EMC0TxD1, EMC1TxD	AF13		
[GPIO18]EMCTxD2, EMC1TxD0[NFCLE]	AF14		
[GPIO19]EMCTxD3, EMC1TxD1[NFALE]	AC14		
[GPIO20]EMCRxErr, EMC0RxErr	AD16		
[GPIO21]EMCDV, EMC1CrsDV[$\overline{\text{NFREn}}$]	AF17		
[GPIO22]EMCCrS, EMC0CrsDV	AD15		
[GPIO23]EMCTxErr, EMC1TxEn[$\overline{\text{NFWEn}}$]	AF18		
[GPIO24]EMCTxEn, EMC0TxEn, EMCSync	AF20		
[GPIO25]EMCCD, EMC1RxErr[$\overline{\text{NFRdyBusy}}$]	AC16		
GPIO26	AC26		
[GPIO27]$\overline{\text{ExtReq}}$	AD26		
GPIO28	Y24		
[GPIO29]HoldAck	AB25		
[GPIO30]$\overline{\text{ExtAck}}$	AA25		
[GPIO31]BusReq	AA23		

Table 3. Signals Listed Alphabetically (Sheet 7 of 24)

Signal Name	Ball	Interface Group	Page
GPIO32	W24	System	56
GPIO33	AB26		
[GPIO34]UART0_DCD/UART1_CTS/UART2_Tx	R25		
[GPIO35]UART0_DSR/UART1_RTS/UART2_Rx	U26		
[GPIO36]UART0_CTS/UART3_Rx	V26		
[GPIO37]UART0_RTS/UART3_Tx	R26		
[GPIO38]UART0_DTR/UART1_Tx	N24		
[GPIO39]UART0_RI/UART1_Rx	P24		
[GPIO40]IRQ0	D03		
[GPIO41]IRQ1	G04		
[GPIO42]IRQ2	F02		
[GPIO43]IRQ3	G02		
[GPIO44]IRQ4[DMAAck1]	G25		
[GPIO45]IRQ6[EOT1/TC1]	H23		
[GPIO46]IRQ7[DMAReq0]	B24		
[GPIO47]IRQ8[DMAAck0]	D18		
[GPIO48]IRQ9[EOT0/TC0]	A19		
[GPIO49]TrcBS0	AE21		
[GPIO50]TrcBS1	AC25		
[GPIO51]TrcBS2	AA24		
[GPIO52]TrcES0	Y03		
[GPIO53]TrcES1	AA04		
[GPIO54]TrcES2	AB03		
[GPIO55]TrcES3	AB04		
[GPIO56]TrcES4	AF22		
[GPIO57]TrcTS0	AC22		
[GPIO58]TrcTS1	AE24		
[GPIO59]TrcTS2	AD04		
[GPIO60]TrcTS3	AD06		
[GPIO61]TrcTS4	AC09		
[GPIO62]TrcTS5	AD12		
[GPIO63]TrcTS6	AE15		
Halt[DrvrInh2]	C25	System	56
HoldAck[GPIO29]	AB25	External Master Peripheral	54
HoldPri[LeakTest]	V24		
HoldReq[RcvrInh]	Y23		
IIC0SClk	U25	IIC0 Peripheral	54
IIC0SData	T24		

Table 3. Signals Listed Alphabetically (Sheet 8 of 24)

Signal Name	Ball	Interface Group	Page
[IIC1SClk]SCPClkOut	U24	IIC1 Peripheral	54
[IIC1SData]SCPDI	V25		
IRQ0[GPIO40]	D03	Interrupts	55
IRQ1[GPIO41]	G04		
IRQ2[GPIO42]	F02		
IRQ3[GPIO43]	G02		
IRQ4[GPIO44][DMAAck1]	G25		
IRQ5[ModeCtrl][DMAReq1]	AC12		
IRQ6[GPIO45][EOT1/TC1]	H23		
IRQ7[GPIO46][DMAReq0]	B24		
IRQ8[GPIO47][DMAAck0]	D18		
IRQ9[GPIO48][EOT0/TC0]	A19		
[LeakTest]HoldPri	V24	System	56
MemAddr00	P01	DDR SDRAM	51
MemAddr01	P04		
MemAddr02	T02		
MemAddr03	T04		
MemAddr04	U01		
MemAddr05	V02		
MemAddr06	U04		
MemAddr07	W03		
MemAddr08	Y02		
MemAddr09	AB02		
MemAddr10	R03		
MemAddr11	AD01		
MemAddr12	AD02		
MemClkOut0	AF12	DDR SDRAM	51
$\overline{\text{MemClkOut0}}$	AE13		

Table 3. Signals Listed Alphabetically (Sheet 9 of 24)

Signal Name	Ball	Interface Group	Page
MemData00	AE12	DDR SDRAM	51
MemData01	AD13		
MemData02	AC13		
MemData03	AE11		
MemData04	AF10		
MemData05	AE10		
MemData06	AC11		
MemData07	AF09		
MemData08	AE09		
MemData09	AD10		
MemData10	AF08		
MemData11	AE08		
MemData12	AC10		
MemData13	AE07		
MemData14	AD08		
MemData15	AD05		
MemData16	AE03		
MemData17	AC05		
MemData18	AF02		
MemData19	AC03		
MemData20	AC02		
MemData21	AA03		
MemData22	Y04		
MemData23	AA02		
MemData24	V04		
MemData25	Y01		
MemData26	V03		
MemData27	W02		
MemData28	W01		
MemData29	U03		
MemData30	T03		
MemData31	U02		
MemSelfRef	AE04	DDR SDRAM	51
[ModeCtrl]IRQ5[DMAReq1]	AC12	System	56

Table 3. Signals Listed Alphabetically (Sheet 10 of 24)

Signal Name	Ball	Interface Group	Page
[NFALE]EMCTxD3, EMC1TxD1[GPIO19]	AC14	NAND Flash	55
[$\overline{\text{NFCE0}}$]$\overline{\text{PerCS0}}$	D06		
[$\overline{\text{NFCE1}}$]$\overline{\text{PerCS1}}$[GPIO06]	C06		
[$\overline{\text{NFCE2}}$]$\overline{\text{PerCS2}}$[GPIO07]	A04		
[$\overline{\text{NFCE3}}$]$\overline{\text{PerCS3}}$[GPIO08]	B07		
[NFCLE]EMCTxD2, EMC1TxD0[GPIO18]	AF14		
[$\overline{\text{NFRdyBusy}}$]EMCCD, EMC1RxErr[GPIO25]	AC16		
[$\overline{\text{NFREn}}$]EMCDV, EMC1CrsDV[GPIO21]	AF17		
[$\overline{\text{NFWEn}}$]EMCTxErr, EMC1TxEn[GPIO23]	AF18		
No ball	F06	A physical ball does not exist at these ball coordinates.	NA
No ball	F07		
No ball	F08		
No ball	F09		
No ball	F10		
No ball	F11		
No ball	F12		
No ball	F13		
No ball	F14		
No ball	F15		
No ball	F16		
No ball	F17		
No ball	F18		
No ball	F19		
No ball	F20		
No ball	F21		
No ball	G06		
No ball	G07		
No ball	G08		
No ball	G09		
No ball	G10		
No ball	G11		
No ball	G12		
No ball	G13		
No ball	G14		
No ball	G15		

Table 3. Signals Listed Alphabetically (Sheet 11 of 24)

Signal Name	Ball	Interface Group	Page
No ball	G16	A physical ball does not exist at these ball coordinates.	NA
No ball	G17		
No ball	G18		
No ball	G19		
No ball	G20		
No ball	G21		
No ball	H06		
No ball	H07		
No ball	H08		
No ball	H09		
No ball	H10		
No ball	H11		
No ball	H12		
No ball	H13		
No ball	H14		
No ball	H15		
No ball	H16		
No ball	H17		
No ball	H18		
No ball	H19		
No ball	H20		
No ball	H21		
No ball	J06		
No ball	J07		
No ball	J08		
No ball	J09		
No ball	J10		
No ball	J11		
No ball	J12		
No ball	J13		
No ball	J14		
No ball	J15		
No ball	J16		
No ball	J17		
No ball	J18		
No ball	J19		

Table 3. Signals Listed Alphabetically (Sheet 12 of 24)

Signal Name	Ball	Interface Group	Page
No ball	J20	A physical ball does not exist at these ball coordinates.	NA
No ball	J21		
No ball	K06		
No ball	K07		
No ball	K08		
No ball	K09		
No ball	K10		
No ball	K11		
No ball	K12		
No ball	K13		
No ball	K14		
No ball	K15		
No ball	K16		
No ball	K17		
No ball	K18		
No ball	K19		
No ball	K20		
No ball	K21		
No ball	L06		
No ball	L07		
No ball	L08		
No ball	L09		
No ball	L10		
No ball	L17		
No ball	L18		
No ball	L19		
No ball	L20		
No ball	L21		
No ball	M06		
No ball	M07		
No ball	M08		
No ball	M09		
No ball	M10		
No ball	M17		
No ball	M18		

Table 3. Signals Listed Alphabetically (Sheet 13 of 24)

Signal Name	Ball	Interface Group	Page
No ball	M19	A physical ball does not exist at these ball coordinates.	NA
No ball	M20		
No ball	M21		
No ball	N06		
No ball	N07		
No ball	N08		
No ball	N09		
No ball	N10		
No ball	N17		
No ball	N18		
No ball	N19		
No ball	N20		
No ball	N21		
No ball	P06		
No ball	P07		
No ball	P08		
No ball	P09		
No ball	P10		
No ball	P17		
No ball	P18		
No ball	P19		
No ball	P20		
No ball	P21		
No ball	R06		
No ball	R07		
No ball	R08		
No ball	R09		
No ball	R10		
No ball	R17		
No ball	R18		
No ball	R19		
No ball	R20		
No ball	R21		
No ball	T06		
No ball	T07		
No ball	T08		

Table 3. Signals Listed Alphabetically (Sheet 14 of 24)

Signal Name	Ball	Interface Group	Page
No ball	T09	A physical ball does not exist at these ball coordinates.	NA
No ball	T10		
No ball	T17		
No ball	T18		
No ball	T19		
No ball	T20		
No ball	T21		
No ball	U06		
No ball	U07		
No ball	U08		
No ball	U09		
No ball	U10		
No ball	U11		
No ball	U12		
No ball	U13		
No ball	U14		
No ball	U15		
No ball	U16		
No ball	U17		
No ball	U18		
No ball	U19		
No ball	U20		
No ball	U21		
No ball	V06		
No ball	V07		
No ball	V08		
No ball	V09		
No ball	V10		
No ball	V11		
No ball	V12		
No ball	V13		
No ball	V14		
No ball	V15		
No ball	V16		
No ball	V17		

Table 3. Signals Listed Alphabetically (Sheet 15 of 24)

Signal Name	Ball	Interface Group	Page
No ball	V18	A physical ball does not exist at these ball coordinates.	NA
No ball	V19		
No ball	V20		
No ball	V21		
No ball	W06		
No ball	W07		
No ball	W08		
No ball	W09		
No ball	W10		
No ball	W11		
No ball	W12		
No ball	W13		
No ball	W14		
No ball	W15		
No ball	W16		
No ball	W17		
No ball	W18		
No ball	W19		
No ball	W20		
No ball	W21		
No ball	Y06		
No ball	Y07		
No ball	Y08		
No ball	Y09		
No ball	Y10		
No ball	Y11		
No ball	Y12		
No ball	Y13		
No ball	Y14		
No ball	Y15		
No ball	Y16		
No ball	Y17		
No ball	Y18		
No ball	Y19		
No ball	Y20		
No ball	Y21		

Table 3. Signals Listed Alphabetically (Sheet 16 of 24)

Signal Name	Ball	Interface Group	Page
No ball	AA06	A physical ball does not exist at these ball coordinates.	NA
No ball	AA07		
No ball	AA08		
No ball	AA09		
No ball	AA10		
No ball	AA11		
No ball	AA12		
No ball	AA13		
No ball	AA14		
No ball	AA15		
No ball	AA16		
No ball	AA17		
No ball	AA18		
No ball	AA19		
No ball	AA20		
No ball	AA21		
OV_{DD}	E06	Power	57
OV_{DD}	E07		
OV_{DD}	E08		
OV_{DD}	E13		
OV_{DD}	E19		
OV_{DD}	E20		
OV_{DD}	E21		
OV_{DD}	F05		
OV_{DD}	F22		
OV_{DD}	G05		
OV_{DD}	G22		
OV_{DD}	H05		
OV_{DD}	H22		
OV_{DD}	L12		
OV_{DD}	L15		
OV_{DD}	M11		
OV_{DD}	M16		
OV_{DD}	N22		

Table 3. Signals Listed Alphabetically (Sheet 17 of 24)

Signal Name	Ball	Interface Group	Page
PCIAD00	B16	PCI	50
PCIAD01	C15		
PCIAD02	D15		
PCIAD03	A17		
PCIAD04	B17		
PCIAD05	A18		
PCIAD06	C16		
PCIAD07	D16		
PCIAD08	C18		
PCIAD09	A20		
PCIAD10	C20		
PCIAD11	B22		
PCIAD12	A23		
PCIAD13	A24		
PCIAD14	C22		
PCIAD15	D22		
PCIAD16	H24		
PCIAD17	F25		
PCIAD18	J24		
PCIAD19	K23		
PCIAD20	K24		
PCIAD21	J25		
PCIAD22	L23		
PCIAD23	K25		
PCIAD24	K26		
PCIAD25	M24		
PCIAD26	M23		
PCIAD27	L25		
PCIAD28	N23		
PCIAD29	N26		
PCIAD30	M26		
PCIAD31	P26		
PCIC0/$\overline{\text{BE0}}$	B18	PCI	50
PCIC1/$\overline{\text{BE1}}$	F23		
PCIC2/$\overline{\text{BE2}}$	F24		
PCIC3/$\overline{\text{BE3}}$	E26		
PCIClk	B21	PCI	50
$\overline{\text{PCIDevSel}}$	D26	PCI	50
$\overline{\text{PCIFrame}}$	G24	PCI	50

Table 3. Signals Listed Alphabetically (Sheet 18 of 24)

Signal Name	Ball	Interface Group	Page
PCIGnt0/Req	D17	PCI	50
PCIGnt1	L24		
PCIGnt2	A25		
PCIGnt3	D25		
PCIGnt4	H25		
PCIGnt5	E24		
PCIIDSel	G26	PCI	50
PCIINT	D20	PCI	50
PCIIRDY	E25	PCI	50
PCIPar	C23	PCI	50
PCIPErr	D24	PCI	50
PCIReq0/Gnt	N25	PCI	50
PCIReq1	B20		
PCIReq2	B19		
PCIReq3	C19		
PCIReq4	A22		
PCIReq5	H26		
PCIReset	D19	PCI	50
PCISErr	J23	PCI	50
PCIStop	E23	PCI	50
PCITRDY	G23	PCI	50

Table 3. Signals Listed Alphabetically (Sheet 19 of 24)

Signal Name	Ball	Interface Group	Page
PerAddr02[GPIO05][EOT3/TC3]	B04	External Slave Peripheral	53
PerAddr03[GPIO04][DMAAck3]	C07		
PerAddr04[GPIO03][DMAReq3]	D08		
PerAddr05[GPIO02][EOT2/TC2]	A05		
PerAddr06[GPIO01][DMAAck2]	B06		
PerAddr07[GPIO00][DMAReq2]	C08		
PerAddr08	D09		
PerAddr09	A07		
PerAddr10	C09		
PerAddr11	B08		
PerAddr12	D10		
PerAddr13	A08		
PerAddr14	B09		
PerAddr15	C10		
PerAddr16	C11		
PerAddr17	D12		
PerAddr18	C12		
PerAddr19	B11		
PerAddr20	B12		
PerAddr21	D13		
PerAddr22	A13		
PerAddr23	A12		
PerAddr24	A14		
PerAddr25	B13		
PerAddr26	C13		
PerAddr27	B14		
PerAddr28	A15		
PerAddr29	B15		
PerAddr30	C14		
PerAddr31	D14		
$\overline{\text{PerBLast}}$	D11	External Slave Peripheral	53
PerClk	C02	External Master Peripheral	54
$\overline{\text{PerCS0}}$[$\overline{\text{NFCE0}}$]	D06	External Slave Peripheral	53
$\overline{\text{PerCS1}}$[$\overline{\text{NFCE1}}$][GPIO06]	C06		
$\overline{\text{PerCS2}}$[$\overline{\text{NFCE2}}$][GPIO07]	A04		
$\overline{\text{PerCS3}}$[$\overline{\text{NFCE3}}$][GPIO08]	B07		
$\overline{\text{PerCS4}}$[GPIO09]	B10		
$\overline{\text{PerCS5}}$[GPIO10]	A10		

Table 3. Signals Listed Alphabetically (Sheet 20 of 24)

Signal Name	Ball	Interface Group	Page
PerData00	H01	External Slave Peripheral	53
PerData01	K04		
PerData02	G01		
PerData03	J03		
PerData04	J04		
PerData05	H03		
PerData06	E01		
PerData07	G03		
PerData08	H04		
PerData09	E02		
PerData10	D01		
PerData11	F03		
PerData12	C01		
PerData13	F04		
PerData14	E03		
PerData15	B01		
PerErr[GPIO11]	E04	External Master Peripheral	53
$\overline{\text{PerOE}}$	B03	External Slave Peripheral	53
PerReady	C05	External Slave Peripheral	53
PerR/$\overline{\text{W}}$	D05	External Slave Peripheral	53
$\overline{\text{PerWBE0}}$	H02	External Slave Peripheral	53
$\overline{\text{PerWBE1}}$	C04		
PSROOut	C26	System	56
$\overline{\text{RAS}}$	K02	DDR SDRAM	51
[RcvrInh]HoldReq	Y23	System	56
RefEn	W23	System	56
RejectPkt[DrvrInh1]	Y25	Ethernet	52

Table 3. Signals Listed Alphabetically (Sheet 21 of 24)

Signal Name	Ball	Interface Group	Page
Reserved	R23	Other	57
Reserved	R24		
Reserved	U23		
Reserved	V23		
Reserved	W25		
Reserved	W26		
Reserved	Y26		
Reserved	AB23		
Reserved	AB24		
Reserved	AC20		
Reserved	AC21		
Reserved	AC24		
Reserved	AD20		
Reserved	AD21		
Reserved	AD22		
Reserved	AD23		
Reserved	AE22		
Reserved	AE23		
Reserved	AE26		
Reserved	AF23		
Reserved	AF24		
SAGND	AF15	Power	57
SAV_{DD}	AE14		
SCPClkOut[IIC1SClk]	U24	Serial Peripheral (SPI)	55
SCPDI[IIC1SData]	V25		
SCPDO	T23		

Table 3. Signals Listed Alphabetically (Sheet 22 of 24)

Signal Name	Ball	Interface Group	Page
SV_{DD}	P05	Power	57
SV_{DD}	R11		
SV_{DD}	R16		
SV_{DD}	T12		
SV_{DD}	T15		
SV_{DD}	W05		
SV_{DD}	W22		
SV_{DD}	Y05		
SV_{DD}	Y22		
SV_{DD}	AA05		
SV_{DD}	AA22		
SV_{DD}	AB06		
SV_{DD}	AB07		
SV_{DD}	AB08		
SV_{DD}	AB14		
SV_{DD}	AB19		
SV_{DD}	AB20		
SV_{DD}	AB21		
SV_{REF1}	W04	DDR SDRAM	51
SV_{REF2A}	P03		
SV_{REF2B}	AE06		
SysClk	AE19	System	56
SysErr	AB01	System	56
$\overline{\text{SysReset}}$	AE18	System	56
TCK	B05	JTAG	55
TDI	C17	JTAG	55
TDO	C21	JTAG	55
TestEn	A03	System	56
TmrClk1	AD11	System	56
TmrClk2	AD25	System	56
TMS	D02	JTAG	55
TrcBS0[GPIO49]	AE21	Trace	57
TrcBS1[GPIO50]	AC25		
TrcBS2[GPIO51]	AA24		
TrcClk	AC19	Trace	57

Table 3. Signals Listed Alphabetically (Sheet 23 of 24)

Signal Name	Ball	Interface Group	Page
TrcES0[GPIO52]	Y03	Trace	57
TrcES1[GPIO53]	AA04		
TrcES2[GPIO54]	AB03		
TrcES3[GPIO55]	AB04		
TrcES4[GPIO56]	AF22		
TrcTS0[GPIO57]	AC22	Trace	57
TrcTS1[GPIO58]	AE24		
TrcTS2[GPIO59]	AD04		
TrcTS3[GPIO60]	AD06		
TrcTS4[GPIO61]	AC09		
TrcTS5[GPIO62]	AD12		
TrcTS6[GPIO63]	AE15		
$\overline{\text{TRST}}$	D07	JTAG	55
$\overline{\text{UART0\_CTS}}$/UART3_Rx[GPIO36]	V26	UART Peripheral	54
$\overline{\text{UART0\_RTS}}$/UART3_Tx[GPIO37]	R26		
UART0_Rx	T25		
UART0_Tx	P25		
$\overline{\text{UART0\_DCD}}$/$\overline{\text{UART1\_CTS}}$/UART2_Tx[GPIO34]	R25		
$\overline{\text{UART0\_DSR}}$/$\overline{\text{UART1\_RTS}}$/UART2_Rx[GPIO35]	U26		
$\overline{\text{UART0\_DTR}}$/UART1_Tx[GPIO38]	N24		
$\overline{\text{UART0\_RI}}$/UART1_Rx[GPIO39]	P24		
UARTSerClk	P23		

Table 3. Signals Listed Alphabetically (Sheet 24 of 24)

Signal Name	Ball	Interface Group	Page
V_{DD}	E05	Power	57
V_{DD}	E10		
V_{DD}	E11		
V_{DD}	E12		
V_{DD}	E15		
V_{DD}	E16		
V_{DD}	E17		
V_{DD}	E22		
V_{DD}	K05		
V_{DD}	K22		
V_{DD}	L05		
V_{DD}	L22		
V_{DD}	M05		
V_{DD}	M22		
V_{DD}	M14		
V_{DD}	N12		
V_{DD}	P15		
V_{DD}	R05		
V_{DD}	R13		
V_{DD}	R22		
V_{DD}	T05		
V_{DD}	T22		
V_{DD}	U05		
V_{DD}	U22		
V_{DD}	AB05		
V_{DD}	AB10		
V_{DD}	AB11		
V_{DD}	AB12		
V_{DD}	AB15		
V_{DD}	AB16		
V_{DD}	AB17		
V_{DD}	AB22		
$\overline{WE}$	K01	DDR SDRAM	51

In the following table, only the primary (default) signal name is shown for each pin. Multiplexed or multifunction signals are marked with an asterisk (*). To determine what signals or functions are multiplexed on those pins, look up the primary signal name in Table 3, *Signals Listed Alphabetically*.

Table 4. Signals Listed by Ball Assignment (Sheet 1 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	GND	B01	PerData15	C01	PerData12	D01	PerData10
A02	GND	B02	GND	C02	PerClk	D02	TMS
A03	TestEn	B03	$\overline{\text{PerOE}}$	C03	GND	D03	IRQ0*
A04	$\overline{\text{PerCS2}}$*	B04	PerAddr02*	C04	$\overline{\text{PerWBE1}}$	D04	GND
A05	PerAddr05*	B05	TCK	C05	PerReady	D05	PerR/$\overline{\text{W}}$
A06	GND	B06	PerAddr06*	C06	$\overline{\text{PerCS1}}$*	D06	$\overline{\text{PerCS0}}$*
A07	PerAddr09	B07	$\overline{\text{PerCS3}}$*	C07	PerAddr03*	D07	$\overline{\text{TRST}}$
A08	PerAddr13	B08	PerAddr11	C08	PerAddr07*	D08	PerAddr04*
A09	GND	B09	PerAddr14	C09	PerAddr10	D09	PerAddr08
A10	$\overline{\text{PerCS5}}$*	B10	$\overline{\text{PerCS4}}$*	C10	PerAddr15	D10	PerAddr12
A11	GND	B11	PerAddr19	C11	PerAddr16	D11	$\overline{\text{PerBLast}}$
A12	PerAddr23	B12	PerAddr20	C12	PerAddr18	D12	PerAddr17
A13	PerAddr22	B13	PerAddr25	C13	PerAddr26	D13	PerAddr21
A14	PerAddr24	B14	PerAddr27	C14	PerAddr30	D14	PerAddr31
A15	PerAddr28	B15	PerAddr29	C15	PCIAD01	D15	PCIAD02
A16	GND	B16	PCIAD00	C16	PCIAD06	D16	PCIAD07
A17	PCIAD03	B17	PCIAD04	C17	TDI	D17	$\overline{\text{PCIGnt0}}$/$\overline{\text{Req}}$
A18	PCIAD05	B18	PCIC0/$\overline{\text{BE0}}$	C18	PCIAD08	D18	IRQ8*
A19	IRQ9*	B19	$\overline{\text{PCIReq2}}$	C19	$\overline{\text{PCIReq3}}$	D19	$\overline{\text{PCIReset}}$
A20	PCIAD09	B20	$\overline{\text{PCIReq1}}$	C20	PCIAD10	D20	$\overline{\text{PCIINT}}$
A21	GND	B21	PCIClk	C21	TDO	D21	GND
A22	$\overline{\text{PCIReq4}}$	B22	PCIAD11	C22	PCIAD14	D22	PCIAD15
A23	PCIAD12	B23	$\overline{\text{ExtReset}}$	C23	PCIPar	D23	GND
A24	PCIAD13	B24	IRQ7*	C24	GND	D24	$\overline{\text{PCIPErr}}$
A25	$\overline{\text{PCIGnt2}}$	B25	GND	C25	$\overline{\text{Halt}}$*	D25	$\overline{\text{PCIGnt3}}$
A26	GND	B26	GND	C26	PSROOut	D26	$\overline{\text{PCIDevSel}}$

Table 4. Signals Listed by Ball Assignment (Sheet 2 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	PerData06	F01	GND	G01	PerData02	H01	PerData00
E02	PerData09	F02	IRQ2*	G02	IRQ3*	H02	$\overline{\text{PerWBE0}}$
E03	PerData14	F03	PerData11	G03	PerData07	H03	PerData05
E04	PerErr*	F04	PerData13	G04	IRQ1*	H04	PerData08
E05	V_{DD}	F05	OV_{DD}	G05	OV_{DD}	H05	OV_{DD}
E06	OV_{DD}	F06	No ball	G06	No ball	H06	No ball
E07	OV_{DD}	F07	No ball	G07	No ball	H07	No ball
E08	OV_{DD}	F08	No ball	G08	No ball	H08	No ball
E09	GND	F09	No ball	G09	No ball	H09	No ball
E10	V_{DD}	F10	No ball	G10	No ball	H10	No ball
E11	V_{DD}	F11	No ball	G11	No ball	H11	No ball
E12	V_{DD}	F12	No ball	G12	No ball	H12	No ball
E13	OV_{DD}	F13	No ball	G13	No ball	H13	No ball
E14	GND	F14	No ball	G14	No ball	H14	No ball
E15	V_{DD}	F15	No ball	G15	No ball	H15	No ball
E16	V_{DD}	F16	No ball	G16	No ball	H16	No ball
E17	V_{DD}	F17	No ball	G17	No ball	H17	No ball
E18	GND	F18	No ball	G18	No ball	H18	No ball
E19	OV_{DD}	F19	No ball	G19	No ball	H19	No ball
E20	OV_{DD}	F20	No ball	G20	No ball	H20	No ball
E21	OV_{DD}	F21	No ball	G21	No ball	H21	No ball
E22	V_{DD}	F22	OV_{DD}	G22	OV_{DD}	H22	OV_{DD}
E23	$\overline{\text{PCIStop}}$	F23	PCIC1/$\overline{\text{BE1}}$	G23	$\overline{\text{PCITRDY}}$	H23	IRQ6*
E24	$\overline{\text{PCIGnt5}}$	F24	PCIC2/$\overline{\text{BE2}}$	G24	$\overline{\text{PCIFrame}}$	H24	PCIAD16
E25	$\overline{\text{PCIIRDY}}$	F25	PCIAD17	G25	IRQ4*	H25	$\overline{\text{PCIGnt4}}$
E26	PCIC3/$\overline{\text{BE3}}$	F26	GND	G26	PCIIDSel	H26	$\overline{\text{PCIReq5}}$

Table 4. Signals Listed by Ball Assignment (Sheet 3 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	DM2	K01	$\overline{WE}$	L01	GND	M01	ECC2
J02	$\overline{CAS}$	K02	$\overline{RAS}$	L02	ECC6	M02	ECC3
J03	PerData03	K03	DQS2	L03	DM3	M03	ECC7
J04	PerData04	K04	PerData01	L04	GND	M04	DQS3
J05	GND	K05	V_{DD}	L05	V_{DD}	M05	V_{DD}
J06	No ball	K06	No ball	L06	No ball	M06	No ball
J07	No ball	K07	No ball	L07	No ball	M07	No ball
J08	No ball	K08	No ball	L08	No ball	M08	No ball
J09	No ball	K09	No ball	L09	No ball	M09	No ball
J10	No ball	K10	No ball	L10	No ball	M10	No ball
J11	No ball	K11	No ball	L11	GND	M11	OV_{DD}
J12	No ball	K12	No ball	L12	OV_{DD}	M12	GND
J13	No ball	K13	No ball	L13	GND	M13	GND
J14	No ball	K14	No ball	L14	GND	M14	V_{DD}
J15	No ball	K15	No ball	L15	OV_{DD}	M15	GND
J16	No ball	K16	No ball	L16	GND	M16	OV_{DD}
J17	No ball	K17	No ball	L17	No ball	M17	No ball
J18	No ball	K18	No ball	L18	No ball	M18	No ball
J19	No ball	K19	No ball	L19	No ball	M19	No ball
J20	No ball	K20	No ball	L20	No ball	M20	No ball
J21	No ball	K21	No ball	L21	No ball	M21	No ball
J22	GND	K22	V_{DD}	L22	V_{DD}	M22	V_{DD}
J23	$\overline{PCISErr}$	K23	PCIAD19	L23	PCIAD22	M23	PCIAD26
J24	PCIAD18	K24	PCIAD20	L24	$\overline{PCIGnt1}$	M24	PCIAD25
J25	PCIAD21	K25	PCIAD23	L25	PCIAD27	M25	GND
J26	GND	K26	PCIAD24	L26	GND	M26	PCIAD30

Table 4. Signals Listed by Ball Assignment (Sheet 4 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	$\overline{\text{BankSel3}}$	P01	MemAddr00	R01	$\overline{\text{BankSel2}}$	T01	GND
N02	ECC1	P02	ECC0	R02	$\overline{\text{BankSel1}}$	T02	MemAddr02
N03	ECC4	P03	SV_{REF2A}	R03	MemAddr10	T03	MemData30
N04	ECC5	P04	MemAddr01	R04	$\overline{\text{BankSel0}}$	T04	MemAddr03
N05	GND	P05	SV_{DD}	R05	V_{DD}	T05	V_{DD}
N06	No ball	P06	No ball	R06	No ball	T06	No ball
N07	No ball	P07	No ball	R07	No ball	T07	No ball
N08	No ball	P08	No ball	R08	No ball	T08	No ball
N09	No ball	P09	No ball	R09	No ball	T09	No ball
N10	No ball	P10	No ball	R10	No ball	T10	No ball
N11	GND	P11	GND	R11	SV_{DD}	T11	GND
N12	V_{DD}	P12	GND	R12	GND	T12	SV_{DD}
N13	GND	P13	GND	R13	V_{DD}	T13	GND
N14	GND	P14	GND	R14	GND	T14	GND
N15	GND	P15	V_{DD}	R15	GND	T15	SV_{DD}
N16	GND	P16	GND	R16	SV_{DD}	T16	GND
N17	No ball	P17	No ball	R17	No ball	T17	No ball
N18	No ball	P18	No ball	R18	No ball	T18	No ball
N19	No ball	P19	No ball	R19	No ball	T19	No ball
N20	No ball	P20	No ball	R20	No ball	T20	No ball
N21	No ball	P21	No ball	R21	No ball	T21	No ball
N22	OV_{DD}	P22	GND	R22	V_{DD}	T22	V_{DD}
N23	PCIAD28	P23	UARTSerClk	R23	Reserved	T23	SCPDO
N24	$\overline{\text{UART0\_DTR}}$*	P24	$\overline{\text{UART0\_RI}}$*	R24	Reserved	T24	IIC0SData
N25	$\overline{\text{PCIReq0}}/\overline{\text{Gnt}}$	P25	UART0_Tx*	R25	$\overline{\text{UART0\_DCD}}$*	T25	UART0_Rx
N26	PCIAD29	P26	PCIAD31	R26	$\overline{\text{UART0\_RTS}}$*	T26	GND

Table 4. Signals Listed by Ball Assignment (Sheet 5 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	MemAddr04	V01	GND	W01	MemData28	Y01	MemData25
U02	MemData31	V02	MemAddr05	W02	MemData27	Y02	MemAddr08
U03	MemData29	V03	MemData26	W03	MemAddr07	Y03	TrcES0*
U04	MemAddr06	V04	MemData24	W04	SV_{REF1}	Y04	MemData22
U05	V_{DD}	V05	GND	W05	SV_{DD}	Y05	SV_{DD}
U06	No ball	V06	No ball	W06	No ball	Y06	No ball
U07	No ball	V07	No ball	W07	No ball	Y07	No ball
U08	No ball	V08	No ball	W08	No ball	Y08	No ball
U09	No ball	V09	No ball	W09	No ball	Y09	No ball
U10	No ball	V10	No ball	W10	No ball	Y10	No ball
U11	No ball	V11	No ball	W11	No ball	Y11	No ball
U12	No ball	V12	No ball	W12	No ball	Y12	No ball
U13	No ball	V13	No ball	W13	No ball	Y13	No ball
U14	No ball	V14	No ball	W14	No ball	Y14	No ball
U15	No ball	V15	No ball	W15	No ball	Y15	No ball
U16	No ball	V16	No ball	W16	No ball	Y16	No ball
U17	No ball	V17	No ball	W17	No ball	Y17	No ball
U18	No ball	V18	No ball	W18	No ball	Y18	No ball
U19	No ball	V19	No ball	W19	No ball	Y19	No ball
U20	No ball	V20	No ball	W20	No ball	Y20	No ball
U21	No ball	V21	No ball	W21	No ball	Y21	No ball
U22	V_{DD}	V22	GND	W22	SV_{DD}	Y22	SV_{DD}
U23	Reserved	V23	Reserved	W23	RefEn	Y23	HoldReq*
U24	SCPClkOut*	V24	HoldPri*	W24	GPIO32	Y24	GPIO28
U25	IIC0SClk	V25	SCPDI*	W25	Reserved	Y25	RejectPkt*
U26	$\overline{\text{UART0\_DSR}}$*	V26	$\overline{\text{UART0\_CTS}}$*	W26	Reserved	Y26	Reserved

Table 4. Signals Listed by Ball Assignment (Sheet 6 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	GND	AB01	SysErr	AC01	GND	AD01	MemAddr11
AA02	MemData23	AB02	MemAddr09	AC02	MemData20	AD02	MemAddr12
AA03	MemData21	AB03	TrcES2*	AC03	MemData19	AD03	GND
AA04	TrcES1*	AB04	TrcES3*	AC04	GND	AD04	TrcTS2*
AA05	SV_{DD}	AB05	V_{DD}	AC05	MemData17	AD05	MemData15
AA06	No ball	AB06	SV_{DD}	AC06	DQS8	AD06	TrcTS3*
AA07	No ball	AB07	SV_{DD}	AC07	GND	AD07	DM1
AA08	No ball	AB08	SV_{DD}	AC08	DQS1	AD08	MemData14
AA09	No ball	AB09	GND	AC09	TrcTS4*	AD09	DQS0
AA10	No ball	AB10	V_{DD}	AC10	MemData12	AD10	MemData09
AA11	No ball	AB11	V_{DD}	AC11	MemData06	AD11	TmrClk1
AA12	No ball	AB12	V_{DD}	AC12	IRQ5*	AD12	TrcTS5*
AA13	No ball	AB13	GND	AC13	MemData02	AD13	MemData01
AA14	No ball	AB14	SV_{DD}	AC14	EMCTxD3*	AD14	EMCTxD0*
AA15	No ball	AB15	V_{DD}	AC15	EMCTxClk*	AD15	EMCCrS*
AA16	No ball	AB16	V_{DD}	AC16	EMCCD*	AD16	EMCRxErr*
AA17	No ball	AB17	V_{DD}	AC17	EMCRxD3*	AD17	AV_{DD}
AA18	No ball	AB18	GND	AC18	EMCMDIO	AD18	EMCRxD2*
AA19	No ball	AB19	SV_{DD}	AC19	TrcClk	AD19	EMCRxD0*
AA20	No ball	AB20	SV_{DD}	AC20	Reserved	AD20	Reserved
AA21	No ball	AB21	SV_{DD}	AC21	Reserved	AD21	Reserved
AA22	SV_{DD}	AB22	V_{DD}	AC22	TrcTS0*	AD22	Reserved
AA23	BusReq*	AB23	Reserved	AC23	GND	AD23	Reserved
AA24	TrcBS2*	AB24	Reserved	AC24	Reserved	AD24	GND
AA25	$\overline{\text{ExtAck}}$*	AB25	HoldAck*	AC25	TrcBS1*	AD25	TmrClk2
AA26	GND	AB26	GPIO33	AC26	GPIO26	AD26	$\overline{\text{ExtReq}}$*

Table 4. Signals Listed by Ball Assignment (Sheet 7 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AE01	GND	AF01	GND				
AE02	GND	AF02	MemData18				
AE03	MemData16	AF03	BA0				
AE04	MemSelfRef	AF04	BA1				
AE05	DM0	AF05	ClkEn				
AE06	SV_{REF2B}	AF06	GND				
AE07	MemData13	AF07	DM8				
AE08	MemData11	AF08	MemData10				
AE09	MemData08	AF09	MemData07				
AE10	MemData05	AF10	MemData04				
AE11	MemData03	AF11	GND				
AE12	MemData00	AF12	MemClkOut0				
AE13	$\overline{\text{MemClkOut0}}$	AF13	EMCTxD1*				
AE14	SAV_{DD}	AF14	EMCTxD2*				
AE15	TrcTS6*	AF15	SAGND				
AE16	EMCMDClk	AF16	GND				
AE17	AGND	AF17	EMCDV*				
AE18	$\overline{\text{SysReset}}$	AF18	EMCTxErr*				
AE19	SysClk	AF19	EMCRxClk				
AE20	EMCRxD1*	AF20	EMCTxEn*				
AE21	TrcBS0*	AF21	GND				
AE22	Reserved	AF22	TrcES4*				
AE23	Reserved	AF23	Reserved				
AE24	TrcTS1*	AF24	Reserved				
AE25	GND	AF25	GND				
AE26	Reserved	AF26	GND				

Signal Descriptions

The PPC440GR embedded controller is packaged in a 456-ball enhanced plastic ball grid array (E-PBGA). The following tables describe the package level pinout.

Table 5. Pin Summary

Group	No. of Pins
Signal pins, non-multiplexed	221
Signal pins, multiplexed	62
Total Signal Pins	**283**
AV_{DD}	1
SAV_{DD}	1
SAGnd	1
AGnd	1
OV_{DD}	18
SV_{DD}	18
V_{DD}	32
Gnd	80
Total Power Pins	**152**
Reserved	21
Total Pins	**456**

In the table “Signal Functional Description” on page 50, each I/O signal is listed along with a short description of its function. Active-low signals (for example, $\overline{RAS}$) are marked with an overline. Please see “Signals Listed Alphabetically” on page 17 for the pin (ball) number to which each signal is assigned.

Multiplexed Signals

Some signals are multiplexed on the same pin so that the pin can be used for different functions. In most cases, the signal names shown in this table are not accompanied by signal names that may be multiplexed on the same pin. If you need to know what, if any, signals are multiplexed with a particular signal, look up the name in “Signals Listed Alphabetically” on page 17. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible. The circuit type for multiplexed signals is shown as “Multiplex.” The actual circuit type is the same as the primary signal.

Multipurpose Signals

In addition to multiplexing, some pins are also multi-purpose. For example, the EBC peripheral controller address pins (PerAddr) are used as outputs by the PPC440GR to broadcast an address to external slave devices when the PPC440GR has control of the external bus. When during the course of normal chip operation an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the PPC440GR. In this example, the pins are also bidirectional, serving both as inputs and outputs.

Multimode Signals

In some cases (for example, Ethernet) the function of a pin may vary with different modes of operation. When a pin has multiple signal names assigned to distinguish different modes of operation, all of the names are shown.

Strapping Pins

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 79). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

Reserved Pins

The balls marked *Reserved* on this chip are not functional. However, most of the reserved balls cannot be left unconnected. Connect the balls shown in Table 6 as indicated:

Table 6. Non-Functional Ball Connections

Ball	Connection
R23	GND
R24	GND
U23	GND
V23	GND
W25	GND
W26	GND
Y26	GND
AB23	GND
AB24	GND
AC20	GND
AC21	GND
AC24	GND
AD20	GND
AD21	GND
AD22	GND
AD23	GND
AE22	do not connect
AE23	GND
AE26	GND
AF23	do not connect
AF24	GND

Table 7. Signal Functional Description (Sheet 1 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI Interface				
PCIAD00:31	Address/Data bus (bidirectional).	I/O	3.3V PCI	
PCIC0:3/$\overline{\text{BE0:3}}$	PCI Command/Byte Enables.	I/O	3.3V PCI	
PCIClk	Provides timing to the PCI interface for PCI transactions.	I	3.3V PCI	
$\overline{\text{PCIDevSel}}$	Indicates the driving device has decoded its address as the target of the current access.	I/O	3.3V PCI	
$\overline{\text{PCIFrame}}$	Driven by the current master to indicate beginning and duration of an access.	I/O	3.3V PCI	
$\overline{\text{PCIGnt1}}$/$\overline{\text{Req}}$	Indicates that the specified agent is granted access to the bus. When the internal arbiter is enabled, output is PCIGnt0. When the internal arbiter is disabled, output is Req.	O	3.3V PCI	
$\overline{\text{PCIGnt2:6}}$	Indicates that the specified agent is granted access to the bus.	O	3.3V PCI	
PCIIDSel	Used as a chip select during configuration read and write transactions.	I	3.3V PCI	
$\overline{\text{PCIINT}}$	Level sensitive PCI interrupt.	O	3.3V PCI	
$\overline{\text{PCIIRDY}}$	Indicates initiating agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	
PCIPar	Even parity.	I/O	3.3V PCI	
$\overline{\text{PCIPErr}}$	Reports data parity errors during all PCI transactions except a Special Cycle.	I/O	3.3V PCI	
$\overline{\text{PCIReq0}}$/$\overline{\text{Gnt}}$	Indicates to the PCI arbiter that the specified agent wishes to use the bus. When the internal arbiter is enabled, input is PCIReq0. When internal arbiter is disabled, input is Gnt.	I	3.3V PCI	
$\overline{\text{PCIReq1:5}}$	An indication to the PCI arbiter that the specified agent wishes to use the bus.	I	3.3V PCI	
$\overline{\text{PCIReset}}$	Brings PCI device registers and logic to a consistent state.	O	3.3V PCI	
$\overline{\text{PCISErr}}$	Reports address parity errors, data parity errors on the Special Cycle command, or other catastrophic system errors.	I/O	3.3V PCI	
$\overline{\text{PCIStop}}$	Indicates the current target is requesting the master to stop the current transaction.	I/O	3.3V PCI	
$\overline{\text{PCITRDY}}$	Indicates the target agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	

Table 7. Signal Functional Description (Sheet 2 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
DDR SDRAM Interface				
BA0:1	Bank Address supporting up to four internal banks.	O	2.5V SSTL_2	
$\overline{\text{BankSel0:3}}$	Selects up to four external DDR SDRAM banks.	O	2.5V SSTL_2	
$\overline{\text{CAS}}$	Column Address Strobe.	O	2.5V SSTL_2	
ClkEn	Clock Enable.	O	2.5V SSTL_2	
DM0:3 DM8	Memory write data byte lane masks. DM8 is the byte lane mask for the ECC byte lane.	O	2.5V SSTL_2	
DQS0:3 DQS8	Byte lane data strobe. DQS8 is the data strobe for the ECC byte lane.	I/O	2.5V SSTL_2	
ECC0:7	ECC check bits 0:7.	I/O	2.5V SSTL_2	
MemAddr00:12	Memory address bus.	O	2.5V SSTL_2	
MemClkOut0 $\overline{\text{MemClkOut0}}$	Subsystem clock.	O	2.5V SSTL_2 Diff driver	
MemData00:31	Memory data bus.	I/O	2.5V SSTL_2	
MemSelfRef	Self refresh.	I	3.3V tolerant 2.5V CMOS	5
$\overline{\text{RAS}}$	Row Address Strobe.	O	2.5V SSTL_2	
$\overline{\text{WE}}$	Write Enable.	O	2.5V SSTL_2	
S_{VREF1}	SSTL reference voltage.	I	Volt ref receiver	
$S_{VREF2A:B}$	Supplemental SSTL reference voltage.	I	Volt ref pin (supplemental)	

Table 7. Signal Functional Description (Sheet 3 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Ethernet Interface				
EMCCD, EMC1RxErr	MII: Collision detection. RMII B: Receive error.	I/O	3.3V tolerant 2.5V CMOS	
EMCCrS, EMC0CrsDV	MII: Carrier sense. RMII A: Carrier sense data valid.	I/O	3.3V tolerant 2.5V CMOS	
EMCDV, EMC1CrsDV	MII: Data valid. RMII B: Carrier sense data valid.	I/O	3.3V tolerant 2.5V CMOS	
EMCMDClk	MII: Management data clock.	O	3.3V tolerant 2.5V CMOS	
EMCMDIO	MII: Transfer command and status information between MII and PHY.	I/O	3.3V tolerant 2.5V CMOS	
EMCRxClk	MII: Receive clock.	I/O	3.3V tolerant 2.5V CMOS	
EMCRxD0:1, EMC0RxD0:1 EMC0:BRxD	MII: Receive data. RMII A: Receive data. SMII A and B: Receive data.	I/O	3.3V tolerant 2.5V CMOS	
EMCRxD2:3, EMC1RxD0:1	MII: Receive data. RMII B: Receive data.	I/O	3.3V tolerant 2.5V CMOS	
EMCRxErr, EMC0RxErr	MII: Receive error. RMII A: Receive error.	I/O	3.3V tolerant 2.5V CMOS	
EMCTxClk, EMCRefClk	MII: Transmit clock. RMII and SMII: Transmit clock (max 125MHz in SMII).	I	3.3V tolerant 2.5V CMOS	
EMCTxD0:1, EMC0TxD0:1 EMC0:BTxD	MII: Transmit data. RMII A: Transmit data. SMII A and B: Transmit data.	I/O	3.3V tolerant 2.5V CMOS	
EMCTxD2:3, EMC1TxD0:1	MII: Transmit data. RMII B: Transmit data.	I/O	3.3V tolerant 2.5V CMOS	
EMCTxEn, EMC0TxEn, EMCSync	MII: Transmit data enabled. RMII A: Transmit data enabled. SMII: Sync signal.	O	3.3V tolerant 2.5V CMOS	
EMCTxErr, EMC1TxEn	MII: Transmit error. RMII B: Transmit data enabled.	I/O	3.3V tolerant 2.5V CMOS	
RejectPkt	External request to reject a packet.	I	3.3V tolerant 2.5V CMOS	5

Table 7. Signal Functional Description (Sheet 4 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
External Slave Peripheral Interface				
DMAAck0:3	Used by the PPC440GR to indicate that data transfers have occurred.	O	Multiplex	
DMAReq0:3	Used by slave peripherals to indicate they are prepared to transfer data.	I	Multiplex	1, 5
EOT0:3/TC0:3	End Of Transfer/Terminal Count.	I/O	Multiplex	1, 5
PerAddr02:07	Peripheral address bus used by PPC440GR when not in external master mode, otherwise used by external master.	I/O	3.3V LVTTL	1, 2
PerAddr08:31	Peripheral address bus used by PPC440GR when not in external master mode, otherwise used by external master.	I/O	3.3V LVTTL	
$\overline{\text{PerBLast}}$	Used by either the peripheral controller, DMA controller, or external master to indicates the last transfer of a memory access.	I/O	3.3V LVTTL	1, 4
$\overline{\text{PerCS0:5}}$	External peripheral device select.	O	3.3V LVTTL	2
PerData00:15	Peripheral data bus used by PPC440GR when not in external master mode, otherwise used by external master. **Note:** PerData00 is the most significant bit (msb) on this bus.	I/O	3.3V LVTTL	1
$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC440GR is the bus master, it enables the selected device to drive the bus.	O	3.3V LVTTL	2
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	3.3V LVTTL	
PerR/$\overline{\text{W}}$	Used by the PPC440GR when not in external master mode, as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise, it used by the external master as an input to indicate the direction of transfer.	I/O	3.3V LVTTL	1, 2
$\overline{\text{PerWBE0:1}}$	External peripheral data bus byte enables.	I/O	3.3V LVTTL	1, 2
PerErr	External Error. Used as an input to record external slave peripheral errors.	I/O	3.3V LVTTL	1, 5

Table 7. Signal Functional Description (Sheet 5 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
External Master Peripheral Interface				
BusReq	Bus Request. Used when the PPC440GR needs to regain control of peripheral interface from an external master.	O	Multiplex	
$\overline{\text{ExtAck}}$	External Acknowledgement. Used by the PPC440GR to indicate that a data transfer occurred.	O	Multiplex	
$\overline{\text{ExtReq}}$	External Request. Used by an external master to indicate it is prepared to transfer data.	I	Multiplex	1, 4
$\overline{\text{ExtReset}}$	Peripheral Reset. Used by an external master and by synchronous peripheral slaves.	O	3.3V LVTTL	
HoldAck	Hold Acknowledge. Used by the PPC440GR to transfer ownership of peripheral bus to an external master.	O	Multiplex	
HoldReq	Hold Request. Used by an external master to request ownership of the peripheral bus.	I	Multiplex	1, 5
HoldPri	Hold Primary. Used by an external master to indicate the priority of a given external master tenure.	I	Multiplex	
PerClk	Peripheral Clock. Used by an external master and by synchronous peripheral slaves.	O	3.3V LVTTL	
UART Peripheral Interface				
UARTSerClk	Serial clock input that provides an alternative to the internally generated serial clock. Used in cases where the allowable internally generated clock rates are not satisfactory.	I	3.3V LVTTL	1, 4
UARTn_Rx	UART Receive data.	I	3.3V LVTTL	1, 4
UARTn_Tx	UART Transmit data.	O	3.3V LVTTL	4
$\overline{\text{UARTn\_DCD}}$	UART Data Carrier Detect.	I	3.3V LVTTL	6
$\overline{\text{UARTn\_DSR}}$	UART Data Set Ready.	I	3.3V LVTTL	6
$\overline{\text{UARTn\_CTS}}$	UART Clear To Send.	I	3.3V LVTTL	1, 4, 6
$\overline{\text{UARTn\_DTR}}$	UART Data Terminal Ready.	O	3.3V LVTTL	4
$\overline{\text{UARTn\_RTS}}$	UART Request To Send.	O	3.3V LVTTL	4
$\overline{\text{UARTn\_RI}}$	UART Ring Indicator.	I	3.3V LVTTL	1, 4
IIC Peripheral Interface				
IIC0SClk	IIC0 Serial Clock.	I/O	3.3V LVTTL	1, 2
IIC0SData	IIC0 Serial Data.	I/O	3.3V LVTTL	1, 2
IIC10SClk	IIC1 Serial Clock.	I/O	Multiplex	
IIC1SData	IIC1 Serial Data.	I/O	Multiplex	

Table 7. Signal Functional Description (Sheet 6 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
NAND Flash Interface				
NFALE	Address Latch Enable.	O	Multiplex	
$\overline{\text{NFCE0:3}}$	Chip Enable (multiplexed with the $\overline{\text{PerCS0:3}}$ signals).	O	Multiplex	
NFCLE	Command Latch Enable.	O	Multiplex	
$\overline{\text{NFRdyBusy}}$	Ready/Busy. Indicates status of device during program erase or page read. This signal is wire-or connected from all NAND Flash devices.	I	Multiplex	
$\overline{\text{NFREn}}$	Read Enable strobe.	O	Multiplex	
$\overline{\text{NFWEn}}$	Write Enable strobe.	O	Multiplex	
Serial Peripheral Interface				
SCPClkOut	Clock output. SCPClkOut, the serial port master clock out, is used to synchronize all data movement both into and out of the device through the serial data ports. Normally, data is shifted out on the rising edge of the clock and shifted in on the negative edge. SCPClkOut is also used to shift data into and out of the slave device. When the SPMODE register is reset, SCPClkOut is forced to 0.	O	3.3V LVTTL	
SCPDI	Data In. Data is received from the connected slave device and is captured synchronously with SysClk.	I	3.3V LVTTL	
SCPDO	Data output. Data is sent to the connected slave device synchronously with SysClk.	O	3.3V LVTTL	
Interrupts Interface				
IRQ0:4	External interrupt requests 0 through 4.	I/O	3.3V LVTTL	1, 5
IRQ5	External interrupt request 5.	I	3.3V tolerant 2.5V CMOS	1, 5
IRQ6:9	External interrupt requests 6 through 9.	I/O	3.3V LVTTL	1, 5
JTAG Interface				
TCK	Test Clock.	I	3.3V LVTTL w/pull-up	1
TDI	Test Data In.	I	3.3V LVTTL w/pull-up	4
TDO	Test Data Out.	O	3.3V LVTTL	
TMS	Test Mode Select.	I	3.3V LVTTL w/pull-up	1
$\overline{\text{TRST}}$	Test Reset.	I	3.3V LVTTL w/pull-up	5

Table 7. Signal Functional Description (Sheet 7 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	Main system clock input.	Clock	3.3V LVTTL	
SysErr	Set to 1 when a machine check is generated.	O	3.3V tolerant 2.5V CMOS	
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to initiate a system reset. A system reset can also be initiated by software. Implemented as an open-drain output (two states; 0 or open circuit).	I/O	3.3V tolerant 2.5V CMOS	1, 2
$\overline{\text{Halt}}$	Halt from external debugger.	I	3.3V LVTTL	1, 4
TmrClk1	Processor timer external input clock.	I	3.3V tolerant 2.5V CMOS	
TmrClk2	This signal must be connected to a clock. It can be connected to any available clocking signal in the frequency range of 32kHz to 100MHz including TmrClk1.	I	3.3V tolerant 2.5V CMOS	
GPIO00:63	General purpose I/O 0 through 63. To access these functions, software must set DCR register bits.	I/O	Multiplex	
TestEn	Test Enable.	I	Multiplex	3
RcvrInh	Receiver Inhibit. Active only when TestEn is active.	I	Multiplex	
ModeCtrl	Mode Control.	I	Multiplex	
LeakTest	Leakage Test.	I	Multiplex	
RefEn	Reference Enable.	I	Multiplex	
DrvrInh1:2	Driver Inhibit. Used for test purposes only. Tie up as specified in Note 2 for normal operation.	I	3.3V tolerant 2.5V CMOS	2
PSROOut	Module characterization and screening.	O	Perf screen ring osc	1, 3

Table 7. Signal Functional Description (Sheet 8 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Trace Interface				
TrcBS0:2	Trace branch execution status.	I/O	3.3V tolerant 2.5V CMOS	
TrcClk	Trace data capture clock, runs at 1/4 the frequency of the processor.	O	3.3V tolerant 2.5V CMOSL	
TrcES0:4	Trace Execution Status is presented every fourth processor clock cycle.	I/O	3.3V LVTTL	
TrcTS0:6	Additional information on trace execution and branch status.	I/O	3.3V tolerant 2.5V CMOS	
Power				
V_{DD}	1.5V supply—Logic voltage.	na	na	
OV_{DD}	3.3V supply—I/O (except DDR SDRAM, Ethernet).	na	na	
SV_{DD}	2.5V supply—SDRAM, Ethernet.	na	na	
GND	Ground.	na	na	
AV_{DD}	1.5V—Filtered voltage for system PLLs (analog).	na	na	
AGND	PLL (analog) voltage ground.	na	na	
SAV_{DD}	1.5V—Filtered voltage for memory PLL (analog).	na	na	
SAGND	PLL (analog) memory voltage ground.	na	na	
Other				
Reserved	To avoid noise pickup problems, most of these balls must be connected in the board design as shown Table 6 on page 49.	na	na	

Device Characteristics

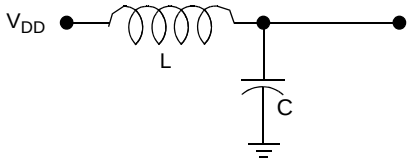
Table 8. Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specification contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit	Notes
Supply Voltage (Internal Logic)	V_{DD}	0 to +1.65	V	1
Supply Voltage (I/O, except SDRAM, Ethernet)	OV_{DD}	0 to +3.6	V	1
Supply Voltage (SDRAM, Ethernet)	SV_{DD}	0 to +2.7	V	
PLL Supply Voltage	AV_{DD}	0 to +1.65	V	2
SDRAM PLL Supply Voltage	SAV_{DD}	0 to +1.65	V	2
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to +3.6	V	
Storage Temperature Range	T_{STG}	-55 to +150	°C	
Case temperature under bias	T_C	-40 to +120	°C	3

Notes:

1. If $OV_{DD} \leq 0.4V$, it is required that $V_{DD} \leq 0.4V$. Supply excursions not meeting this criteria must be limited to less than 25ms duration during each power up or power down event.
2. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440GR. A separate filter, as shown below, is recommended for each voltage:



L – SMT ferrite bead chip, Murata BLM31A700S

C – 0.1µF ceramic

3. This value is not a specification of the operational temperature range, it is a stress rating only.

Table 9. Recommended DC Operating Conditions (Sheet 1 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	+1.4	+1.5	+1.6	V	4
I/O Supply Voltage	OV_{DD}	+3.0	+3.3	+3.6	V	4
SDRAM Supply Voltage	SV_{DD}	+2.3	+2.5	+2.7	V	4
PLL Supply Voltages	AV_{DD}	+1.4	+1.5	+1.6	V	3, 4
SDRAM PLL Voltage	SAV_{DD}	+1.4	+1.5	+1.6	V	3, 4
DDR SDRAM Reference Voltage	SV_{REF}	+1.15	+1.25	+1.35	V	2
Input Logic High (2.5V SSTL)	V_{IH}	SV_{REF}+0.18		SV_{DD}+0.3	V	
Input Logic High (2.5V CMOS, 3.3V tolerant receiver)		1.7		???	V	
Input Logic High (3.3V PCI)		$0.5OV_{DD}$		OV_{DD}+0.5	V	1
Input Logic High (3.3V LVTTL)		+2.0		+3.6	V	
Input Logic Low (2.5V SSTL)	V_{IL}	-0.3		SV_{REF}-0.18	V	
Input Logic Low (2.5V CMOS, 3.3V tolerant receiver)		???		0.7	V	
Input Logic Low (3.3V PCI)		-0.5		$0.35OV_{DD}$	V	1
Input Logic Low (3.3V LVTTL)		0		+0.8	V	
Output Logic High (2.5V SSTL)	V_{OH}	+1.95		SV_{DD}	V	
Output Logic High (2.5V CMOS, 3.3V tolerant receiver)		2.0		???	V	
Output Logic High (3.3V PCI)		$0.9OV_{DD}$		OV_{DD}	V	1
Output Logic High (3.3V LVTTL)		+2.4		OV_{DD}	V	
Output Logic Low (2.5V SSTL)	V_{OL}	0		0.55	V	
Output Logic Low (2.5V CMOS, 3.3V tolerant receiver)				0.4	V	
Output Logic Low (3.3V PCI)				$0.1OV_{DD}$	V	1
Output Logic Low (3.3V LVTTL)		0		+0.4	V	
Input Leakage Current (No pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for Pull-Down	I_{IL2}	0 (LPDL)		200 (MPUL)	µA	
Input Leakage Current for Pull-Up	I_{IL3}	-150 (LPDL)		0 (MPUL)	µA	
Input Max Allowable Overshoot (3.3V LVTTL)	V_{IMAO}			+3.9	V	
Input Max Allowable Undershoot (3.3V LVTTL)	V_{IMAU}	-0.6			V	
Output Max Allowable Overshoot (3.3V LVTTL)	V_{OMAO}			+3.9	V	
Output Max Allowable Undershoot (3.3V LVTTL)	V_{OMAU3}	-0.6			V	

Table 9. Recommended DC Operating Conditions (Sheet 2 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Temperature: 333MHz, 400MHz, and 533MHz parts 667MHz parts	T_C	 -40 -40		 +100 +85	°C	

Notes:

1. PCI drivers meet PCI specifications.
2. $SV_{REF} = SV_{DD}/2$
3. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440GR. See "Absolute Maximum Ratings" on page 58.

Power Sequencing

Startup sequencing of the power supply voltages is not required. However, a power-down cycle must complete (OV_{DD} and V_{DD} are below +0.4V) before a new power-up cycle is started.

Table 10. Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
Group 1 (2.5V SSTL I/O)	C_{IN1}	2.5	pF	
Group 2 (3.3V LVTTL I/O)	C_{IN2}	2.1	pF	
Group 3 (PCI I/O)	C_{IN3}	2.5	pF	
Group 4 (Receivers)	C_{IN4}	0.9	pF	
Group 5 (3.3V tolerant CMOS I/O)	C_{IN5}	2.4	pF	

Table 11. Typical DC Power Supply Requirements

Frequency (MHz)	+1.5V Supply (V_{DD}+AV_{DD}+SAV_{DD})	+2.5V Supply (SV_{DD})	+3.3V Supply (OV_{DD})	Total	Unit	Notes
333	1.00	1.15	0.04	2.19	W	1
400	1.09	1.15	0.04	2.28	W	1
533	1.28	1.15	0.04	2.47	W	1
667	1.93	1.15	0.04	3.12	W	1

Notes:

1. Typical Power is based on nominal voltage of V_{DD} = +1.5V, T_C = max. specified in Table 9 on page 59, while running Linux and a test application that exercises each core with representative traffic.

Table 12. V_{DD} Supply Power Dissipation

Frequency (MHz)	+1.4V	+1.5V	+1.6V	Unit	Notes
333	0.83	1.00	1.24	W	1
400	0.91	1.09	1.35	W	1
533	1.09	1.28	1.57	W	1
667	1.62	1.93	2.38	W	1

Notes:
1. Power is based on V_{DD} specified in the table and T_C = max. specified in Table 9 on page 59, while running Linux and a test application that exercises each core with representative traffic.

Table 13. DC Power Supply Loads

Parameter	Symbol	Typical	Maximum	Unit	Notes
V_{DD} (1.5V) active operating current	I_{DD}	1250	1900	mA	
OV_{DD} (3.3V) active operating current	I_{ODD}	10	100	mA	
SV_{DD} (2.5V) active operating current	I_{SDD}	460	600	mA	
AV_{DD} (1.5V) input current	I_{ADD}	3.2	5	mA	1
SAV_{DD} (1.5V) active operating current	I_{SADD}	6.05	10	mA	1

Notes:
1. See “Absolute Maximum Ratings” on page 58 for filter recommendations.
2. The maximum current values listed above are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results. V_{DD} current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, PCI, Ethernet, and so on). OV_{DD} current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.
3. Typical current is estimated at 667MHz with V_{DD} = +1.5V, OV_{DD} = +3.3V, SV_{DD} = +2.5V, and T_C = +85°C, while running Linux and a test application that exercises each core with representative traffic..
4. Maximum current is estimated at 667MHz with V_{DD} = +1.6V, OV_{DD} = +3.6V, SV_{DD} = +2.7V, and T_C = +85°C, and best-case process (which drives worst-case power), while running Linux and a test application that exercises each core with representative traffic.

Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized with V_{DD} = 1.5V, T_C = +85 °C and a 50pF test load as shown in the figure to the right.

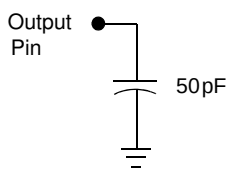


Table 14. Package Thermal Specifications

Thermal resistance values for the E-PBGA package are as follows:

Parameter	Symbol	Package	Airflow ft/min (m/sec)			Unit	Notes
			0 (0)	100 (0.51)	200 (1.02)		
Junction-to-ambient thermal resistance without heat sink	θ_{JA}	E-PBGA	20.0	18.7	17.9	°C/W	
		TE-PBGA	15.6	13.6	12.8	°C/W	
Junction-to-ambient thermal resistance with heat sink	θ_{JA}	E-PBGA	15.3	11.9	10.5	°C/W	
		TE-PBGA	13.9	10.4	9.0	°C/W	
			Resistance Value				
Junction-to-case thermal resistance	θ_{JC}	E-PBGA	8.3			°C/W	
		TE-PBGA	6.3			°C/W	
Junction-to-board thermal resistance	θ_{JB}	E-PBGA	14.3			°C/W	
		TE-PBGA	9.3			°C/W	

Notes:

1. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
2. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
3. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature (+125°C) and P is power consumption.
4. The preceding equations assume that the chip is mounted on a board with at least one signal and two power planes.
5. Values in the table were achieved with a JEDEC standard board: 114.5mm x 101.6mm x 1.6mm, 4 layers.
6. Values for an attached heat sink were achieved with a 35mm x 35mm x 15mm unit (see Thermal Management below), attached with a 0.1mm thickness of adhesive having a thermal conductivity of 1.3 W/mK.

Thermal Management

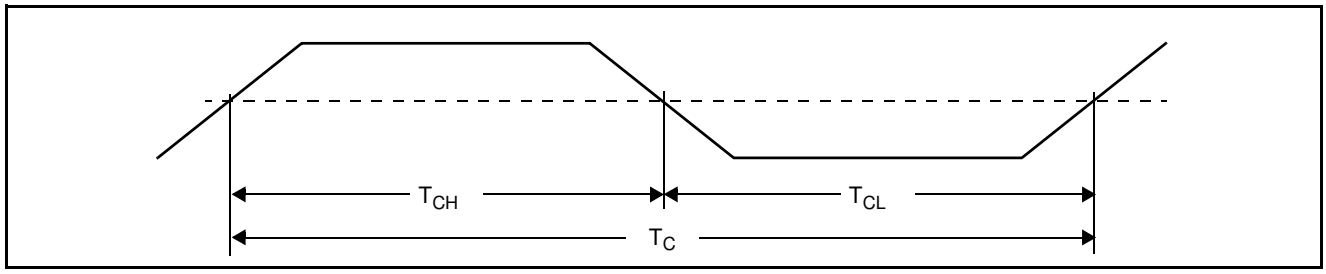
The following heat sinks were used in the above thermal analysis:
ALPHA W35-15W (35mm x 35mm x15mm)
ALPHA LPD35-15B (35mm x 35mm x15mm)

The heat sinks are manufactured by:
Alpha Novatech, Inc. (www.alphanovatech.com)
473 Sapena Court, #12
Santa Clara, CA 95054
Phone: 408-567-8082

Table 15. Clocking Specifications

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	Frequency	33.33	66.66	MHz
T_C	Period	15	30	ns
T_{CS}	Edge stability (cycle-to-cycle jitter)	–	±0.15	ns
T_{CH}	High time	40% of nominal period	60% of nominal period	ns
T_{CL}	Low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate ≥ 1 V/ns				
MemClkOut and PLB Clock				
F_C	Frequency	100	133.33	MHz
T_C	Period	7.5	10	ns
T_{CH}	High time	45% of nominal period	55% of nominal period	ns
PLL VCO				
F_C	Frequency	600	1334	MHz
T_C	Period	0.7496	1.66	ns
MAL Clock				
F_C	Frequency	45	83.33	MHz
T_C	Period	12	22.2	ns

Figure 4. Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC440GR. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC440GR the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC440GR with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board PPC440GR peripherals impose more stringent requirements.
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the DDR SDRAM MemClkOut since it also tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Important: It is up to the system designer to ensure that any SSCG used with the PPC440GR meets the above requirements and does not adversely affect other aspects of the system.

I/O Specifications

Table 16. Peripheral Interface Clock Timings

Parameter	Min	Max	Units	Notes
PCIClk input frequency (asynchronous mode)	–	66.66	MHz	
PCIClk period (asynchronous mode)	15	–	ns	
PCIClk input high time	40% of nominal period	60% of nominal period	ns	
PCIClk input low time	40% of nominal period	60% of nominal period	ns	
EMCMDClk output frequency	–	2.5	MHz	
EMCMDClk period	400	–	ns	
EMCMDClk output high time	160	–	ns	
EMCMDClk output low time	160	–	ns	
EMCTxClk input frequency MII(RMII)	2.5(5)	25(50)	MHz	
EMCTxClk period MII(RMII)	40(20)	400(200)	ns	
EMCTxClk input high time	35% of nominal period	–	ns	
EMCTxClk input low time	35% of nominal period	–	ns	
EMCRxClk input frequency MII(RMII)	2.5(5)	25(50)	MHz	
EMCRxClk period MII(RMII)	40(20)	400(200)	ns	
EMCRxClk input high time	35% of nominal period	–	ns	
EMCRxClk input low time	35% of nominal period	–	ns	
PerClk (and OPB Clock) output frequency (for ext. master or sync. slaves)	–	66.66	MHz	
PerClk period	15	–	ns	
PerClk output high time	50% of nominal period	66% of nominal period	ns	
PerClk output low time	33% of nominal period	50% of nominal period	ns	
UARTSerClk input frequency	–	$1000/(2T_{OPB}{}^{1}+2ns)$	MHz	1
UARTSerClk period	$2T_{OPB}+2$	–	ns	1
UARTSerClk input high time	$T_{OPB}+1$	–	ns	1
UARTSerClk input low time	$T_{OPB}+1$	–	ns	1
TmrClk1 input frequency	–	100	MHz	2
TmrClk1 period	10	–	ns	
TmrClk1 input high time	40% of nominal period	60% of nominal period	ns	
TmrClk1 input low time	40% of nominal period	60% of nominal period	ns	

Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at 1/2 the frequency of the PLB clock. The maximum OPB clock frequency is 66.66 MHz.
2. See Table 7 for information on the TmrClk2 signal.

Figure 5. Input Setup and Hold Waveform

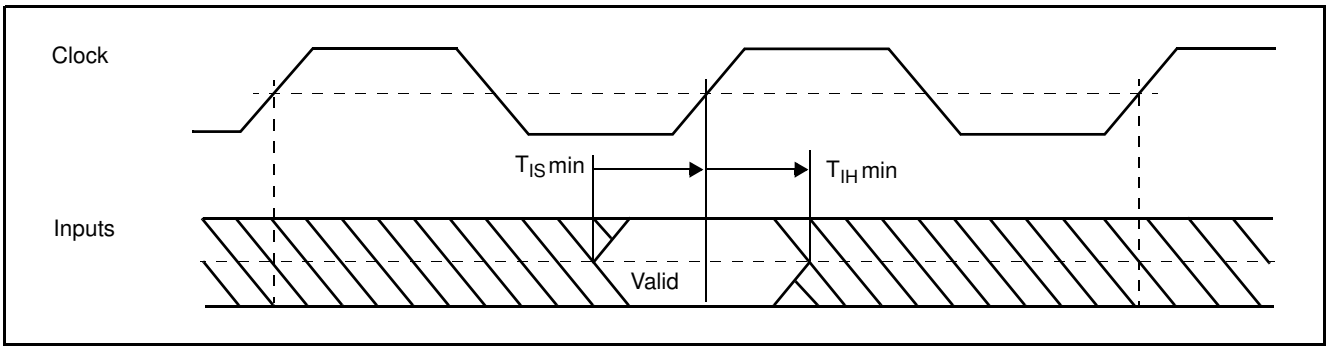


Figure 6. Output Delay and Float Timing Waveform

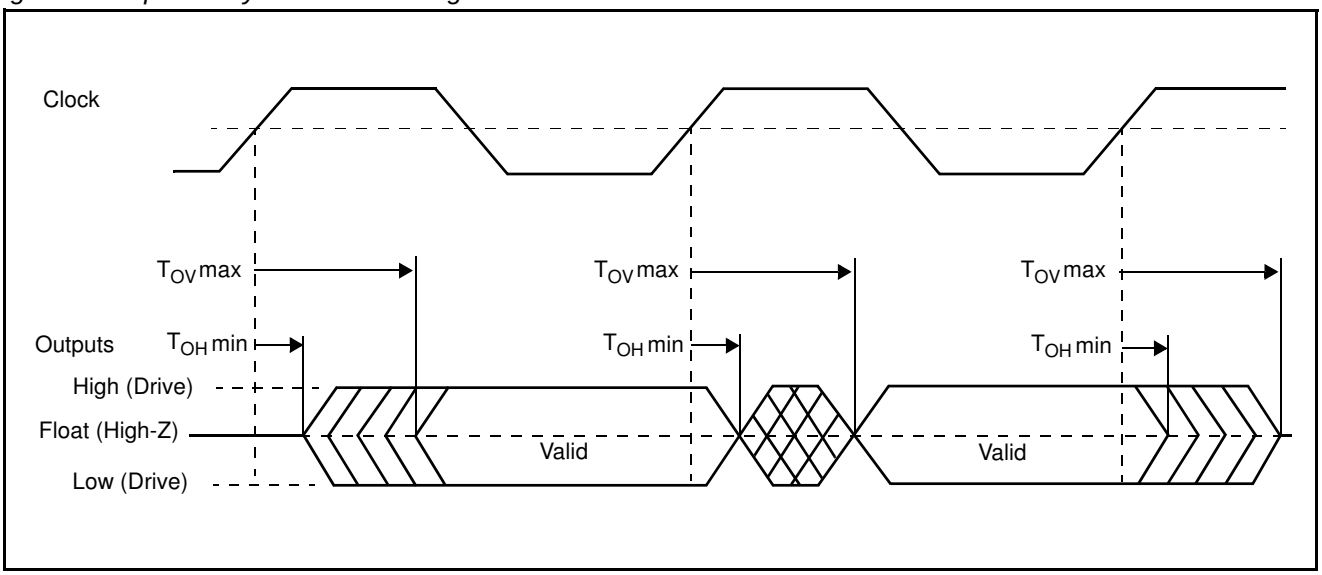


Table 17. I/O Specifications—All Speeds (Sheet 1 of 2)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
PCI Interface								
PCIAD31:00	5	0	6	2	0.5	1.5	PCIClk	
PCIC3:0/BE3:0	5	0	6	2	0.5	1.5	PCIClk	
PCIClk	dc	dc			na	na		async
PCIDevSel	5	0	6	2	0.5	1.5	PCIClk	
PCIFrame	5	0	6	2	0.5	1.5	PCIClk	
PCIGnt0:5	n/a	n/a	6	2	0.5	1.5	PCIClk	
PCIIDSel	5	0	n/a	n/a	na	na	PCIClk	
PCIINT	n/a	n/a	6	2	0.5	1.5	PCIClk	async
PCIIRDY	5	0	6	2	0.5	1.5	PCIClk	
PCIPar	5	0	6	2	0.5	1.5	PCIClk	
PCIPErr	5	0	6	2	0.5	1.5	PCIClk	
PCIReq0:5	5	0	n/a	n/a	na	na	PCIClk	
PCIReset	n/a	n/a	n/a	n/a	na	na	PCIClk	
PCISErr	5	0	6	2	0.5	1.5	PCIClk	
PCIStop	5	0	6	2	0.5	1.5	PCIClk	
PCITRDY	5	0	6	2	0.5	1.5	PCIClk	
Ethernet MII Interface								
EMCCD	10	10	n/a	n/a	5.1	6.8		1, async
EMCCrS	10	10	n/a	n/a	5.1	6.8		1, async
EMCDV	10	10	n/a	n/a	5.1	6.8		
EMCMDClk					5.1	6.8		1, async
EMCMDIO	10	10	20	0	5.1	6.8	EMCMDClk	1
EMCRxClk	n/a	n/a	n/a	n/a	5.1	6.8		1, async
EMCRxD0:3	10	10	n/a	n/a	5.1	6.8	EMCRxClk	1
EMCRxErr	10	10	n/a	n/a	5.1	6.8	EMCRxClk	1
EMCTxClk	n/a	n/a	n/a	n/a	na	na		1, async
EMCTxD0:3	n/a	n/a	20	0	5.1	6.8	EMCTxClk	1
EMCTxEn	n/a	n/a	20	0	5.1	6.8	EMCTxClk	1
EMCTxErr	n/a	n/a	20	0	5.1	6.8	EMCTxClk	1
Ethernet RMII Interface								
EMC0CRSDV	4	2	n/a	n/a				
EMC0RxD0:1	4	2	n/a	n/a	5.1	6.8	EMCRefClk	1
EMC0RxErr	4	2	n/a	n/a	5.1	6.8	EMCRefClk	1
EMC0TxD0:1	n/a	n/a	12.5	0	5.1	6.8	EMCRefClk	1
EMC1CRSDV	4	2	n/a	n/a				
EMC1RxD0:1	4	2	n/a	n/a	5.1	6.8	EMCRefClk	1
EMC1RxErr	4	2	n/a	n/a	5.1	6.8	EMCRefClk	1
EMC1TxD0:1	n/a	n/a	12.5	0	5.1	6.8	EMCRefClk	1
EMCRefClk	n/a	n/a	n/a	n/a	5.1	6.8		1, async
Ethernet SMII Interface								
EMC0RxD	1.5	1	n/a	n/a	5.1	6.8	EMCRefClk	1
EMC0TxD	n/a	n/a	3.5	0	5.1	6.8	EMCRefClk	1
EMC1RxD	1.5	1	n/a	n/a	5.1	6.8	EMCRefClk	1
EMC1TxD	n/a	n/a	3.5	0	5.1	6.8	EMCRefClk	1
EMCRefClk	n/a	n/a	n/a	n/a	5.1	6.8		1, async

Table 17. I/O Specifications—All Speeds (Sheet 2 of 2)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Internal Peripheral Interface								
IIC0SClk	n/a	n/a	5	0	15.3	10.2		
IIC0SData	n/a	n/a	5	0	15.3	10.2		
IIC1SClk					15.3	10.2		
IIC1SData					15.3	10.2		
SCPClkOut	7	2	6	0	15.3	10.2		
SCPDI	7	2	n/a	n/a	15.3	10.2		
SCPDO	n/a	n/a	6	0	15.3	10.2		
UARTSerClk	n/a	n/a	n/a	n/a	na	na		
UARTn_Rx	n/a	n/a	n/a	n/a	na	na		
UARTn_Tx	n/a	n/a	n/a	n/a	10.3	7.1		
$\overline{\text{UARTn\_DCD}}$	n/a	n/a	n/a	n/a	na	na		
$\overline{\text{UARTn\_DSR}}$	n/a	n/a	n/a	n/a	na	na		
$\overline{\text{UARTn\_CTS}}$	n/a	n/a	n/a	n/a	na	na		
$\overline{\text{UARTn\_DTR}}$	n/a	n/a	n/a	n/a	10.3	7.1		
$\overline{\text{UARTn\_RI}}$	n/a	n/a	n/a	n/a	na	na		
$\overline{\text{UARTn\_RTS}}$	n/a	n/a	n/a	n/a	10.3	7.1		
Interrupts Interface								
IRQ0:9	n/a	n/a	n/a	n/a	na	na		
JTAG Interface								
TCK	n/a	n/a	n/a	n/a	na	na		async
TDI	n/a	n/a	n/a	n/a	na	na		async
TDO	n/a	n/a	n/a	n/a	15.3	10.2		async
TMS	n/a	n/a	n/a	n/a	na	na		async
$\overline{\text{TRST}}$	n/a	n/a	n/a	n/a	na	na		async
System Interface								
SysClk	n/a	n/a	n/a	n/a	na	na		
TmrClk1:2	n/a	n/a	n/a	n/a	na	na		async
$\overline{\text{SysReset}}$	n/a	n/a	n/a	n/a	na	na		async
$\overline{\text{Halt}}$	n/a	n/a	n/a	n/a	na	na		async
$\overline{\text{SysErr}}$	n/a	n/a	n/a	n/a	10.3	7.1		async
$\overline{\text{TestEn}}$	n/a	n/a	n/a	n/a	na	na		async
DrvrInh1:2	n/a	n/a	n/a	n/a	na	na		
RcvrInh	n/a	n/a	n/a	n/a				
GPIO00:63	n/a	n/a	n/a	n/a	10.3	7.1		
PSROOut	n/a	n/a	n/a	n/a				
Trace Interface								
TrcClk	n/a	n/a	n/a	n/a	10.3	7.1		
TrcBS0:2	n/a	n/a	n/a	n/a	10.3	7.1		
TrcES0:4	n/a	n/a	n/a	n/a	10.3	7.1		
TrcTS0:6	n/a	n/a	n/a	n/a	10.3	7.1		

Table 18. I/O Specifications—333MHz to 533MHz

Notes:
1. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 1.3ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
External Slave Peripheral Interface								
DMAAck0:1	n/a	n/a	10	1	5.1	6.8	PerClk	
DMAAck2:3	n/a	n/a	10	1	15.3	10.2	PerClk	
DMAReq0:3	11.7	0.5	n/a	n/a	na	na	PerClk	
EOT0:1/TC0:1	11.7	0.5	10	1	5.1	6.8	PerClk	
EOT2:3/TC2:3	11.7	0.5	10	1	15.3	10.2	PerClk	
PerAddr02:31	4	1	7.2	1.5	15.3	10.2	PerClk	
PerBLast	4	1	6.5	1.5	15.3	10.2	PerClk	
PerCS0:5	n/a	n/a	6.5	1.5	10.3	7.1	PerClk	
PerData00:15	4	1	7.2	1.5	15.3	10.2	PerClk	
PerOE	n/a	n/a	6.5	1.5	15.3	10.2	PerClk	
PerReady	6	1	n/a	n/a	15.3	10.2	PerClk	
PerR/W	4	1	6.5	1.5	15.3	10.2	PerClk	
PerWBE0:1	4	1	6.5	1.5	15.3	10.2	PerClk	
External Master Peripheral Interface								
BusReq	n/a	n/a	6.5	1.5	7.1	9.6	PerClk	
ExtAck	n/a	n/a	6.5	1.5	7.1	9.6	PerClk	
ExtReq	4	1	n/a	n/a	n/a	n/a	PerClk	
ExtReset	n/a	n/a	6.0	1.5	15.3	10.2	PerClk	
HoldAck	n/a	n/a	6.5	1.5	7.1	9.6	PerClk	
HoldReq	4	1	n/a	n/a	na	na	PerClk	
HoldPri	4	1	n/a	n/a	na	na		
PerClk	n/a	n/a	n/a	n/a	15.3	10.2	PLB Clk	1
PerErr	6	1	n/a	n/a	10.3	7.1	PerClk	
NAND Flash Interface								
NFALE	n/a	n/a	6.5	1.5	5.1	6.8		
NFCE0:3	n/a	n/a	6.5	1.5	10.3	7.1		
NFCLE	n/a	n/a	6.5	1.5	5.1	6.8		
NFRdyBusy	4	1	n/a	n/a	na	na		
NFREn	n/a	n/a	6.5	1.5	5.1	6.8		
NFWEn	n/a	n/a	6.5	1.5	5.1	6.8		

DDR SDRAM I/O Specifications

The DDR SDRAM controller times its operation with internal PLB clock signals and generates MemClkOut0 from the PLB clock. The PLB clock is an internal signal that cannot be directly observed. However MemClkOut0 is the same frequency as the PLB clock signal and is in phase with the PLB clock signal.

Note: MemClkOut0 can be advanced with respect to the PLB clock by means of the SDRAM0_CLKTR programming register. In a typical system, users advance MemClkOut by 90°. This depends on the specific application and requires a thorough understanding of the memory system in general (refer to the DDR SDRAM controller chapter in the *PowerPC 440GR User's Manual*).

In the following sections, the label MemClkOut0(0) refers to MemClkOut0 when it has not been phase-shifted, and MemClkOut0(90) refers to MemClkOut0 when it has been phase-advanced 90°. Advancing MemClkOut0 by 90° creates a 3/4 cycle setup time and 1/4 cycle hold time for the address and control signals in relation to MemClkOut0(90). The rising edge of MemClkOut0(90) aligns with the first rising edge of the DQS signal.

The following DDR data is generated by means of simulation and includes logic, driver, package RLC, and lengths. Values are calculated over best case and worst case processes with speed, temperature, and voltage as follows:

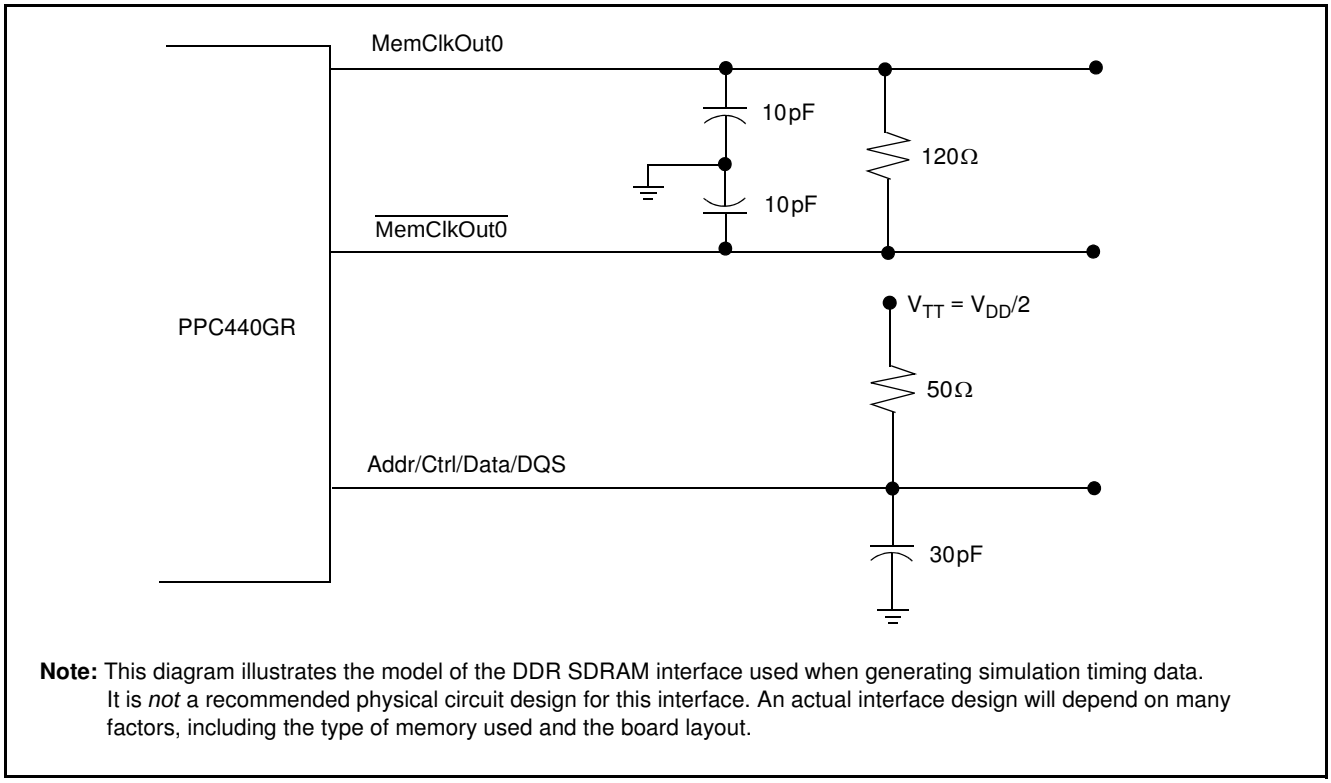
Best Case = Fast process, -40°C, +1.6V

Worst Case = Slow process, +85°C, +1.4V

Note: In all the following DDR tables and timing diagrams, *minimum* values are measured under *best* case conditions and *maximum* values are measured under *worst* case conditions.

The signals are terminated as indicated in the figure below for the DDR timing data in the following sections.

Figure 7. DDR SDRAM Simulation Signal Termination Model



Note: This diagram illustrates the model of the DDR SDRAM interface used when generating simulation timing data. It is *not* a recommended physical circuit design for this interface. An actual interface design will depend on many factors, including the type of memory used and the board layout.

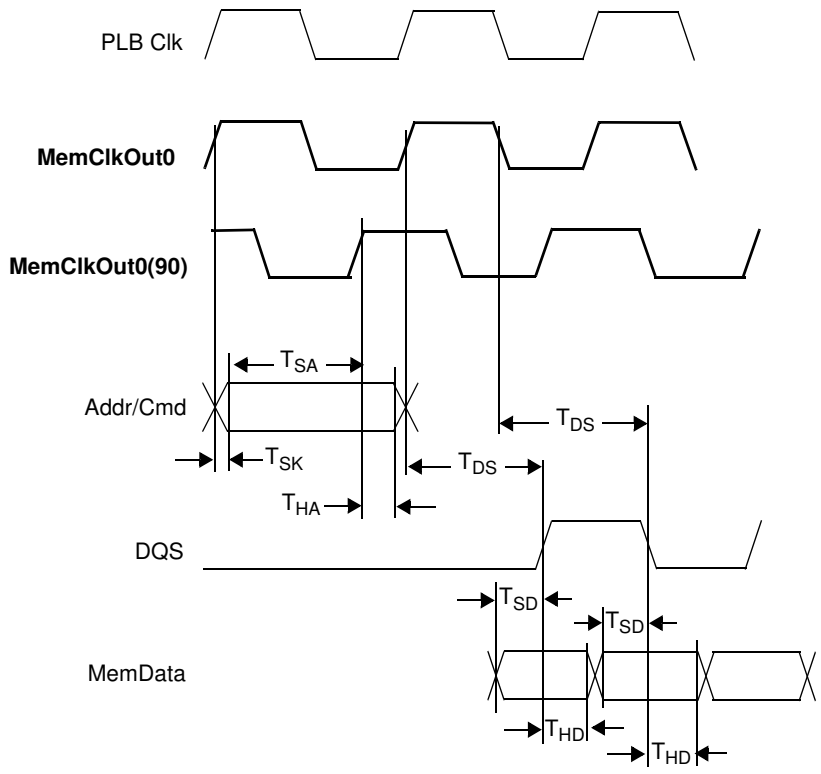
Table 19. DDR SDRAM Output Driver Specifications

Signal Path	Output Current (mA)	
	I/O H (maximum)	I/O L (minimum)
Write Data		
MemData00:07	15.2	15.2
MemData08:15	15.2	15.2
MemData16:23	15.2	15.2
MemData24:31	15.2	15.2
ECC0:7	15.2	15.2
DM0:8	15.2	15.2
MemClkOut0	15.2	15.2
MemAddr00:12	15.2	15.2
BA0:1	15.2	15.2
$\overline{\text{RAS}}$	15.2	15.2
$\overline{\text{CAS}}$	15.2	15.2
$\overline{\text{WE}}$	15.2	15.2
$\overline{\text{BankSel0:3}}$	15.2	15.2
ClkEn0:3	15.2	15.2
DQS0:8	15.2	15.2

DDR SDRAM Write Operation

The following diagram illustrates the relationship among the signals involved with a DDR write operation.

Figure 8. DDR SDRAM Write Cycle Timing



T_{SK} = Delay from rising edge of MemClkOut0(0) to rising/falling edge of signal (skew)
T_{SA} = Setup time for address and command signals to MemClkOut0(90)
T_{HA} = Hold time for address and command signals from MemClkOut0(90)
T_{SD} = Setup time for data signals (minimum time data is valid *before* rising/falling edge of DSQ)
T_{HD} = Hold time for data signals (minimum time data is valid *after* rising/falling edge of DSQ)
T_{DS} = Delay from rising/falling edge of clock to the rising/falling edge of DQS

Note: The timing data in the following tables is based on simulation runs using Einstimer.

Table 20. I/O Timing—DDR SDRAM T_{DS}

Notes:
1. All of the DQS signals are referenced to MemClkOut0(0).
2. Clock speed is 133MHz.
3. The T_{DS} values in the table include 3/4 of a cycle at 133MHz (7.5ns x 0.75 = 5.625 ns).
4. To obtain adjusted values for lower clock frequencies, subtract 5.625 ns from the values in the table and add 3/4 of the cycle time for the lower clock frequency (T_{DS} - 5.625 + 0.75T_{CYC}).

Signal Name	T_{DS} (ns)	
	Minimum	Maximum
DQS0	5.76	5.86
DQS1	5.78	5.91
DQS2	5.82	5.90
DQS3	5.79	5.89
DQS8	5.75	5.88

Table 21. I/O Timing—DDR SDRAM T_{SK}, T_{SA}, and T_{HA}

Notes:
1. Clock speed is 133MHz. T_{SK} is referenced to MemClkOut0(0). T_{SA} and T_{HA} are referenced to MemClkOut0(90).
2. To obtain adjusted T_{SA} values for lower clock frequencies, use 3/4 of the cycle time for the lower clock frequency and subtract T_{SK} maximum (0.75T_{CYC} - T_{SK}max).
3. To obtain adjusted T_{HA} values for lower clock frequencies, use 1/4 of the cycle time for the lower clock frequency and add T_{SK} minimum (0.25T_{CYC} + T_{SK}min).

Signal Name	T_{SK} (ns)		T_{SA} (ns)	T_{HA} (ns)
	Minimum	Maximum	Minimum	Minimum
MemAddr00:12	0.11	0.32	5.31	1.99
BA0:1	0.07	0.31	5.32	1.95
BankSel0:3	0.05	0.25	5.38	1.93
ClkEn0:3	0.07	0.28	5.35	1.95
$\overline{CAS}$	0.05	0.31	5.32	1.93
$\overline{RAS}$	0.05	0.28	5.35	1.93
$\overline{WE}$	0.08	0.22	5.41	1.96

Table 22. I/O Timing—DDR SDRAM T_{SD} and T_{HD}

Notes:
1. T_{SD} and T_{HD} are measured under worst case conditions.
2. Clock speed for the values in the table is 133MHz.
3. The time values in the table include 1/4 of a cycle at 166MHz (7.5ns x 0.25 = 1.875 ns).
4. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 1.875 ns from the values in the table and add 1/4 of the cycle time for the lower clock frequency (e.g., T_{SD} - 1.875 + 0.25T_{CYC}).

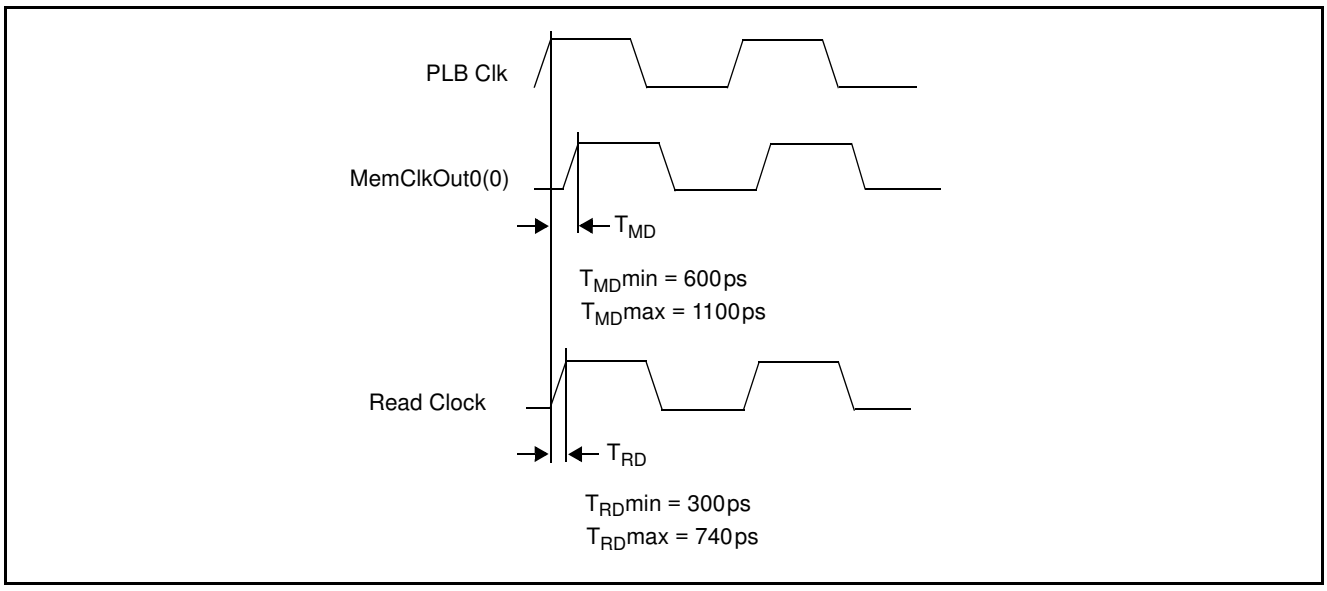
Signal Names	Reference Signal	T_{SD} (ns)	T_{HD} (ns)
MemData00:07, DM0	DQS0	1.795	1.866
MemData08:15, DM1	DQS1	1.775	1.865
MemData16:23, DM2	DQS2	1.745	1.862
MemData24:31, DM3	DQS3	1.765	1.864
ECC0:7, DM8	DQS8	1.685	1.857

DDR SDRAM Read Operation

The following examples of timing for DDR SDRAM read operations are based on the relationship between the incoming data and the PLB clock signal. Since the PLB clock cannot be directly observed, the delay of MemClkOut(0) relative to the PLB clock (T_{MD}) is provided.

The internal Read Clock signal, like MemClkOut0, is derived from the PLB clock and can be delayed relative to the PLB clock by programming the RDCT and RDCD fields in the SDRAM0_TR1 register. The delay can be programmed from 0 to 1/2 cycle in steps using RDCT. Setting RDCD results in a 1/2 cycle delay plus the value set in RDCT. The delay of Read Clock relative to the PLB clock (T_{RD}) shown below assumes the programmable Read Clock delay is set to zero.

Figure 9. DDR SDRAM MemClkOut0 and Read Clock Delay



In operation, following the receipt of an address and read command from the PPC440GR, the SDRAM generates data and the DQS signals coincident with MemClkOut0. The data is latched into the PPC440GR using a DQS signal that is delayed 1/4 of a cycle. In order to accommodate timing variations introduced by the system designs using this chip, the three-stage data path shown below is used to eliminate metastability and allow data sampling to be adjusted for minimum latency. This adjustment requires programming the Read Clock delay and the selection of Stage 1, Stage 2, or Stage 3 data for sampling at RDSP.

Figure 10. DDR SDRAM Read Data Path

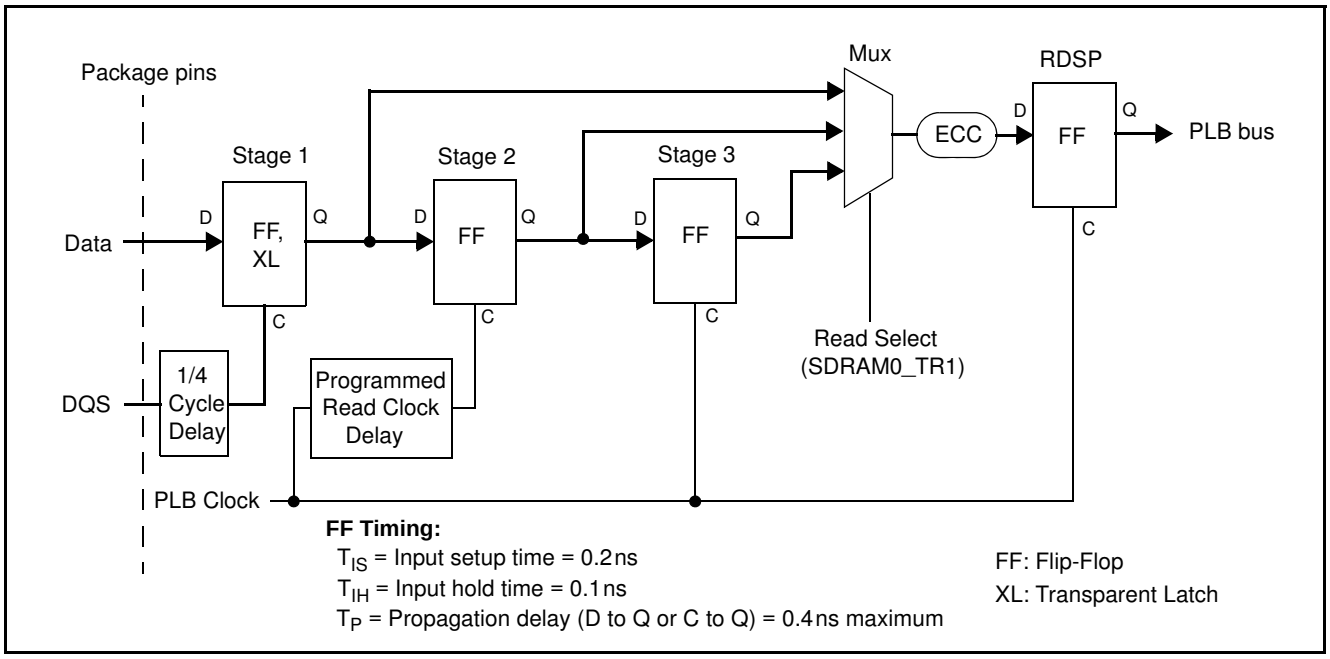


Table 23. I/O Timing—DDR SDRAM T_{SIN} and T_{DIN}

Notes:
1. T_{SIN} = Delay from DQS at package pin to C on Stage 1 FF.
2. T_{DIN} = Delay from data at package pin to D on Stage 1 FF.
3. Clock speed for the values in the table is 133MHz.
4. The time values for T_{SIN} include 1/4 of a cycle at 133MHz (7.5ns x 0.25 = 1.875 ns).

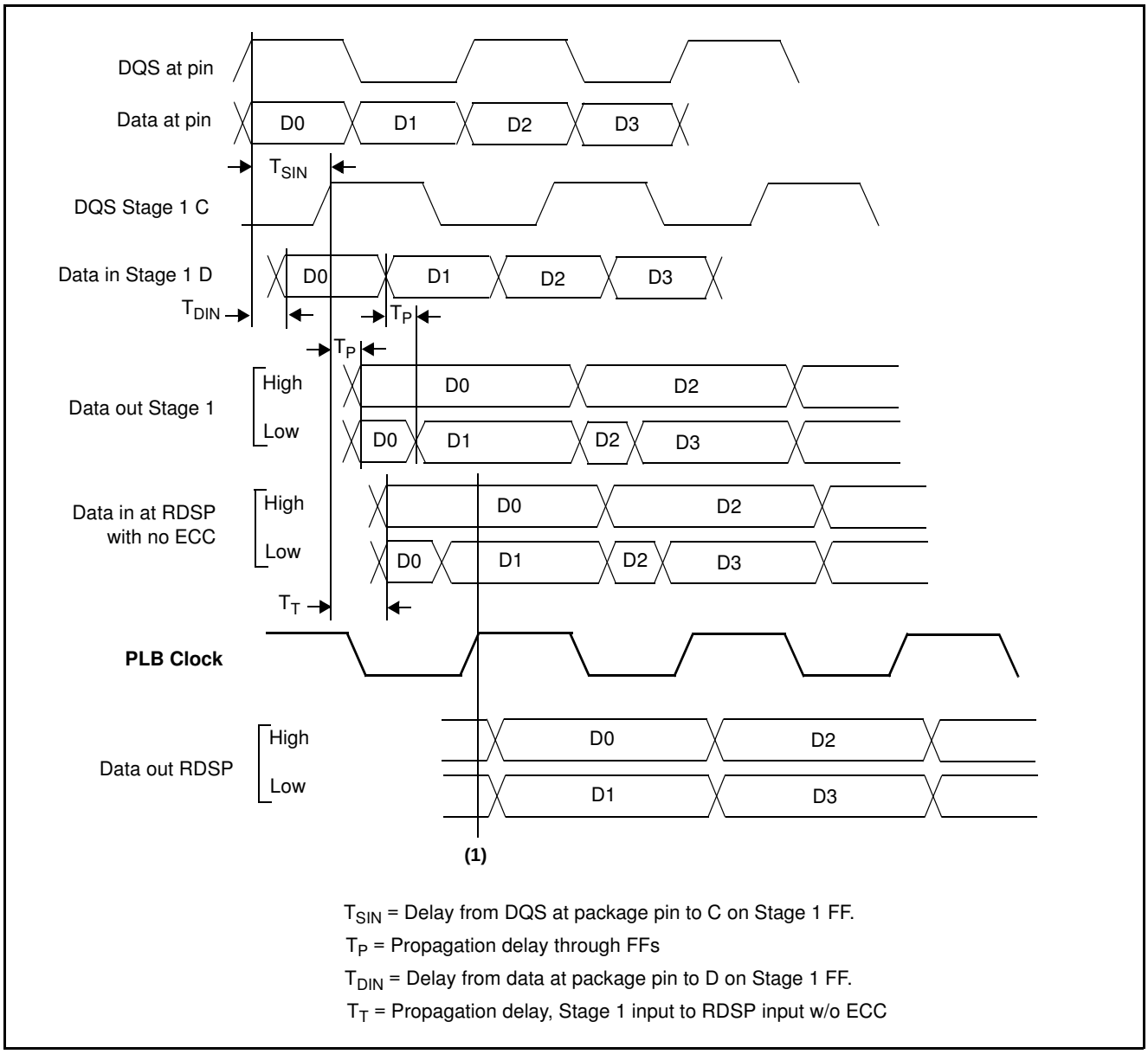
Signal Name	T_{SIN} (ns) minimum	T_{SIN} (ns) maximum	Signal Name	T_{DIN} (ns) minimum	T_{DIN} (ns) maximum
DQS0	2.74	3.70	MemData00:07	0.86	1.87
DQS1	2.75	3.69	MemData08:15	0.87	1.86
DQS2	2.74	3.69	MemData16:23	0.89	1.86
DQS3	2.76	3.69	MemData24:31	0.88	1.85
DQS8	2.77	3.68	ECC0:7	0.89	1.83

In the following examples, the data strobes (DQS) and the data are shown to be coincident. There is actually a slight skew as specified by the SDRAM specifications, and there can be additional skew due to loading and signal routing. It is recommended that the signal length for all of the eight DQS signals be matched.

Example 1:

If the data-to-PLB clock timing is as shown in the example below, then the read clock is not delayed and the Stage 1 data is sampled at **(1)**. Except for small, low frequency memory systems with the memory located physically close to the PPC440GR, it is unlikely that Stage 1 data can be sampled. When the data comes later, it is necessary to sample Stage 2 or Stage 3 data. (see Examples 2 and 3). Another way to get the desired data-to-PLB timing to allow Stage 1 sampling is to buffer MemClkOut0 and skew it enough to guarantee the timing. In this example, T_T is controlled and set by the software.

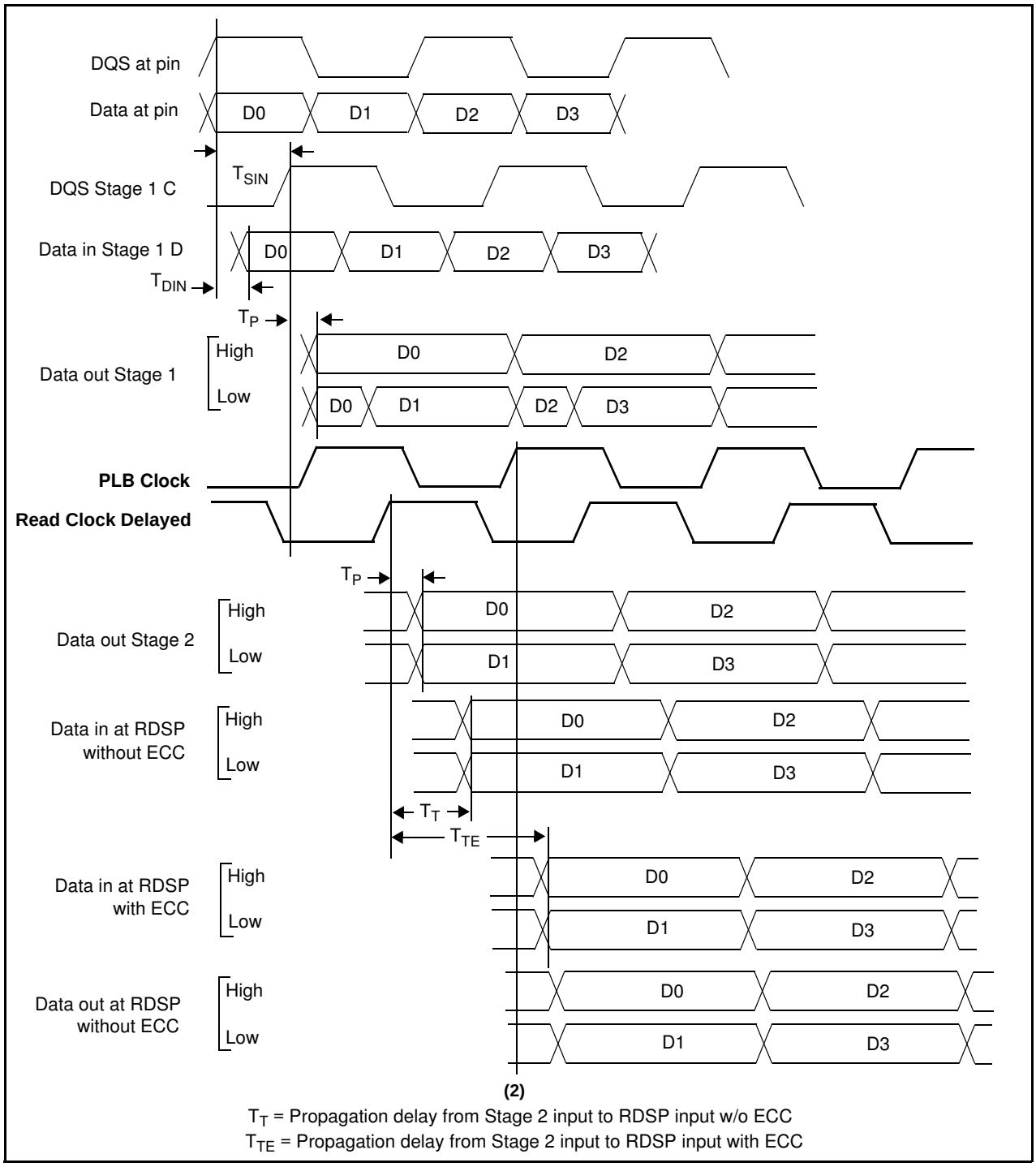
Figure 11. DDR SDRAM Read Cycle Timing—Example 1



Example 2:

In this example Read Clock is delayed almost 1/2 cycle. Without ECC, Stage 2 data can be sampled at **(2)**. If ECC is enabled, Stage 3 data must be sampled (see Example 3). In this example, T_T and T_{TE} are controlled and set by the software.

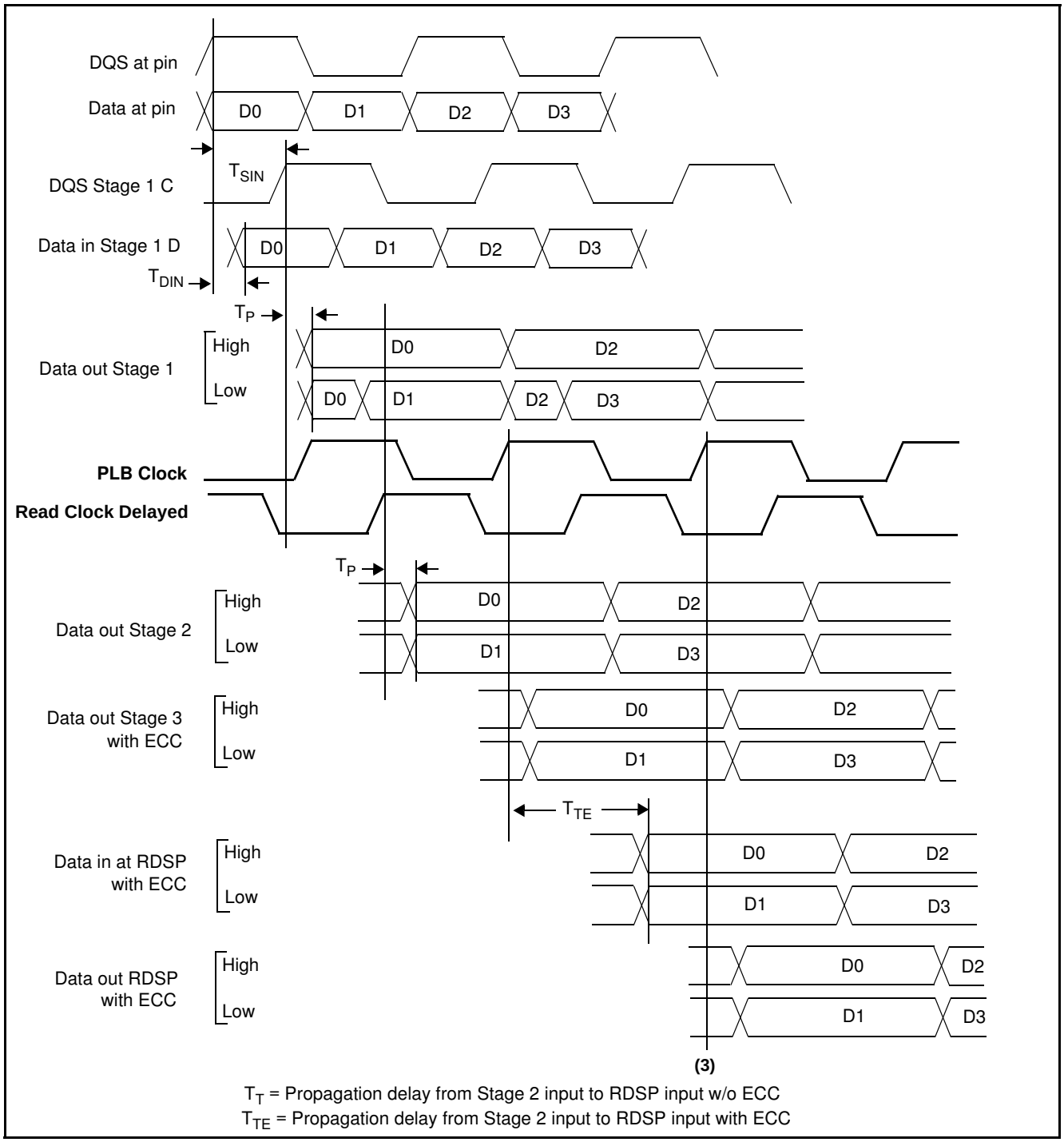
Figure 12. DDR SDRAM Read Cycle Timing—Example 2



Example 3:

In this example, ECC is enabled. This requires that Stage 3 data be sampled at **(3)**. If ECC is disabled, the system will still work, but there will be more latency before the data is sampled into RDSP. In this example, T_T and T_{TE} are controlled and set by the software.

Figure 13. DDR SDRAM Read Cycle Timing—Example 3



Initialization

The PPC440GR provides the option for setting initial parameters based on default values or by reading them from a slave PROM attached to the IIC0 bus (see “Serial EEPROM” below). Some of the default values can be altered by strapping on external pins (see “Strapping” below).

Strapping

While the $\overline{\text{SysReset}}$ input pin is low (system reset), the state of certain I/O pins is read to enable certain default initial conditions prior to PPC440GR start-up. The actual capture instant is the nearest reference clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. These pins are used for strap functions only during reset. Following reset they are used for normal functions. The signal names assigned to the pins for normal operation are shown in parentheses following the pin number.

The following table lists the strapping pins along with their functions and strapping options:

Table 24. Strapping Pin Assignments

Function	Option	Ball Strapping		
		R25 (UART0_DCD)	U26 (UART0_DSR)	V26 (UART0_CTS)
Serial device is disabled. Each of the six options (A–F) is a combination of boot source, boot-source width, and clock frequency specifications. Refer to the IIC Bootstrap Controller chapter in the *PPC440GR Embedded Processor User's Manual* for details.	A	0	0	0
	B	0	0	1
	C	0	1	0
	D	0	1	1
	E	1	0	0
	F	1	1	0
Serial device is enabled. The option being selected is the IIC0 slave address that will respond with strapping data. **Note:** If reading of configuration data from the serial device fails, the PPC440GR defaults to configuration X.	G (0xA8)	1	0	1
	H (0xA4)	1	1	1

Serial EEPROM

During reset, initial conditions other than those obtained from the strapping pins can be read from a ROM device connected to the IIC0 port. At the de-assertion of reset, if the bootstrap controller is enabled, the PPC440GR sequentially reads 16 B from the ROM device on the IIC0 port and sets the SDR0_SDSTP0, SDR0_SDSTP1, SDR0_SDSTP2 and SDR0_SDSTP3 registers accordingly.

The initialization settings and their default values are covered in detail in the *PowerPC 440GR User's Manual*.

Revision Log

Date	Version	Contents of Modification
01/12/2005		Initial creation of document.
01/27/2005		Restore second DMA controller and make PVR and JTAG ID same as 440EP.
01/31/2005		Update DDR SDRAM timing.
03/03/2005		Update I/O definitions. Misc. corrections
03/30/2005		Remove 400MHz and 466MHz part numbers.
04/18/2005		Remove reference to USB end points.
04/28/2005		Update DDR SDRAM timing.
05/09/2005		Update reserved signals and add description of TmrClk2.
05/18/2005		Correct specs regarding the frequency range allowed for TmrClk2.
06/06/2005	1.08	Change description of TmrClk2.
07/11/2005	1.09	Add RoHS comliance statement and change maximum NAND Flash to 256MB.
07/20/2005		Misc. changes.
08/05/2005		Change solder ball size specification.
09/21/2005		Add power dissipation values for all supply voltages at the CPU speeds supported.
09/22/2005	1.10	Transfer applicable data (input capacitance, thermal performace, etc.) from 400EP data sheet.
10/06/2005	1.11	Misc. changes.
10/10/2005	1.12	Add 400Mhz CPU speed back into available PN list.
11/18/2005	1.13	Add default configuration X when bootstrap IIC read fails to Table 24. Add package nomenclature. Correct MemClkOut duty cycle. Correct description and move PerErr signal from master to slave. Change maximum VCO freqruency to 1334MHz.
02/16/2006	1.14	Add revision level B (1.1) part numbers and PVR numbers.
05/24/2006	1.15	Update power dissipation and add additional temperature data.
07/19/2006	1.16	Correct enable/disable specifications for PCI Gnt/Req signals.

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Preliminary Edition (August 4, 2006)

This document contains information on a new product under development by AMCC.
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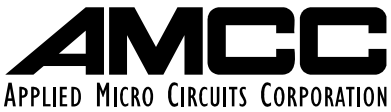

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