
HM5164165 Series HM5165165 Series

64M EDO DRAM (4-Mword $\times$ 16-bit)
8k Refresh/4k Refresh

HITACHI

ADE-203-802B(Z)
Rev. 1.0
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Description

The Hitachi HM5164165 Series, HM5165165 Series are 64M-bit dynamic RAMs organized as 4,194,304-word $\times$ 16-bit. They have realized high performance and low power by employing CMOS process technology. HM5164165 Series, HM5165165 Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. They have the package variations of standard 50-pin plastic SOJ and standard 50-pin plastic TSOPII

Features

- Single 3.3 V supply: 3.3 V $\pm$ 0.3 V
- Access time: 50 ns/60 ns (max)
- Power dissipation
 - Active: 432 mW/396 mW (max) (HM5164165 Series)
 : 504 mW/432 mW (max) (HM5165165 Series)
 - Standby: 1.8 mW (max) (CMOS interface)
 : 0.54 mW (max) (L-version)
- EDO page mode capability
- Refresh cycles
 - $\overline{\text{RAS}}$ -only refresh
 - 8192 cycles /64 ms (HM5164165)
 /128 ms (HM5164165L) (L-version)
 - 4096 cycles /64 ms (HM5165165)
 /128 ms (HM5165165L) (L-version)
 - CBR/Hidden refresh
 - 4096 cycles /64 ms (HM5164165, HM5165165)
 /128 ms (HM5164165L, HM5165165L) (L-version)

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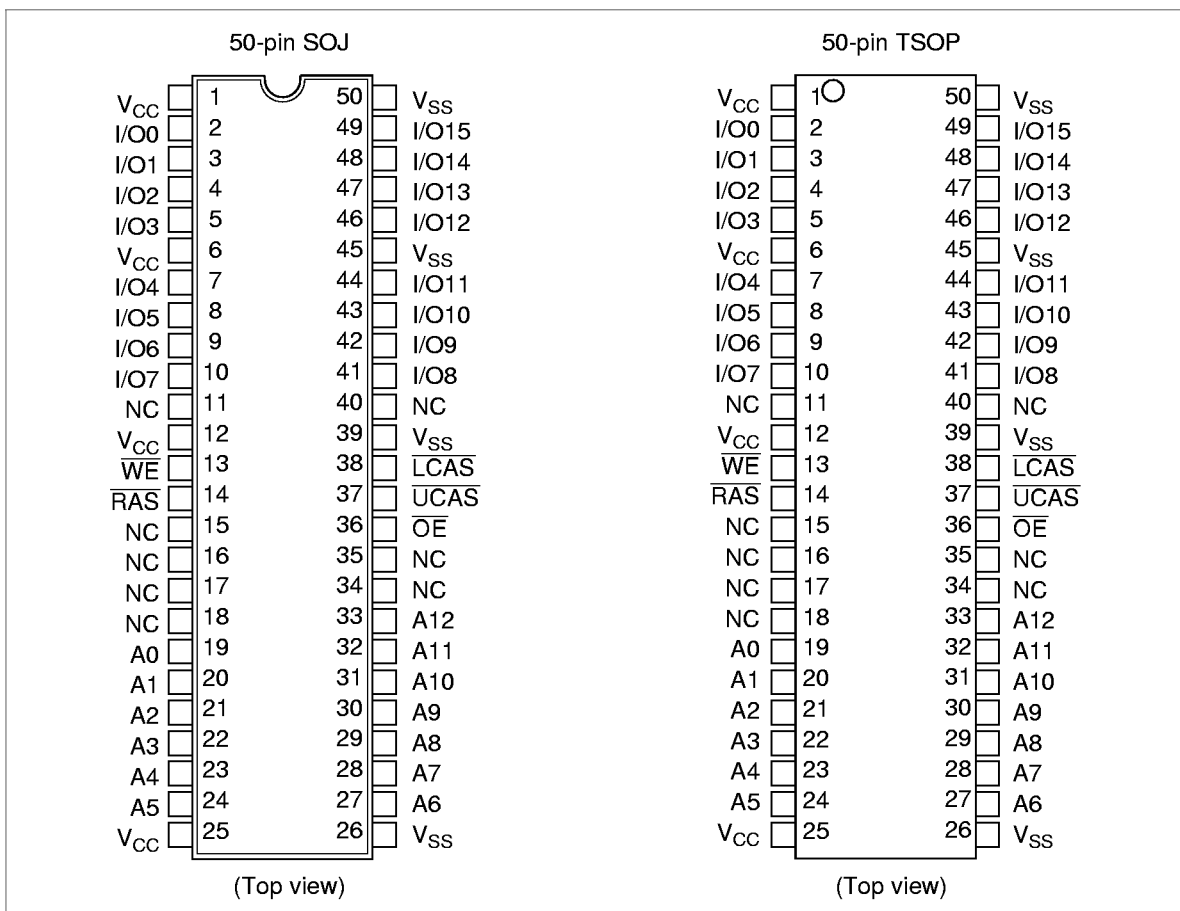
- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)
- 2CAS-byte control
- Battery backup operation (L-version)

Ordering Information

Type No.	Access time	Package
HM5164165J-5	50 ns	400-mil 50-pin plastic SOJ (CP-50DA)
HM5164165J-6	60 ns	
HM5164165LJ-5	50 ns	
HM5164165LJ-6	60 ns	
HM5165165J-5	50 ns	
HM5165165J-6	60 ns	
HM5165165LJ-5	50 ns	
HM5165165LJ-6	60 ns	
HM5164165TT-5	50 ns	400-mil 50-pin plastic TSOP II (TTP-50DB)
HM5164165TT-6	60 ns	
HM5164165LTT-5	50 ns	
HM5164165LTT-6	60 ns	
HM5165165TT-5	50 ns	
HM5165165TT-6	60 ns	
HM5165165LTT-5	50 ns	
HM5165165LTT-6	60 ns	

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Pin Arrangement (HM5164165 Series)

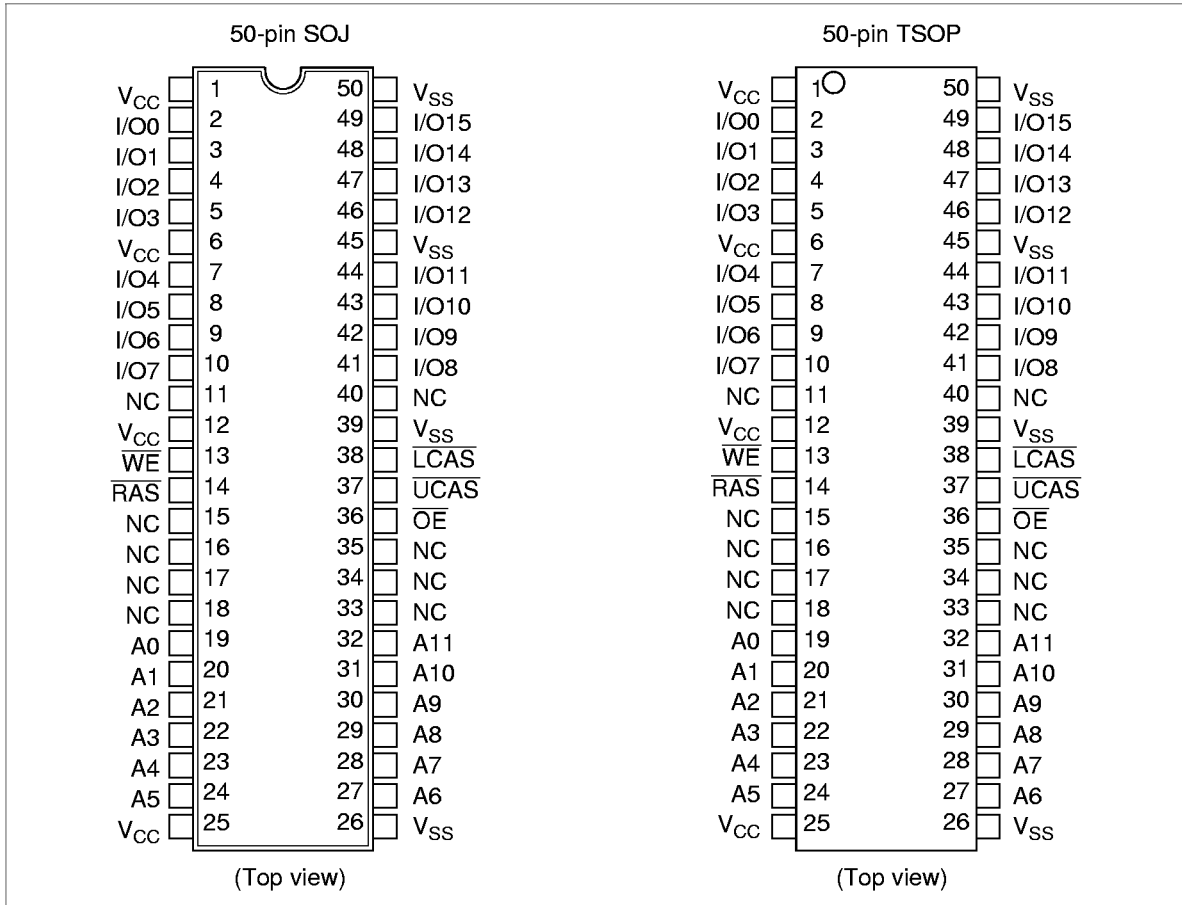


Pin Description

Pin name	Function
A0 to A12	Address input — Row/Refresh address A0 to A12 — Column address A0 to A8
I/O0 to I/O15	Data input/output
RAS	Row address strobe
UCAS, LCAS	Column address strobe
WE	Write enable
OE	Output enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

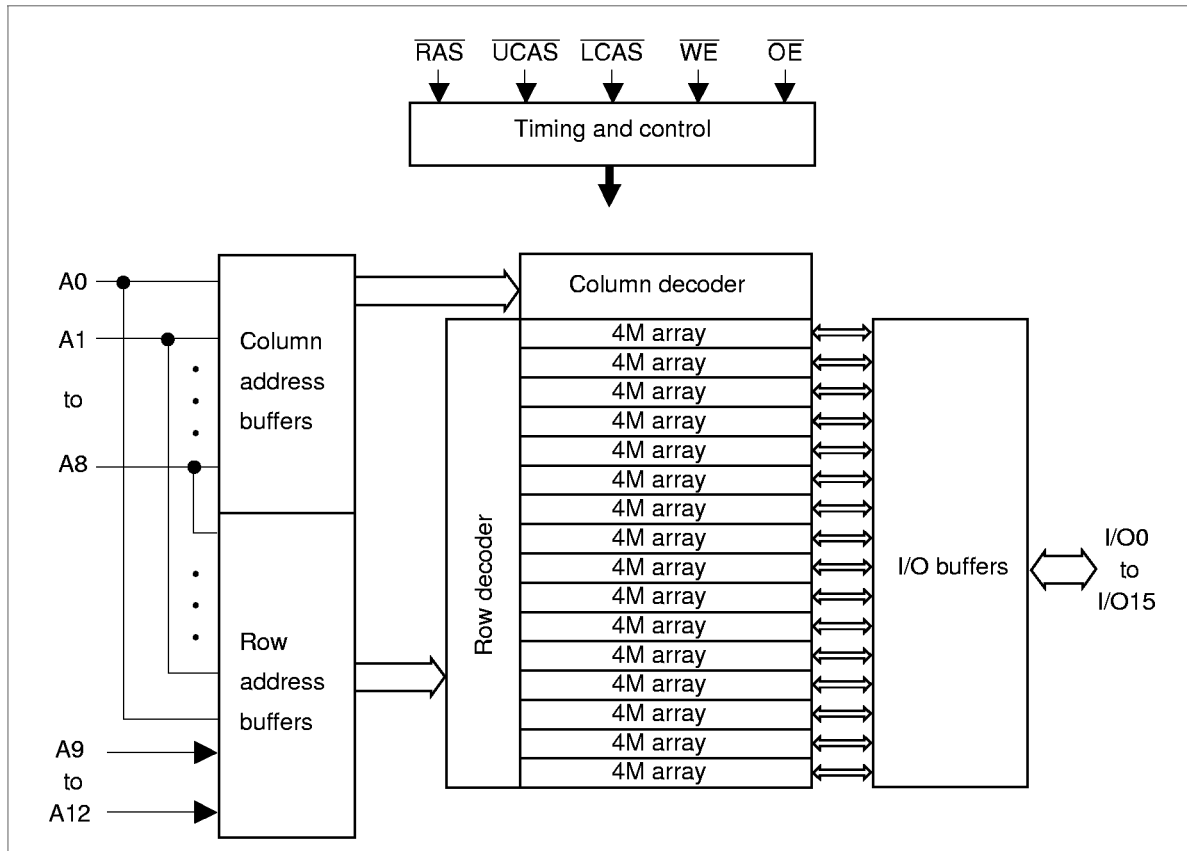
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Pin Arrangement (HM5165165 Series)



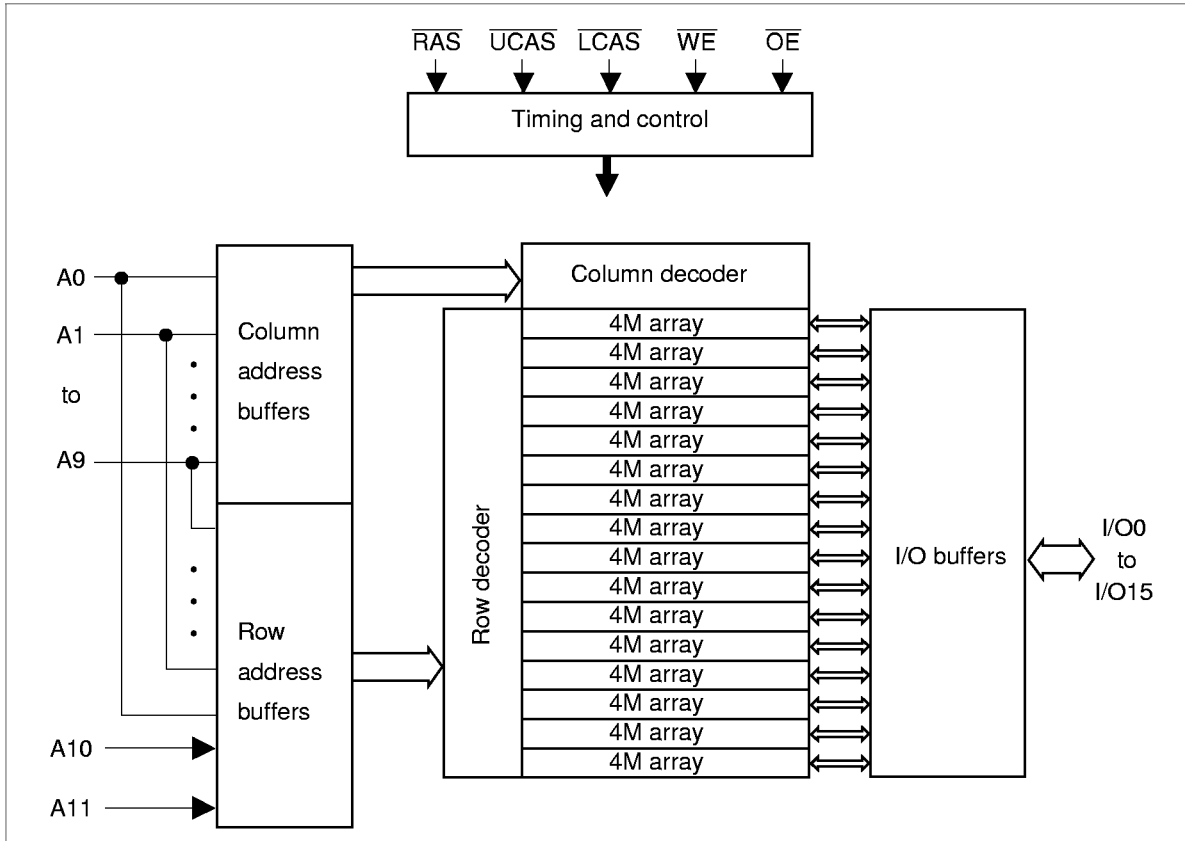
Pin Description

Pin name	Function
A0 to A11	Address input — Row/Refresh address A0 to A11 — Column address A0 to A9
I/O0 to I/O15	Data input/output
RAS	Row address strobe
UCAS, LCAS	Column address strobe
WE	Write enable
OE	Output enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram (HM5164165 Series)

HM5164165 Series, HM5165165 Series

Block Diagram (HM5165165 Series)



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Operation Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O 0 to I/O 7	I/O 8 to I/O 15	Operation
H	×	×	×	×	High-Z	High-Z	Standby
L	L	H	H	L	Dout	High-Z	Read cycle
L	H	L	H	L	High-Z	Dout	
L	L	L	H	L	Dout	Dout	
L	L	H	L ^{*2}	×	Din	×	Early write cycle
L	H	L	L ^{*2}	×	×	Din	
L	L	L	L ^{*2}	×	Din	Din	
L	L	H	L ^{*2}	H	Din	×	Delayed write cycle
L	H	L	L ^{*2}	H	×	Din	
L	L	L	L ^{*2}	H	Din	Din	
L	L	H	H to L	L to H	Dout/Din	High-Z	Read-modify-write cycle
L	H	L	H to L	L to H	High-Z	Dout/Din	
L	L	L	H to L	L to H	Dout/Din	Dout/Din	
L	H	H	×	×	High-Z	High-Z	$\overline{RAS}$ -only refresh cycle
H to L	H	L	H	×	High-Z	High-Z	$\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle or
H to L	L	H	H	×	High-Z	High-Z	Self refresh cycle (L-version)
H to L	L	L	H	×	High-Z	High-Z	
L	L	L	H	H	High-Z	High-Z	Read cycle (Output disabled)

Notes: 1. H: V_{IH} (inactive) L: V_{IL} (active) ×: V_{IH} or V_{IL}

2. $t_{WCS} \geq 0$ ns: Early write cycle

$t_{WCS} < 0$ ns: Delayed write cycle

3. Mode is determined by the OR function of the $\overline{UCAS}$ and $\overline{LCAS}$. (Mode is set by the earliest of $\overline{UCAS}$ and $\overline{LCAS}$ active edge and reset by the latest of $\overline{UCAS}$ and $\overline{LCAS}$ inactive edge.) However write operation and output High-Z control are done independently by each $\overline{UCAS}$, $\overline{LCAS}$.

ex. if $\overline{RAS} = H$ to L , $\overline{LCAS} = L$, $\overline{UCAS} = H$, then $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle is selected.

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5 to $V_{CC} + 0.5$ (≤ 4.6 V (max))	V
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to $+4.6$	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Storage temperature	T_{stg}	-55 to $+125$	$^{\circ}\text{C}$

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
	V_{SS}	0	0	0	V	2
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	-0.3	—	0.8	V	1
Ambient temperature range	T_a	0	—	70	$^{\circ}\text{C}$	

Notes: 1. All voltage referred to V_{SS} .

2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

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DC Characteristics (HM5164165 Series)

HM5164165							
Parameter	Symbol	-5		-6		Unit	Test conditions
		Min	Max	Min	Max		
Operating current*1, *2	I _{CC1}	—	120	—	110	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	mA	TTL interface RAS, UCAS, LCAS = V _{IH} Dout = High-Z
		—	0.5	—	0.5	mA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	μA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current*2	I _{CC3}	—	120	—	110	mA	t _{RC} = min
Standby current*1	I _{CC5}	—	5	—	5	mA	RAS = V _{IH} UCAS, LCAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	120	—	110	mA	t _{RC} = min
EDO page mode current*1, *3	I _{CC7}	—	120	—	110	mA	RAS = V _{IL} , CAS cycle, t _{HPC} = t _{HPC} min
Battery backup current*4 (Standby with CBR refresh) (L-version)	I _{CC10}	—	500	—	500	μA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	400	—	400	μA	CMOS interface RAS, UCAS, LCAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _{LI}	−5	5	−5	5	μA	0 V ≤ Vin ≤ V _{CC} + 0.3 V
Output leakage current	I _{LO}	−5	5	−5	5	μA	0 V ≤ Vout ≤ V _{CC} Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Measured with one sequential address change per EDO cycle, t_{HPC} .

4. $V_{IH} \geq V_{CC} - 0.2 \text{ V}$, $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$.

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DC Characteristics (HM5165165 Series)

HM5165165							
Parameter	Symbol	-5		-6		Unit	Test conditions
		Min	Max	Min	Max		
Operating current*1, *2	I _{CC1}	—	140	—	120	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	mA	TTL interface RAS, UCAS, LCAS = V _{IH} Dout = High-Z
		—	0.5	—	0.5	mA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	μA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current*2	I _{CC3}	—	140	—	120	mA	t _{RC} = min
Standby current*1	I _{CC5}	—	5	—	5	mA	RAS = V _{IH} UCAS, LCAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	140	—	120	mA	t _{RC} = min
EDO page mode current*1, *3	I _{CC7}	—	120	—	110	mA	RAS = V _{IL} , CAS cycle, t _{HPC} = t _{HPC} min
Battery backup current*4 (Standby with CBR refresh) (L-version)	I _{CC10}	—	500	—	500	μA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	400	—	400	μA	CMOS interface RAS, UCAS, LCAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _{LI}	−5	5	−5	5	μA	0 V ≤ Vin ≤ V _{CC} + 0.3 V
Output leakage current	I _{LO}	−5	5	−5	5	μA	0 V ≤ Vout ≤ V _{CC} Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Measured with one sequential address change per EDO cycle, t_{HPC} .

4. $V_{IH} \geq V_{CC} - 0.2 \text{ V}$, $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}} = V_{IH}$ to disable Dout.

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AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$)^{*1, *2, *19, *27}

Test Conditions

- Input rise and fall time: 2 ns
- Input pulse levels: $V_{IL} = 0\text{ V}$, $V_{IH} = 3.0\text{ V}$
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5164165/HM5165165					
		−5		−6			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	84	—	104	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	30	—	40	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	8	—	10	—	ns	31
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10000	60	10000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	8	10000	10	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	ns	
Row address hold time	t _{RAH}	8	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	ns	28
Column address hold time	t _{CAH}	8	—	10	—	ns	28
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	12	37	14	45	ns	3
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	10	25	12	30	ns	4
$\overline{\text{RAS}}$ hold time	t _{RSH}	13	—	15	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	35	—	40	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5	—	5	—	ns	29
$\overline{\text{OE}}$ to Din delay time	t _{OED}	13	—	15	—	ns	5
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	t _{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	2	50	2	50	ns	7

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Read Cycle

		HM5164165/HM5165165					
		−5		−6			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	ns	9, 10, 17
Access time from address	t_{AA}	—	25	—	30	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	13	—	15	ns	9
Read command setup time	t_{RCS}	0	—	0	—	ns	28
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12, 29
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	50	—	60	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	—	30	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	15	—	18	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	21
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	ns	13, 21
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	13	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	13	—	15	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	ns	21
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	13	—	15	ns	13, 21
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	13	—	15	ns	13
$\overline{\text{WE}}$ to Din delay time	t_{WED}	13	—	15	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	13	—	15	—	ns	

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Write Cycle

		HM5164165/HM5165165					
		−5		−6			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t _{WCS}	0	—	0	—	ns	14, 28
Write command hold time	t _{WCH}	8	—	10	—	ns	28
Write command pulse width	t _{WP}	8	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t _{RWL}	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t _{CWL}	8	—	10	—	ns	30
Data-in setup time	t _{DS}	0	—	0	—	ns	15, 30
Data-in hold time	t _{DH}	8	—	10	—	ns	15, 30

Read-Modify-Write Cycle

		HM5164165/HM5165165					
		−5		−6			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	116	—	140	—	ns	
RAS to WE delay time	t _{RWD}	67	—	79	—	ns	14
CAS to WE delay time	t _{CWD}	30	—	34	—	ns	14
Column address to WE delay time	t _{AWD}	42	—	49	—	ns	14
OE hold time from WE	t _{OEH}	13	—	15	—	ns	

Refresh Cycle

		HM5164165/HM5165165					
		−5		−6			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
CAS setup time (CBR refresh cycle)	t _{CSR}	5	—	5	—	ns	28
CAS hold time (CBR refresh cycle)	t _{CHR}	8	—	10	—	ns	29
WE setup time (CBR refresh cycle)	t _{WRP}	0	—	0	—	ns	
WE hold time (CBR refresh cycle)	t _{WRH}	8	—	10	—	ns	
RAS precharge to CAS hold time	t _{RPC}	5	—	5	—	ns	28

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EDO Page Mode Cycle

		HM5164165/HM5165165					
		-5		-6			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t _{HPC}	20	—	25	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t _{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t _{CPA}	—	28	—	35	ns	9, 17, 29
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t _{CPRH}	28	—	35	—	ns	
Output data hold time from $\overline{CAS}$ low	t _{DOH}	3	—	3	—	ns	9, 22
$\overline{CAS}$ hold time referred $\overline{OE}$	t _{COL}	8	—	10	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t _{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t _{RCHC}	28	—	35	—	ns	
Write pulse width during $\overline{CAS}$ precharge	t _{WPE}	8	—	10	—	ns	
$\overline{OE}$ precharge time	t _{OEP}	8	—	10	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HM5164165/HM5165165					
		-5		-6			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	t _{HPRWC}	57	—	68	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t _{CPW}	45	—	54	—	ns	14, 29

Refresh (HM5164165 Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	64	ms	8192 cycles
Refresh period (L-version)	t_{REF}	128	ms	8192 cycles

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Refresh (HM5165165 Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

Self Refresh Mode (L-version)

		HM5164165L/HM5165165L					
		−5		−6			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (self refresh)	t _{RASS}	100	—	100	—	μs	26
$\overline{RAS}$ precharge time (self refresh)	t _{RPS}	90	—	110	—	ns	26
$\overline{CAS}$ hold time (self refresh)	t _{CHS}	−50	—	−50	—	ns	30

Notes: 1. AC measurements assume $t_T = 2$ ns.

2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ -only refresh or $\overline{CAS}$ -before- $\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then the access time is controlled exclusively by t_{CAC} .
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max), t_{OEZ} (max), t_{WEZ} (max) and t_{OFR} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS} and t_{DH} are referred to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

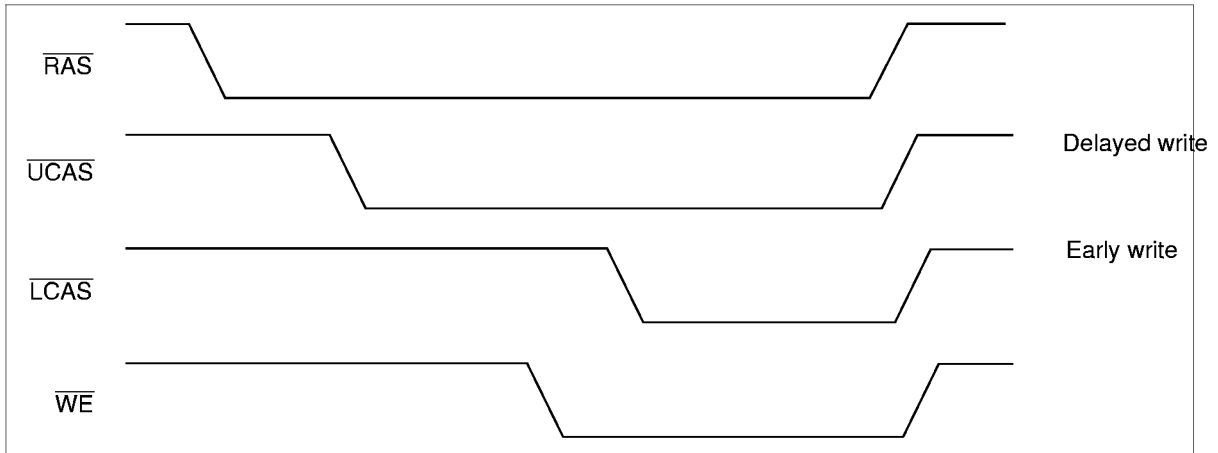
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH\ min}/V_{IL\ max}$ level.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2 t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .
22. t_{DOH} defines the time at which the output level go cross. $V_{OL} = 0.8\ V$, $V_{OH} = 2.0\ V$ of output timing reference level.
23. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64 ms period on the condition a and b below.
 - a. Enter self refresh mode within 15.6 μs after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
 - b. Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6 μs after exiting from self refresh mode.
24. In case of entering from $\overline{RAS}$ -only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 23.
25. For L-version, it is available to apply each 128 ms and 31.2 μs instead of 64 ms and 15.6 μs at note 23.
26. At $t_{RASS} > 100\ \mu s$, self refresh mode is activated, and not activated at $t_{RASS} < 10\ \mu s$. It is undefined within the range of $10\ \mu s \leq t_{RASS} \leq 100\ \mu s$. For $t_{RASS} \geq 10\ \mu s$, it is necessary to satisfy t_{RPS} .
27. When both $\overline{UCAS}$ and $\overline{LCAS}$ go low at the same time, all 16-bit data are written into the device. $\overline{UCAS}$ and $\overline{LCAS}$ cannot be staggered within the same write/read cycles.
28. t_{ASC} , t_{CAH} , t_{RCS} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
29. t_{CRP} , t_{CHR} , t_{RCH} , t_{CPA} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
30. t_{CWL} , t_{DH} , t_{DS} and t_{CHS} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
31. t_{CP} is determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
32. XXX: H or L (H: $V_{IH\ (min)} \leq V_{IN} \leq V_{IH\ (max)}$, L: $V_{IL\ (min)} \leq V_{IN} \leq V_{IL\ (max)}$)
 //: Invalid Dout
 When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

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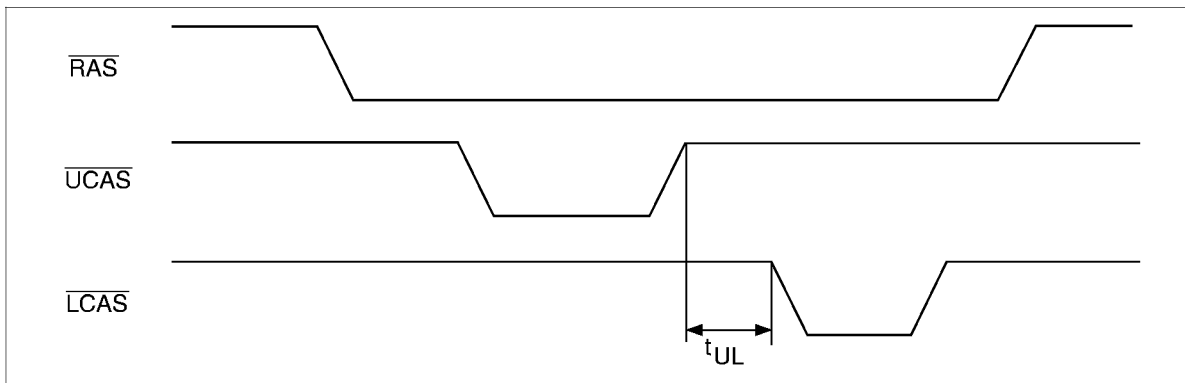
Notes concerning $2\overline{\text{CAS}}$ control

Please do not separate the $\overline{\text{UCAS}}/\overline{\text{LCAS}}$ operation timing intentionally. However skew between $\overline{\text{UCAS}}/\overline{\text{LCAS}}$ are allowed under the following conditions.

1. Each of the $\overline{\text{UCAS}}/\overline{\text{LCAS}}$ should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.



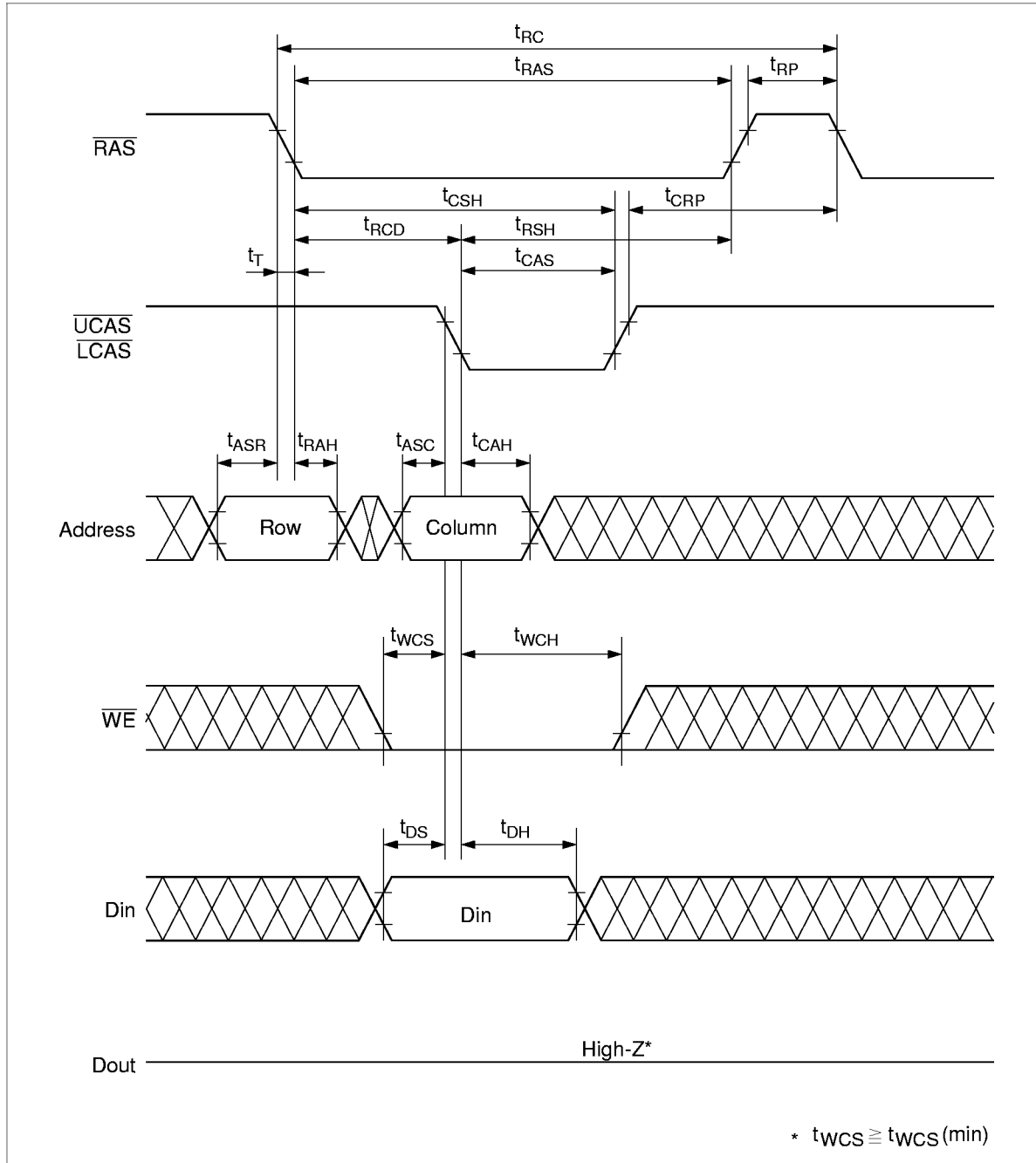
3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{\text{CP}} \leq t_{\text{UL}}$) is satisfied, EDO page mode can be performed.



4. Byte control operation by remaining $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ high is guaranteed.

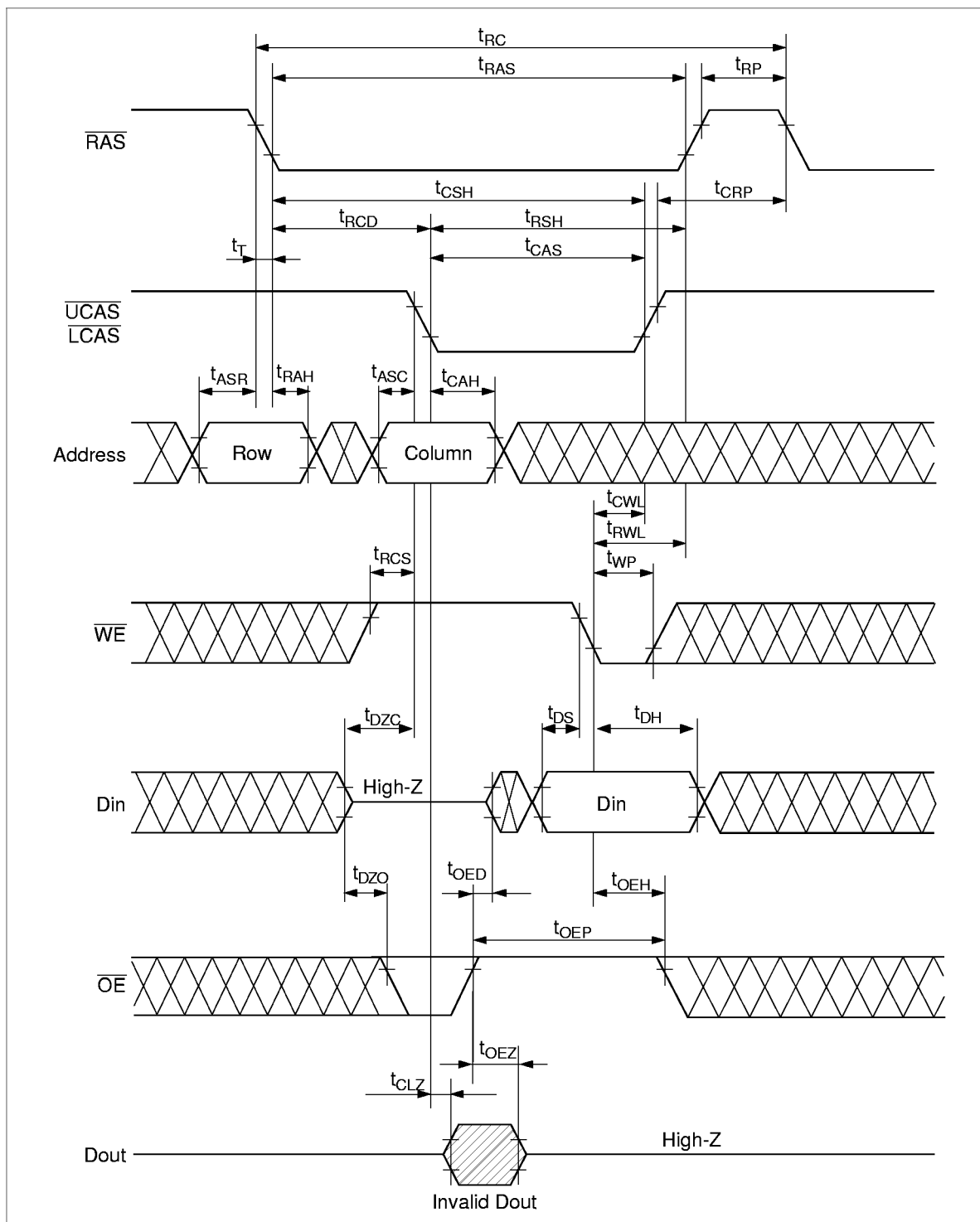
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Early Write Cycle



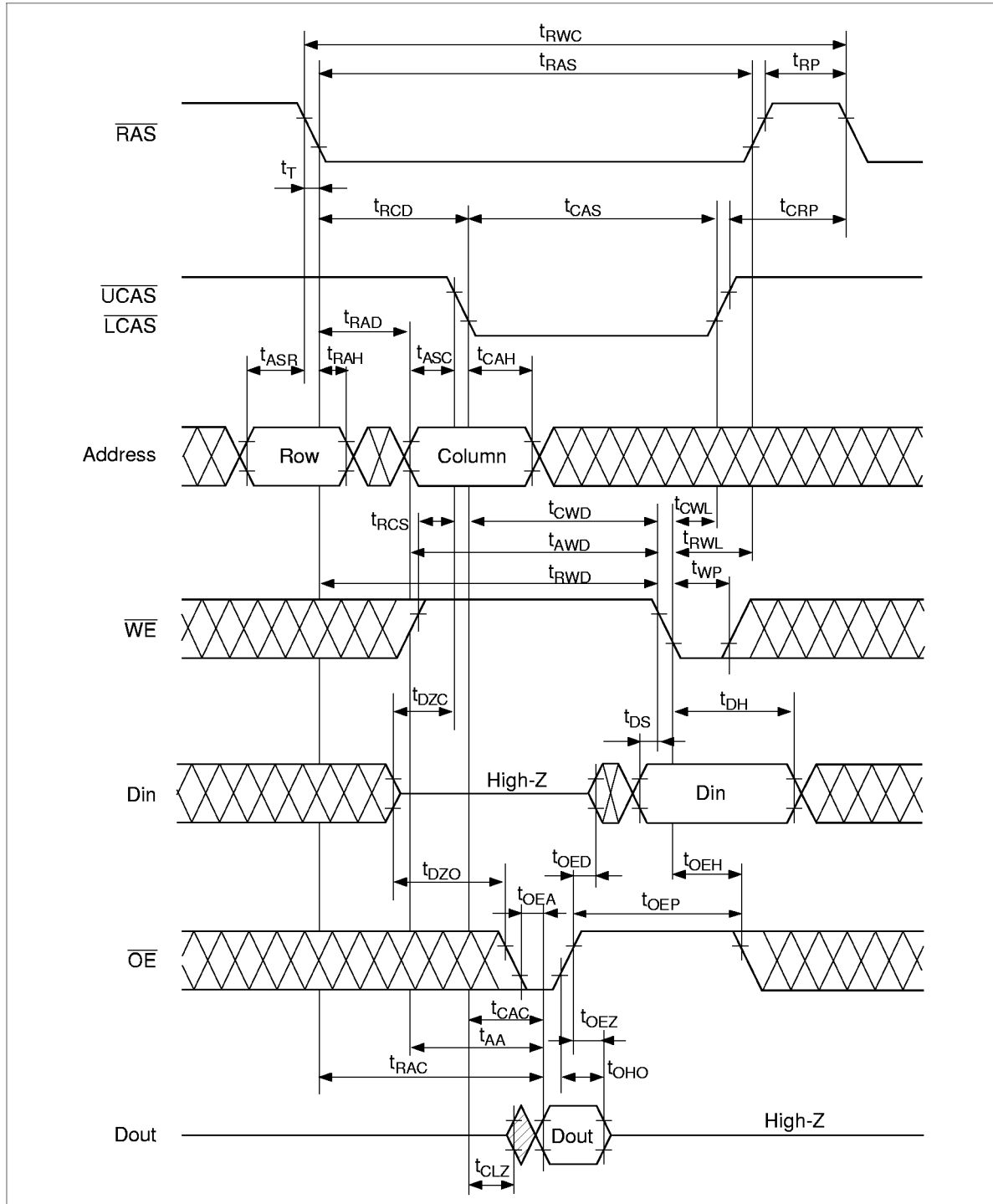
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Delayed Write Cycle*18



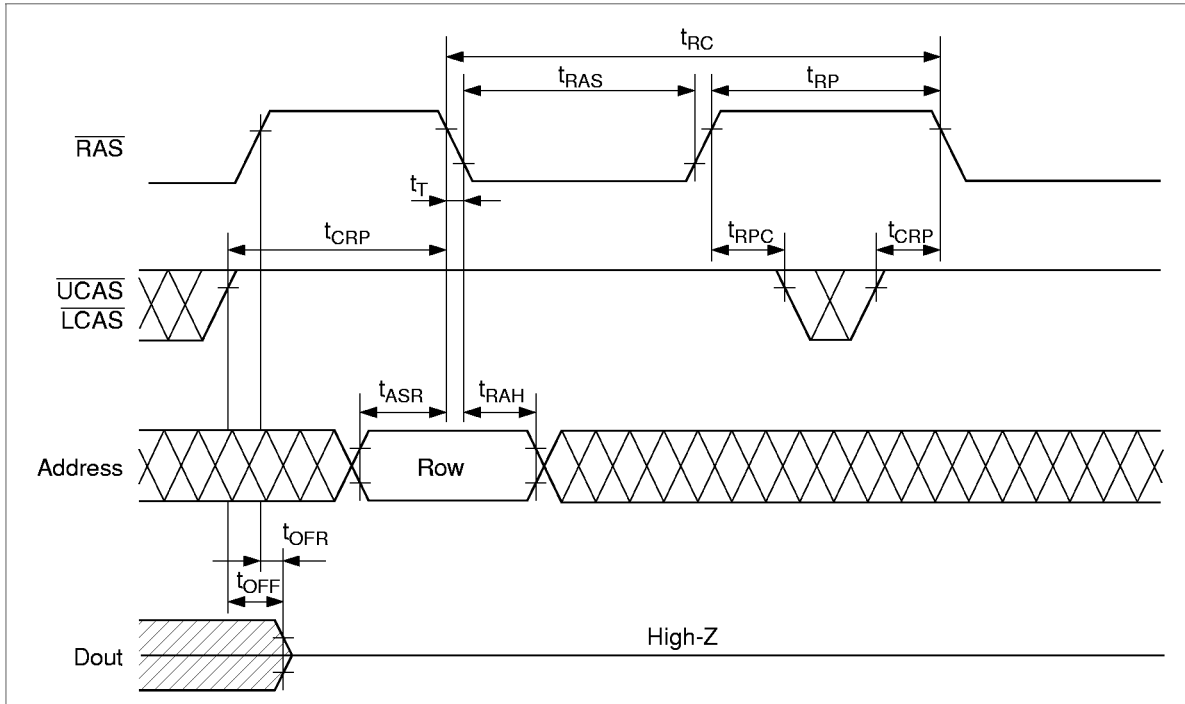
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Read-Modify-Write Cycle*18



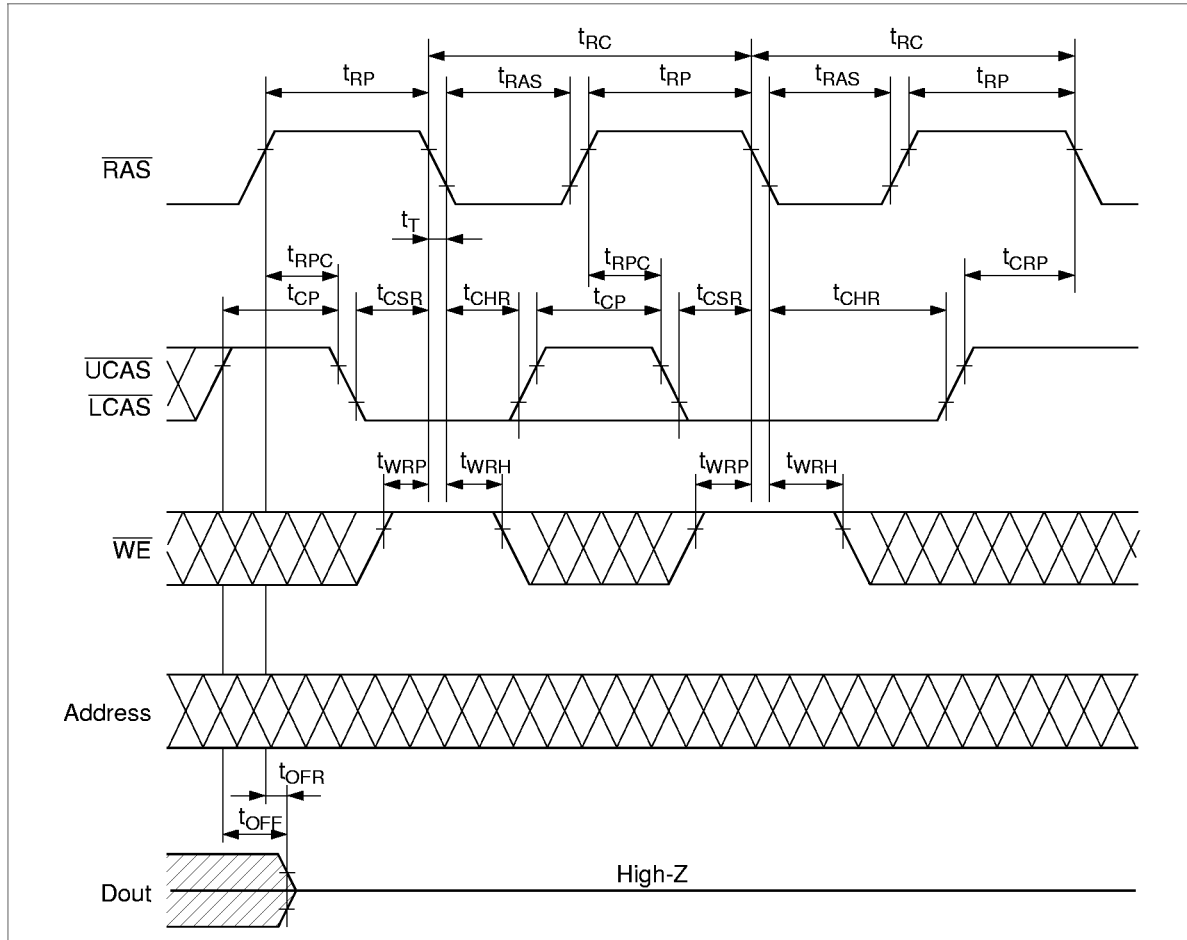
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$\overline{\text{RAS}}$ -Only Refresh Cycle

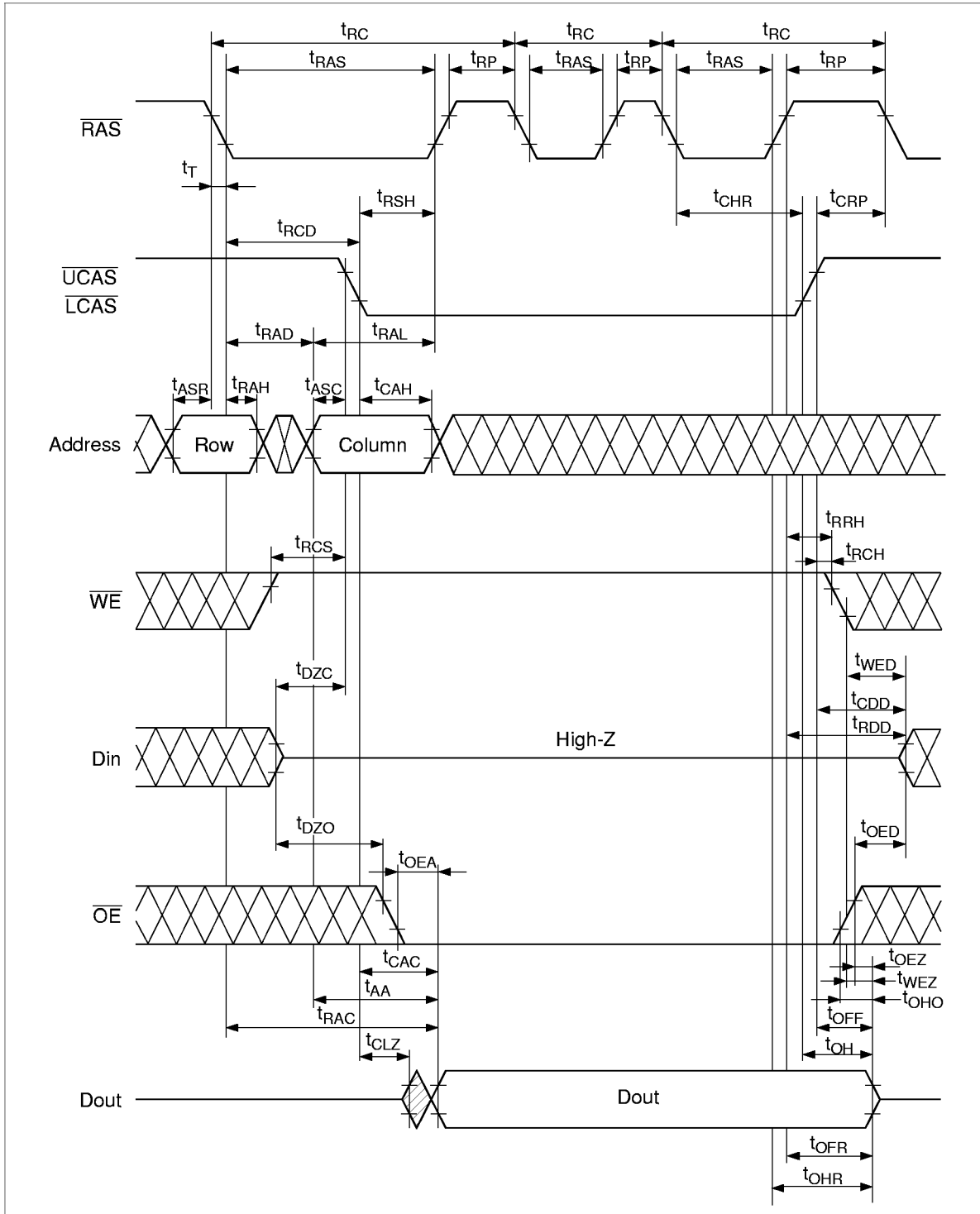


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$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

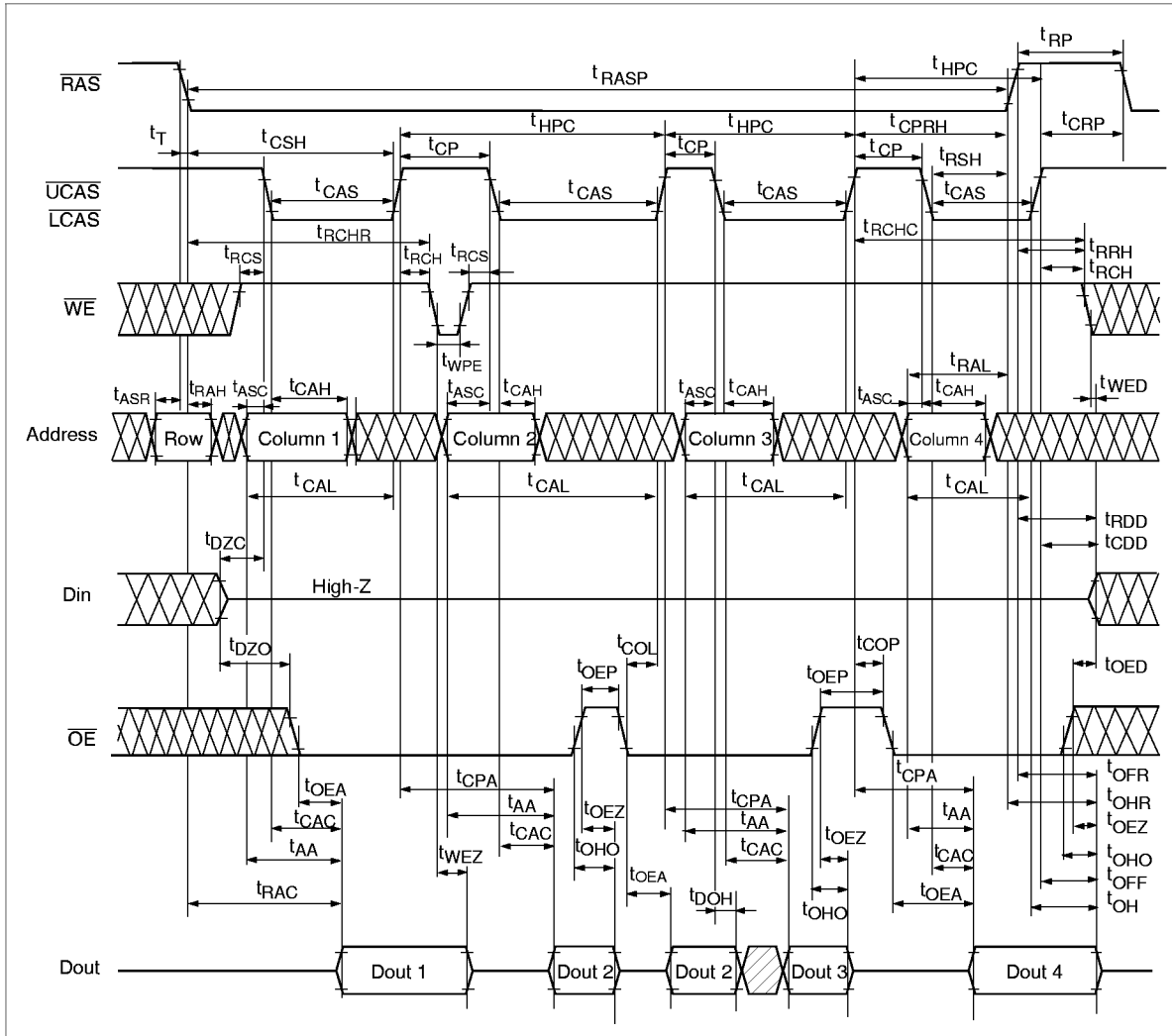


Hidden Refresh Cycle

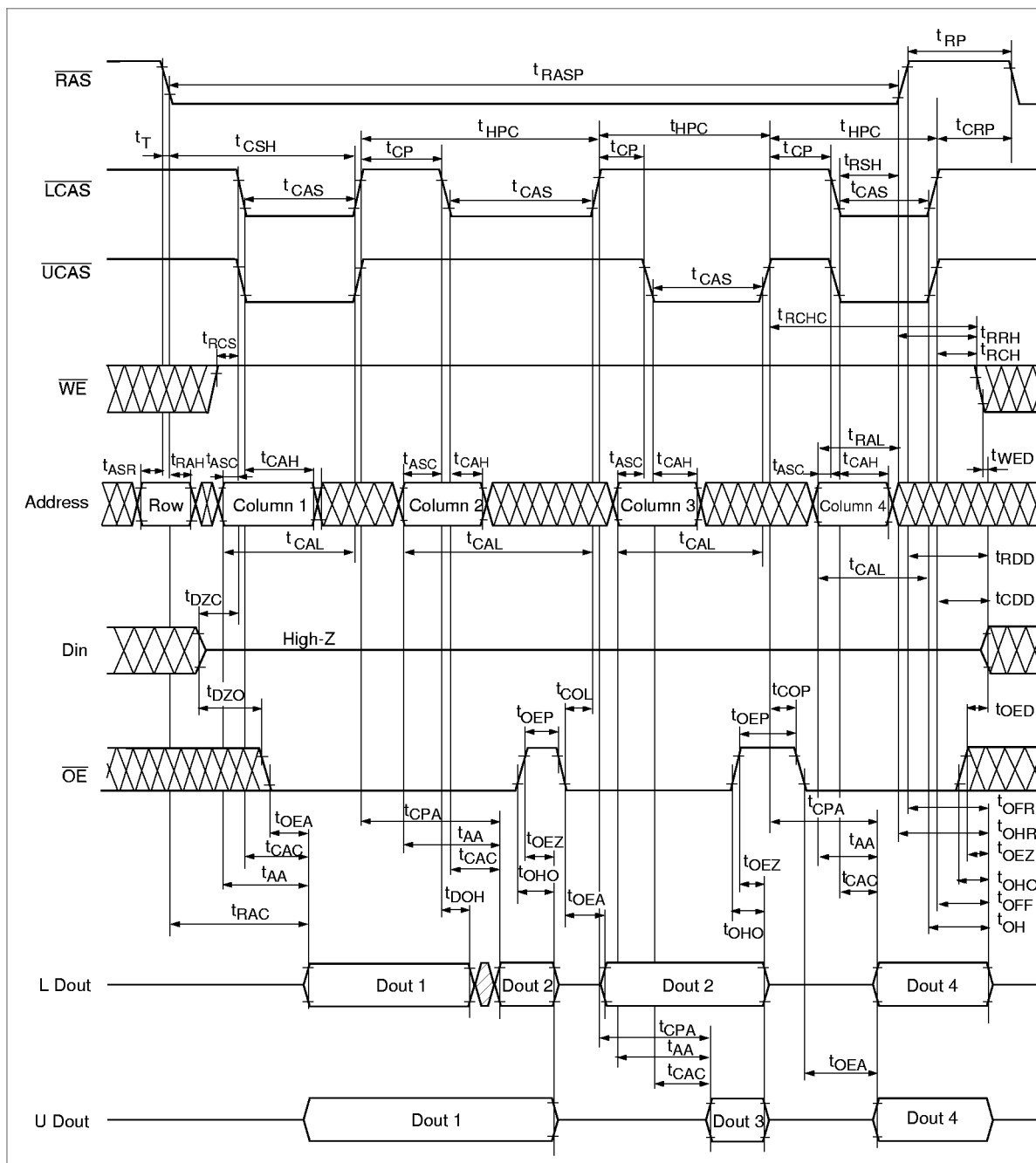


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EDO Page Mode Read Cycle

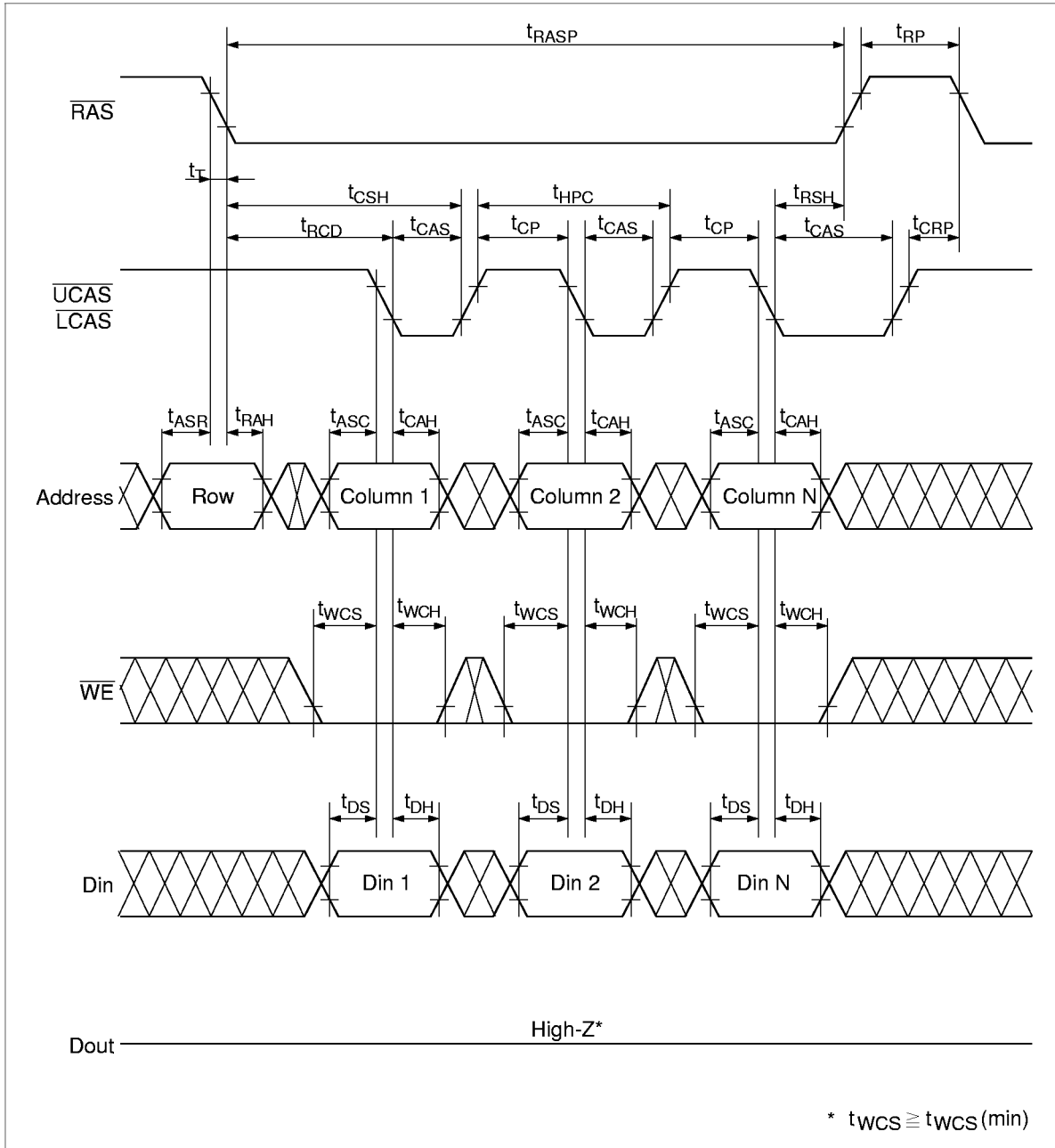


EDO Page Mode Read Cycle ($\overline{2\text{CAS}}$ control)



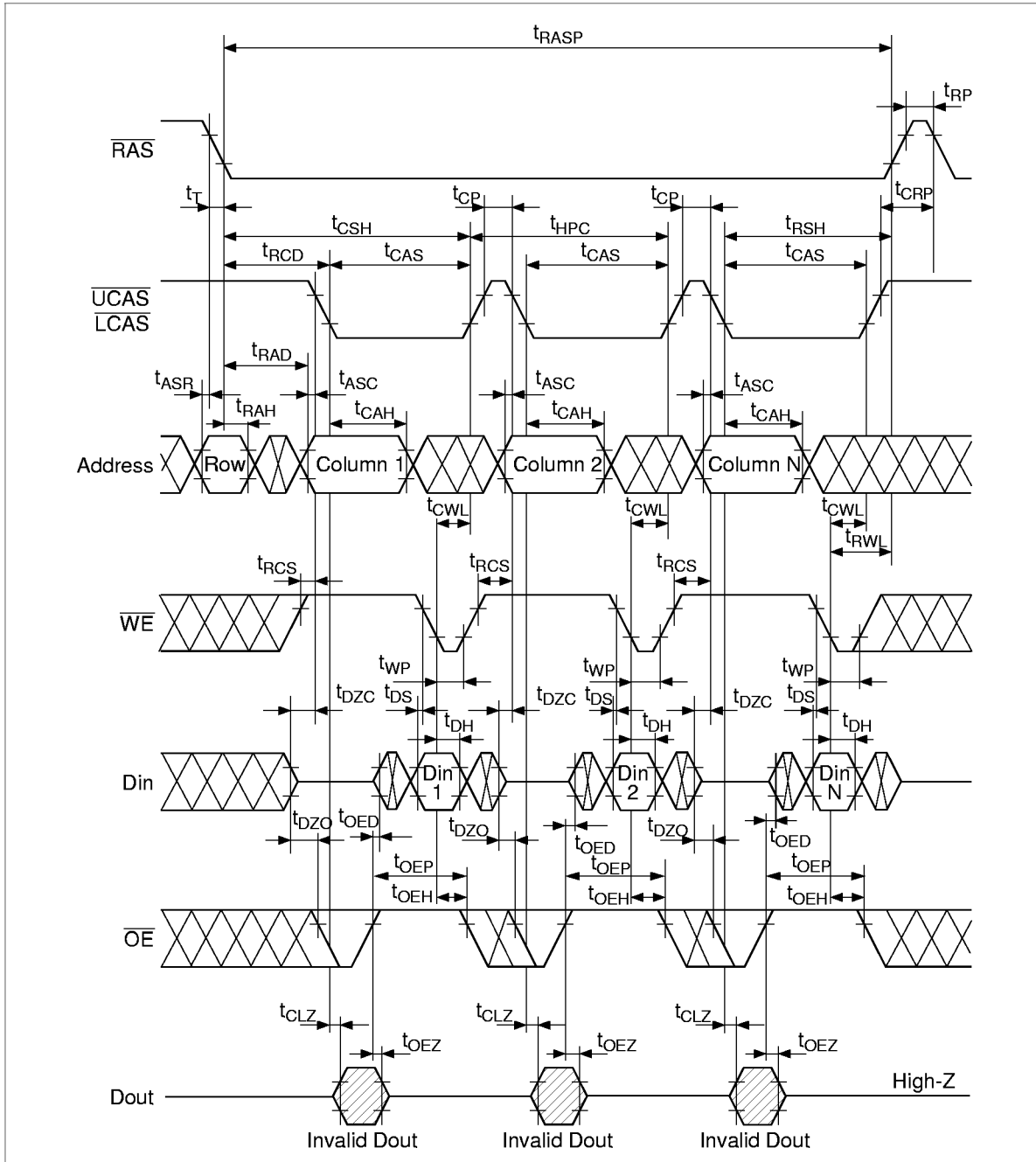
HM5164165 Series, HM5165165 Series

EDO Page Mode Early Write Cycle



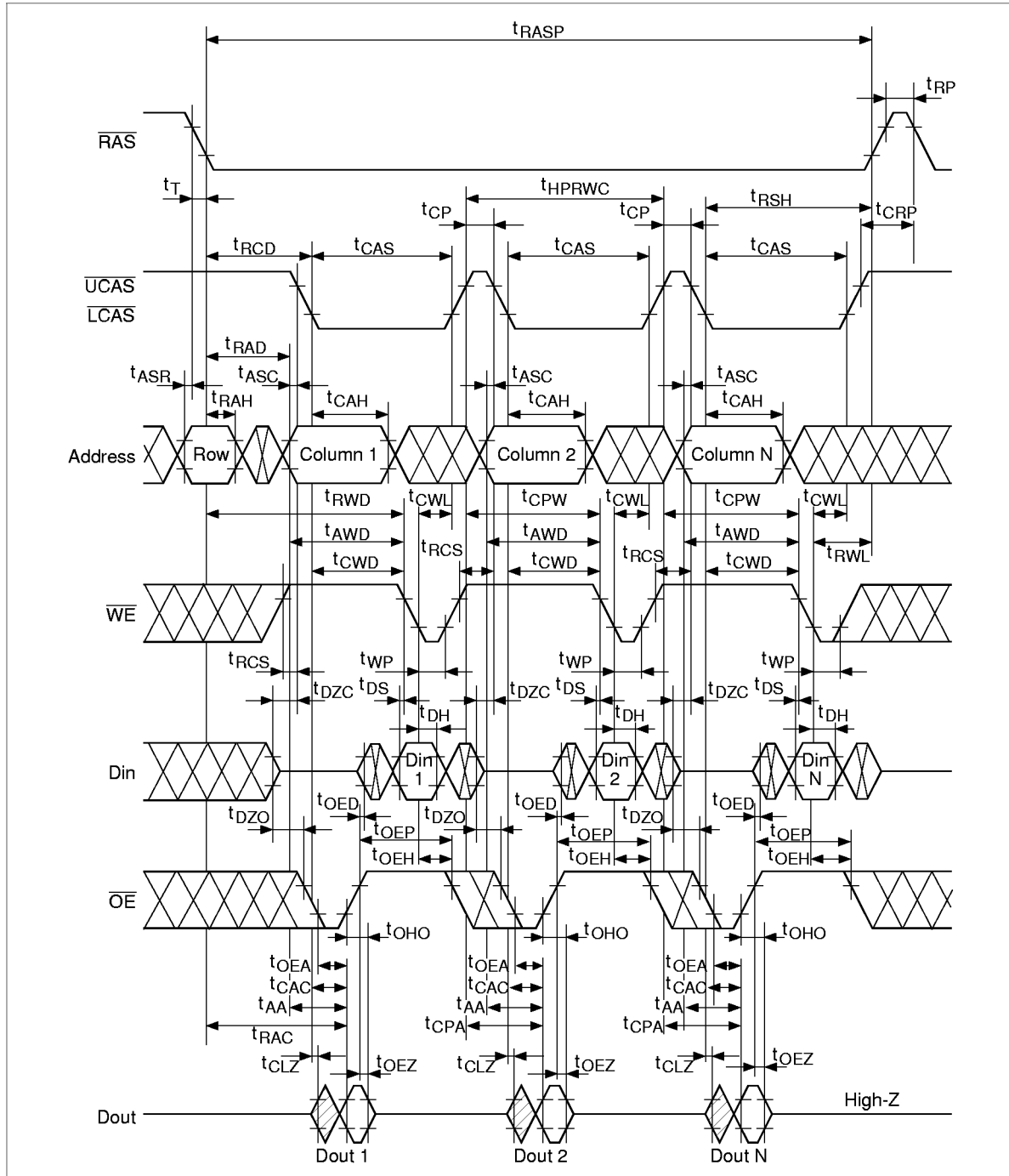
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EDO Page Mode Delayed Write Cycle*18

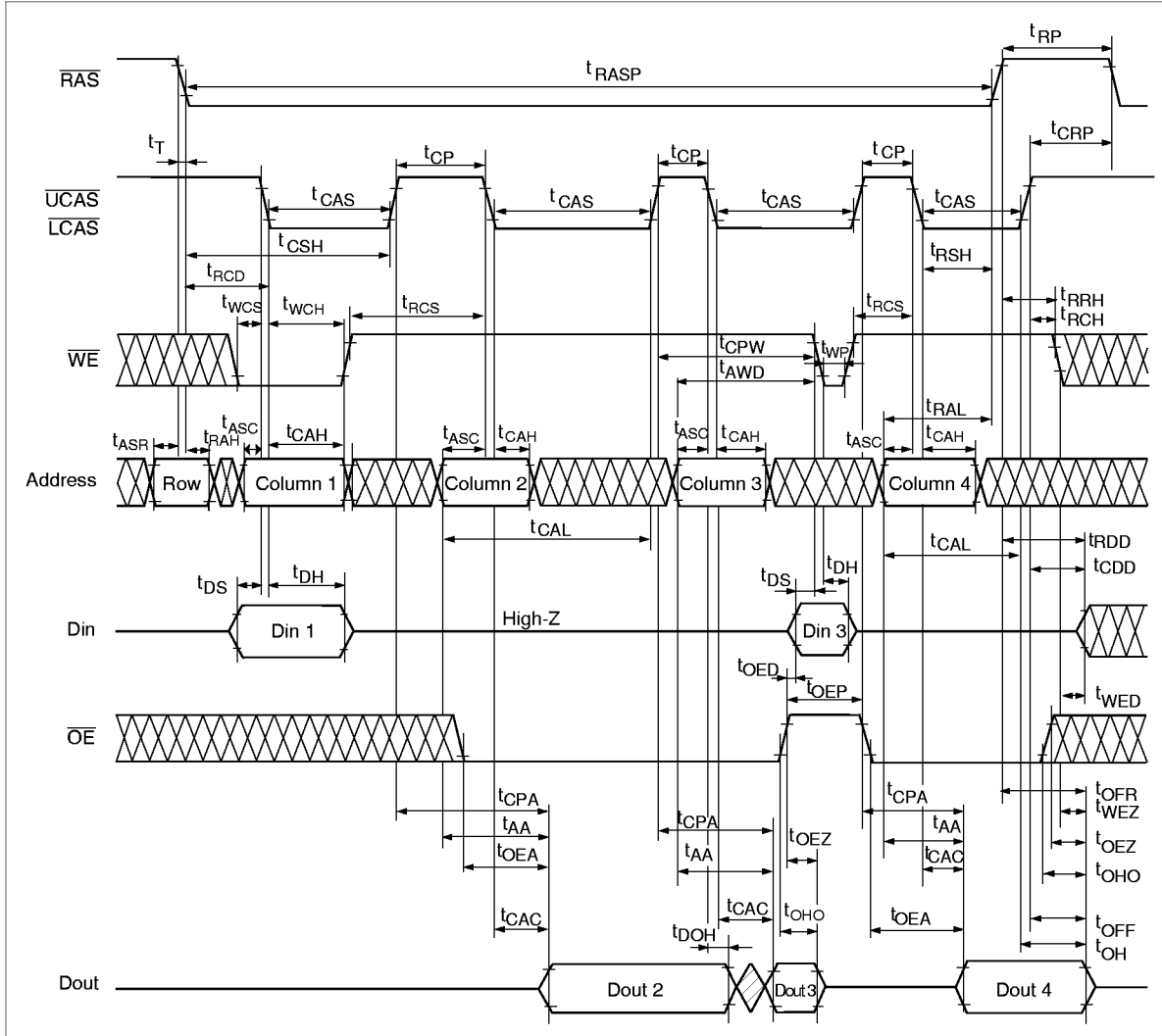


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EDO Page Mode Read-Modify-Write Cycle*18

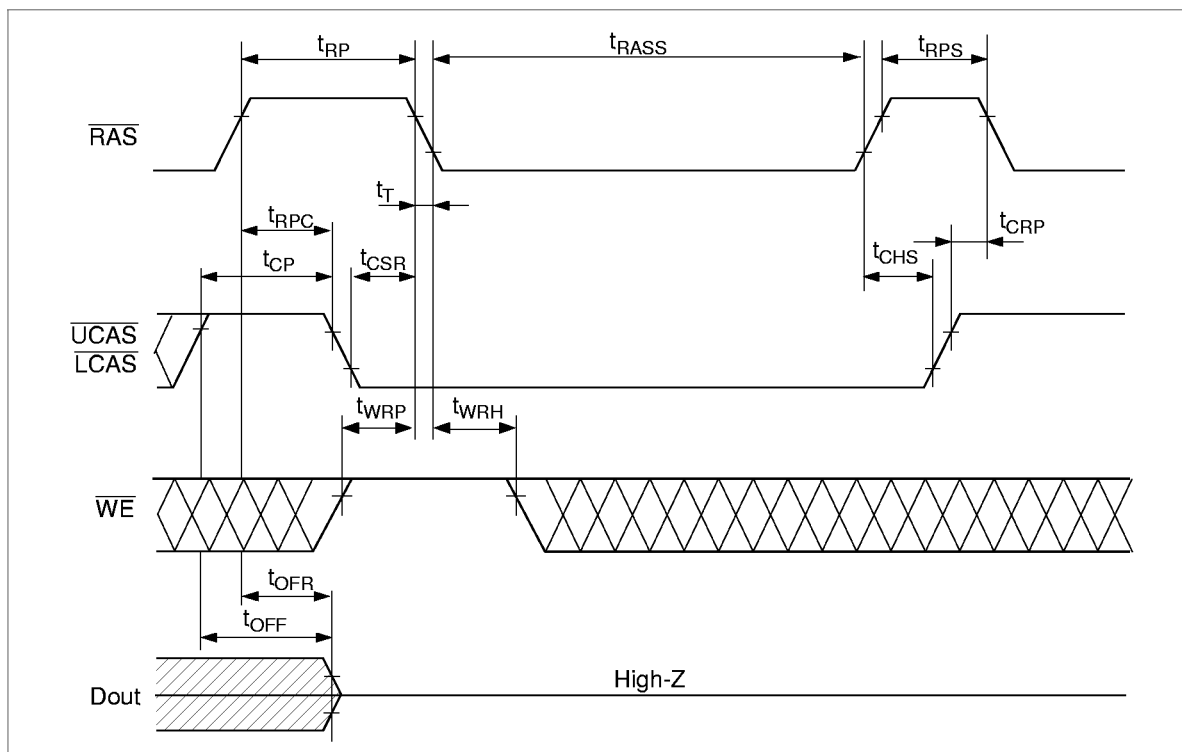


EDO Page Mode Mix Cycle (1) *20



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Self Refresh Cycle (L-version)*23, 24, 25, 26

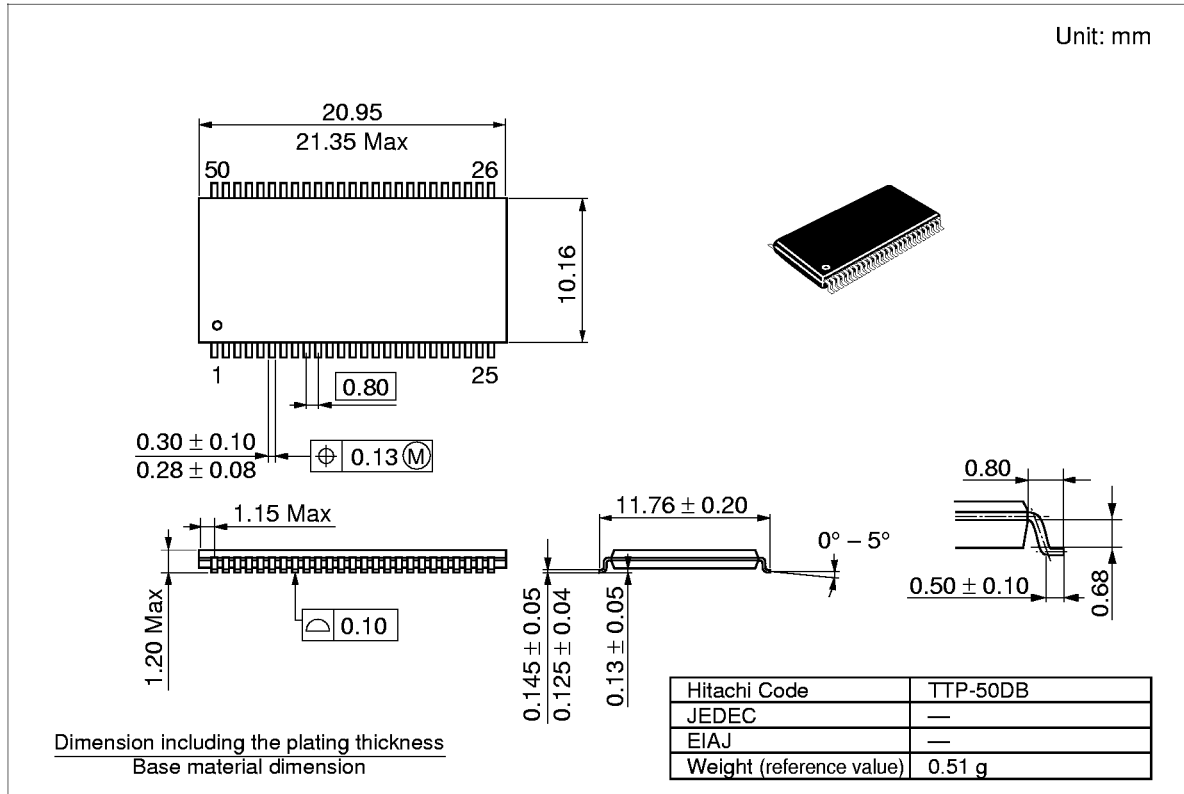


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HM5164165TT/LTT Series

HM5165165TT/LTT Series (TTP-50DB)

Unit: mm



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jul. 23, 1997	Initial issue	J. Miyake	M. Saeki
0.1	Oct. 24, 1997	AC Characteristics Change order of notes Change note numbers of tables Correct errors EDO page mode read cycle	J. Miyake	Y. Takahashi
1.0	Mar. 18, 1998	Deletion of Preliminary		