National Semiconductor

54ABT/74ABT273
Octal D-Type Flip-Flop

General Description

The 'ABT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'ABT377 for clock enable version
- See 'ABT373 for transparent latch version
- See 'ABT374 for TRI-STATE® version
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention
- Standard Military Drawing (SMD) 5962-9321701

Ordering Code: See Section 10

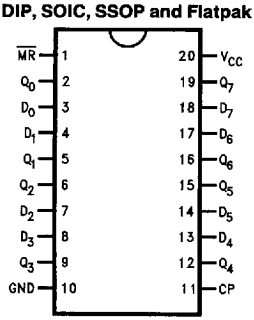
Commercial	Military	Package Number	Package Description
74ABT273CSC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74ABT273CSJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54ABT273J/883	J20A	20-Lead Ceramic Dual-In-Line
74ABT273CMSA (Note 1)		MSA20	20-Lead Molded Shrink Small Outline, EIAJ Type II
	54ABT273W/883	W20A	20-Lead Cerpack
	54ABT273E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74ABT273CMTC (Notes 1, 2)		MTC20	20-Lead Molded Thin Shrink Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX, SJX, MSAX, and MTCX.

Note 2: Contact factory for package availability.

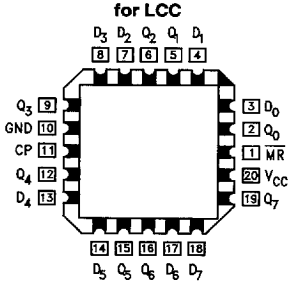
Connection Diagrams

Pin Assignment for DIP, SOIC, SSOP and Flatpak



TL/F/11549–1

Pin Assignment for LCC



TL/F/11549–2

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
Q_0–Q_7	Data Outputs

5

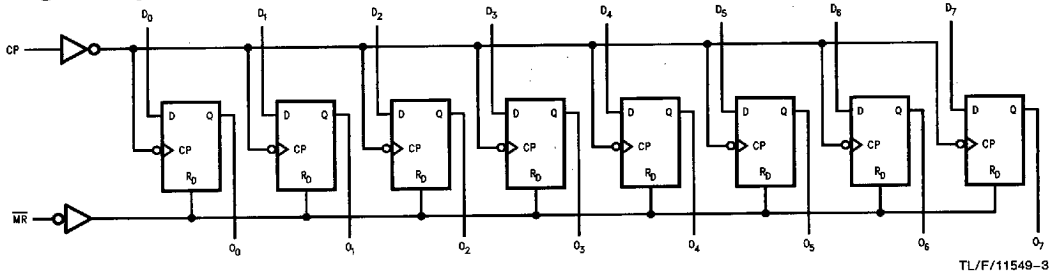
Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load "1"	H	⎍	h	H
Load "0"	H	⎍	l	L

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial
⎍ = LOW-to-HIGH clock transition

Logic Diagram



TL/F/11549–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +4.75V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current (Across Comm Operating Range)	−500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT273 Min	ABT273 Typ	ABT273 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0					I_{OH} = −24 mA
		74ABT	2.0					I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 2)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 2)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCT}	Maximum I_{CC}/Input	Outputs Enabled			1.5	mA	Max	V_I = V_{CC} − 2.1V Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load			0.3	mA/MHz	Max	Outputs Open (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.5 mA/MHz.

Note 2: Guaranteed but not tested.

AC Electrical Characteristics: See Section 2 (SOIC package, contact factory for DIP or SSOP)

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	150	200		150		150		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	2.0 2.8		6.0 6.8	1.0 1.0	7.0 7.5	2.0 2.8	6.0 6.8	ns	2-3, 5
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n	2.5		7.4	1.0	8.2	2.5	7.4	ns	2-3, 5

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.0 2.5		2.0 2.5		2.0 2.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	1.2 1.2		1.4 1.4		1.2 1.2		ns	2-6
$t_w(H)$ $t_w(L)$	Pulse Width, CP, HIGH or LOW	3.3 3.3		3.3 3.3		3.3 3.3		ns	2-3
$t_w(L)$	Master Reset Pulse Width, LOW	3.3		3.3		3.3		ns	2-3
t_{REC}	Recovery Time $\overline{MR}$ to CP	2.0		2.0		2.0		ns	2-6

Capacitance (SOIC package, contact factory for DIP or SSOP)

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$
C_{OUT} (Note 1)	Output Capacitance	9	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-833B, Method 3012.