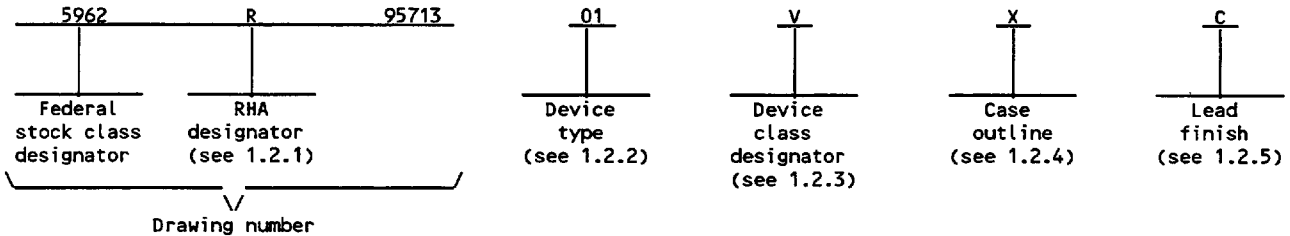




## 1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	82C54RH	Radiation hardened CMOS programmable interval timer

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
J	CDIP2-T24	24	Dual-in-line package
X	CDFP4-F24	24	Ceramic flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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### 1.3 Absolute maximum ratings. 1/

Supply voltage ( $V_{DD}$ )	- - - - -	+7.0 V dc
Input or output voltage range	- - - - -	$V_{SS}$ -0.3 V dc to $V_{DD}$ +0.3 V dc
Storage temperature range ( $T_{STG}$ )	- - - - -	-65°C to +150°C
Junction temperature ( $T_J$ )	- - - - -	+175°C
Thermal resistance Junction-to-case ( $\theta_{JC}$ )	- - - - -	
Case J	- - - - -	+6°C/W
Case X	- - - - -	+4°C/W
Thermal resistance Junction-to-ambient ( $\theta_{JA}$ )	- - - - -	
Case J	- - - - -	+40°C/W
Case X	- - - - -	+60°C/W
Maximum package power dissipation at $T_A = +125^\circ\text{C}$ ( $P_D$ ) 2/	- - - - -	
Case J	- - - - -	+1.25 W
Case X	- - - - -	+0.83 W
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C

### 1.4 Recommended operating conditions.

Operating supply voltage range ( $V_{DD}$ )	- - - - -	4.5 V dc to +5.5 V dc
Operating temperature range ( $T_A$ )	- - - - -	-55°C to +125°C
Input low voltage range ( $V_{IL}$ )	- - - - -	0 V dc to +0.8 V dc
Input high voltage range ( $V_{IH}$ )	- - - - -	$V_{DD}$ -1.5 V dc to $V_{DD}$
Radiation features	- - - - -	
Total dose	- - - - -	> 100K Rads(SI)
Transient upset	- - - - -	> $10^8$ RAD(SI)/sec 3/
Single event upsets (SEU)	- - - - -	22 MEV/(mg/cm <sup>2</sup> ) 3/
Single event latchup (SEL)	- - - - -	60 MEV/(mg/cm <sup>2</sup> ) 3/

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

### SPECIFICATION

#### MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

### STANDARDS

#### MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
MIL-STD-973 - Configuration Management.  
MIL-STD-1835 - Microcircuit Case Outlines.

### BULLETIN

#### MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

### HANDBOOK

#### MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.  
2/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on  $\theta_{JA}$ ) at a rate of 25.0 mW/°C for case J and 16.7 mW/°C for case X.  
3/ Guaranteed by design or process but not tested.

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(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing waveform and test circuit. The timing waveform and test circuit shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TTL output high current	I <sub>OH1</sub>	V <sub>DD</sub> = 4.5 V, V <sub>O</sub> = 3.0 V V <sub>IN</sub> = 0 V or 4.5 V	1,2,3	All	-2.5		mA
CMOS output high current	I <sub>OH2</sub>	V <sub>DD</sub> = 4.5 V, V <sub>O</sub> = 4.1 V V <sub>IN</sub> = 0 V or 4.5 V	1,2,3	All	-100		μA
Output low current	I <sub>OL</sub>	V <sub>DD</sub> = 4.5 V, V <sub>O</sub> = 0.4 V V <sub>IN</sub> = 0 V or 4.5 V	1,2,3	All	2.5		mA
Input leakage current	I <sub>IH</sub> or I <sub>IL</sub>	V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 0 V or 5.5 V Pins: 9, 11, 14-16, 18-23	1,2,3	All	-1.0	1.0	μA
Output leakage current	I <sub>OZL</sub> I <sub>OZH</sub>	V <sub>DD</sub> = 5.25 V, V <sub>IN</sub> = 0 V or 5.5 V Pins: 1-8	1,2,3	All	-10	10	μA
Standby power supply current	I <sub>DDSB</sub>	V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = GND or V <sub>DD</sub> I <sub>O</sub> = 0 mA Counters programmed	1,2,3	All		20.0	μA
Operating power supply current	I <sub>DDOP</sub>	V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = GND or V <sub>DD</sub> I <sub>O</sub> = 0 mA CLK0 = CLK1 = CLK2 = 5MHz	1,2,3	All		12.0	mA
Input capacitance	C <sub>IN</sub>	See 4.4.1c V <sub>DD</sub> = open, f = 1 Mhz Measurement referenced to GND	4	All		15	pF
Output capacitance	C <sub>OUT</sub>	See 4.4.1c V <sub>DD</sub> = open, f = 1 Mhz Measurement referenced to GND	4	All		15	pF
I/O capacitance	C <sub>I/O</sub>	See 4.4.1c V <sub>DD</sub> = open, f = 1 Mhz Measurement referenced to GND	4	All		20	pF
Functional tests		See 4.4.1b V <sub>DD</sub> = 4.5 V and 5.5 V V <sub>IN</sub> = GND or V <sub>DD</sub> , f = 1 MHz	7,8	All			
Noise immunity functional tests		See 4.4.1b V <sub>DD</sub> = 5.5 V V <sub>IN</sub> = GND or V <sub>DD</sub> = 1.5 and V <sub>DD</sub> = 4.5 V V <sub>IN</sub> = 0.8 V or V <sub>DD</sub>	7,8	All			

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address stable before RD	$t_{AVRL}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	75		ns
$\overline{\text{CS}}$ stable before $\overline{\text{RD}}$	$t_{SLRL}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	0		ns
Address hold time after RD	$t_{RHAX}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	0		ns
$\overline{\text{RD}}$ pulse width	$t_{RLRH}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	240		ns
Data delay from $\overline{\text{RD}}$	$t_{RLDV}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All		200	ns
Command recovery time	$t_{RHRL}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	320		ns

## WRITE CYCLE

Address stable before WR	$t_{AVWL}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	0		ns
$\overline{\text{CS}}$ stable before $\overline{\text{WR}}$	$t_{SLWL}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	0		ns
Address hold time after WR	$t_{WHAX}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	0		ns
$\overline{\text{WR}}$ pulse width	$t_{WLWH}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	240		ns
Data setup time before WR	$t_{DVWH}$	$V_{DD} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	225		ns

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data hold time after WR	t <sub>WHDX</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All	35		ns
Command recovery time	t <sub>WHWL</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All	320		ns

**CLOCK AND GATE**

Clock period	t <sub>CLCL</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All	200		ns
High pulse width	t <sub>CHCL</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All	100		ns
Low pulse width	t <sub>CLCH</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All	100		ns
Gate width high	t <sub>GHGL</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All	80		ns
Gate width low	t <sub>GLGH</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All	80		ns
Gate setup time to CLK	t <sub>GVCH</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All	80		ns
Gate hold time after CLK	t <sub>CHGX</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All	80		ns
Output delay from CLK	t <sub>CLOV</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All		240	ns
Output delay from gate	t <sub>GLOV</sub>	V <sub>DD</sub> = 4.5 V and 5.5 V	9,10,11	All		200	ns

See footnote at end of tables.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data delay from address read	$t_{\text{AVAV}}$	$V_{\text{DD}} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All		275	ns
Output delay from WR high	$t_{\text{WNOV}}$	$V_{\text{DD}} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All		260	ns

## TIMING REQUIREMENTS

$\overline{\text{RD}}$ to data float 2/	$t_{\text{RHDZ}}$	$V_{\text{DD}} = 4.5 \text{ V and } 5.5 \text{ V}$	9,10,11	All	8	145	ns
---	-------------------	--	---------	-----	---	-----	----

## TIMING RESPONSES

Clock rise time 2/	$t_{\text{CH1CH2}}$	$V_{\text{DD}} = 4.5 \text{ V and } 5.5 \text{ V},$ 1.0 V to 3.5 V	9,10,11	All		25	ns
Clock fall time 2/	$t_{\text{CL1CL2}}$	$V_{\text{DD}} = 4.5 \text{ V and } 5.5 \text{ V},$ 3.5 V to 1.0 V	9,10,11	All		25	ns

1/ Devices supplied to this drawing will meet all levels M, D, L, R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level,  $T_A = +25^{\circ}\text{C}$ .

2/ These parameters are controlled via design or process and are not directly tested. These parameters are characterized upon initial desing and upon changes which may affect parameters.

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Device type		01	
Case outline		J, X	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D7	13	OUT 1
2	D6	14	GATE 1
3	D5	15	CLK 1
4	D4	16	GATE 2
5	D3	17	OUT 2
6	D2	18	CLK 2
7	D1	19	A0
8	D0	20	A1
9	CLK 0	21	$\overline{\text{CS}}$
10	OUT 0	22	$\overline{\text{RD}}$
11	GATE 0	23	$\overline{\text{WR}}$
12	GND	24	V <sub>DD</sub>

FIGURE 1. Terminal connections.

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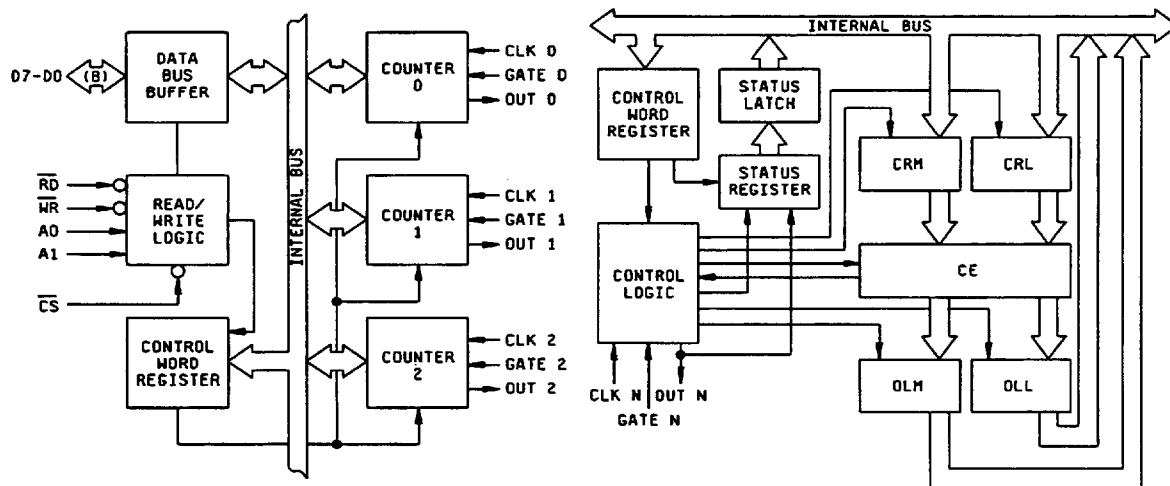


FIGURE 2. Block diagram.

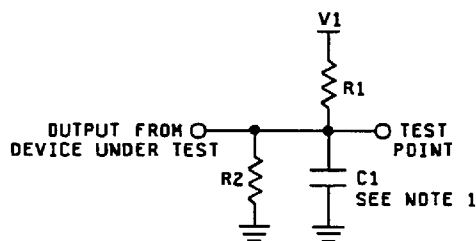
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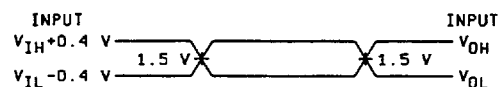
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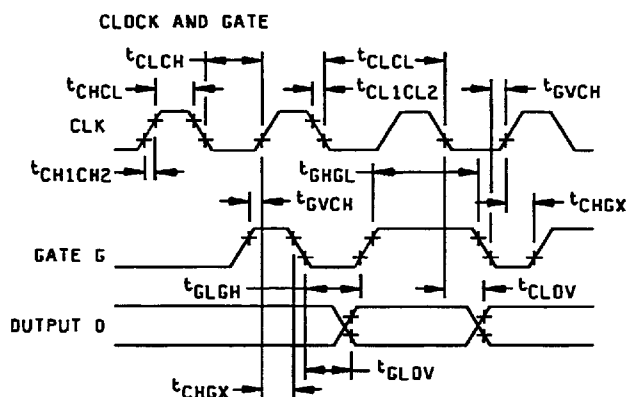
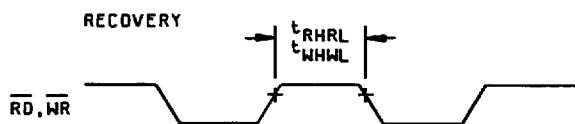
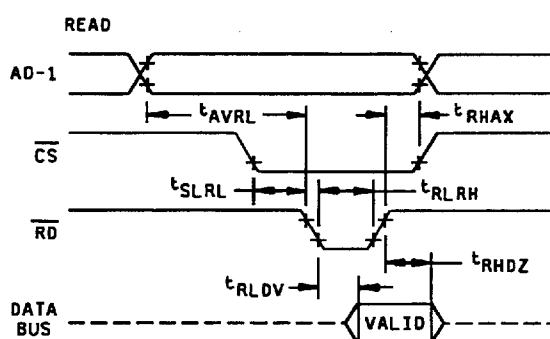
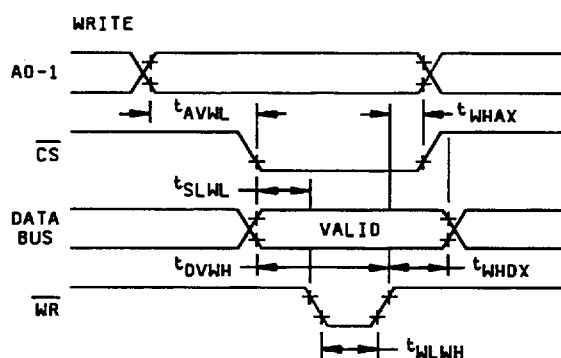
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C1 = 150 pF  
R1 = 510  $\Omega$   
V1 = 1.7 V  
R2 = open



All input signals must switch between  $V_{IL} - 0.4$  V and  $V_{IH} + 0.4$  V. Input rise and fall times are driven at 1 ns/V.



Note:

1. Includes stray jig capacitance.

FIGURE 3. Timing waveform and test circuit.

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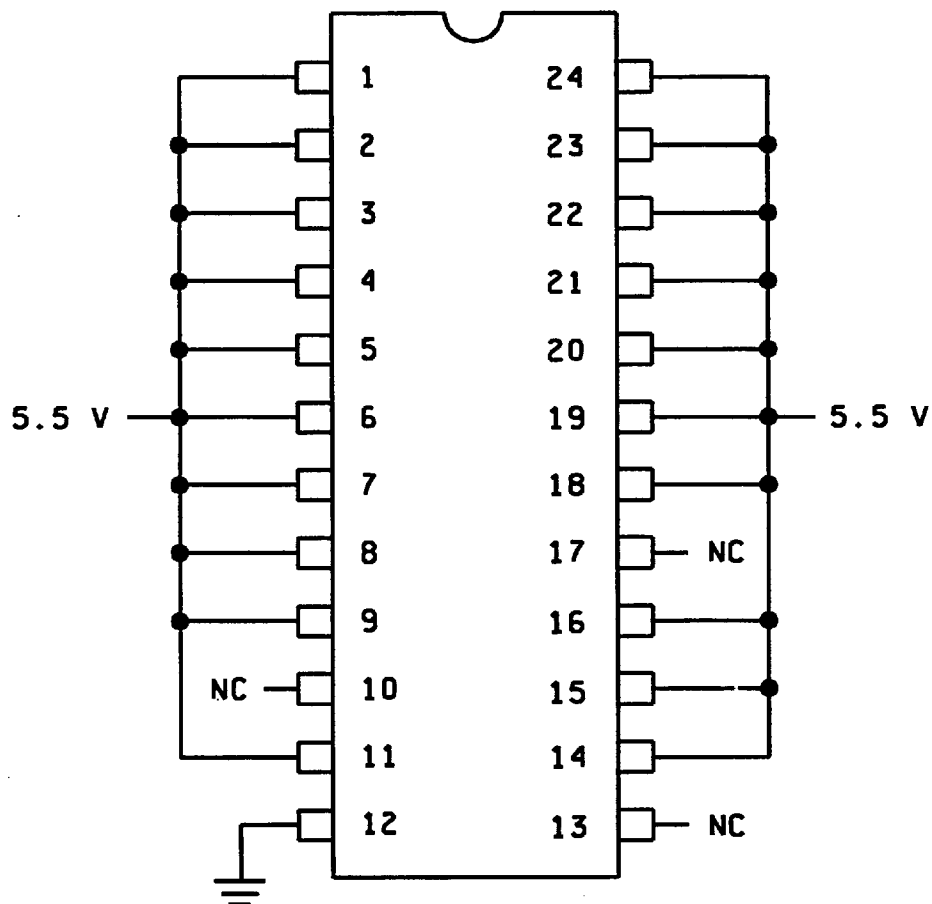
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**Notes:**

1.  $V_{DD} = 5.5V \pm 10\%$ ,  $T_A = +25^\circ C$

FIGURE 4. Radiation exposure circuit.

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#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

##### 4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

##### 4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535, or as modified in the device manufacturers approved Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535, or as specified in QM plan including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

##### 4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 ( $C_{IN}$ ,  $C_{OUT}$ , and  $C_{I/O}$  measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9, 1/ 10,11	1,2,3,7,8, 1/ 9,10,11	1,2,3,7, 2/ 8,9,10,11 3/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9 10,11	1,2,3,4,7,8, 9,10,11	1,2,3,4,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8 9,10,11	1,2,3,7,8 9,10,11	1,2,3,7,8 9,10,11 3/
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1 and 7.

2/ PDA applies to subgroups 1, 7 and delta's.

3/ Delta limits as specified in Table IIB herein shall be required where specified and the delta values shall be completed with reference to the zero hour.

Table IIB. Burn-in and operating life test (+25°C)

Parameters	Symbol	Delta limits
Standby power supply current	IDDSB	±2 µA
Output leakage current	IOZL, IOZH	±2 µA
Input leakage current	IIH, IIL	±200 nA
Output low current	IOL	±500 µA
TTL output high current	IOH TTL	±500 µA
CMOS output high current	IOH CMOS	±20 µA

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b.  $T_A = +125^\circ\text{C}$ , minimum.

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c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-I-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (See 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

- The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- The fluence shall be ≥ 100 errors or ≥ 10<sup>6</sup> ions/cm<sup>2</sup>.
- The flux shall be between 10<sup>2</sup> and 10<sup>5</sup> ions/cm<sup>2</sup>/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- The particle range shall be ≥ 20 microns in silicon.
- The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.
- Bias conditions shall be defined by the manufacturer for latchup measurements.
- Test four devices with zero failures.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V<sub>SS</sub> terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

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## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

Pin symbol	Type	Description															
D7-D0	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.															
CLK 0	I	CLOCK 0: Clock input of counter 0.															
OUT 0	O	OUT 0: Output of counter 0.															
GATE 0	I	GATE 0: Gate input of counter 0.															
GND		GROUND: Power supply connection.															
OUT 1	O	OUT 1: Output of counter 1.															
GATE 1	I	GATE 1: Gate input of counter 1.															
CLK 1	I	CLOCK 1: Clock input of counter 1.															
GATE 2	I	GATE 2: Gate input of counter 2.															
OUT 2	O	OUT 2: Output of counter 2.															
CLK 2	I	CLOCK 2: Clock input of counter 2.															
A0,A1	I	ADDRESS: Select inputs for one of the three counters or control word register for read/write operations. Normally connected to the system address bus.  <table> <tr> <td>A1</td><td>A0</td><td>Selects</td></tr> <tr> <td>0</td><td>0</td><td>Counter 0</td></tr> <tr> <td>0</td><td>1</td><td>Counter 1</td></tr> <tr> <td>1</td><td>0</td><td>Counter 2</td></tr> <tr> <td>1</td><td>1</td><td>Control word register</td></tr> </table>	A1	A0	Selects	0	0	Counter 0	0	1	Counter 1	1	0	Counter 2	1	1	Control word register
A1	A0	Selects															
0	0	Counter 0															
0	1	Counter 1															
1	0	Counter 2															
1	1	Control word register															
$\overline{\text{CS}}$	I	CHIP SELECT: A low on this input enables the device to respond to $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are ignored otherwise.															
$\overline{\text{RD}}$	I	READ: This input is low during CPU read operations.															
$\overline{\text{WR}}$	I	WRITE: This input is low during CPU write operations.															
$V_{DD}$		$V_{DD}$ : The +5 V power supply pin. A 0.1 $\mu\text{F}$ capacitor between pins 12 and 24 is recommended for decoupling.															

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6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

#### 6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Number of upsets (SEP).
- d. Number of transients (SEP).
- e. Occurrence of latchup (SEP).

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