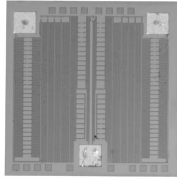


Megohm Center-Tap Chip Resistor



Product may not be to scale

The CTM resistor chips extends the resistance range to 10Meg in a center tap configuration while keeping the die size relatively small.

The CTMs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTMs are 100% electrically tested and visually inspected to MIL-STD-883.

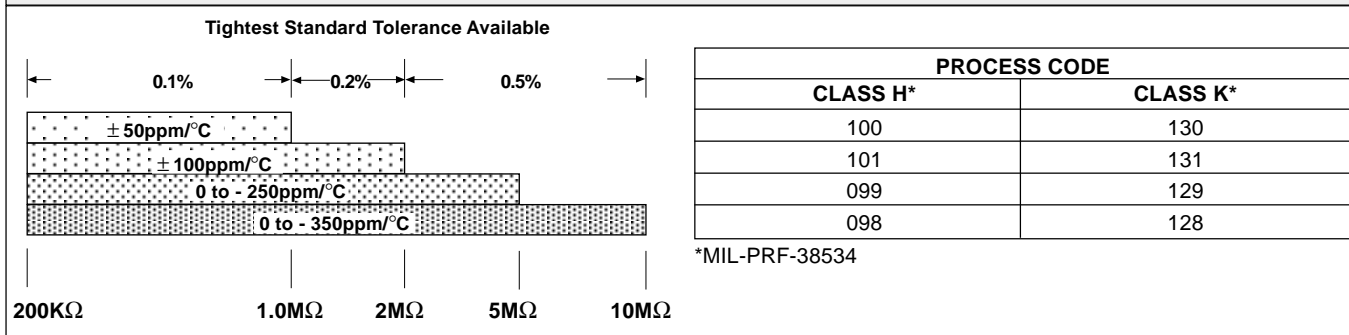
FEATURES

- Resistance range total: 200kΩ to 10MΩ
- Center Tap
- Chip size: 0.040 inches square
- Resistor material: tantalum nitride, self-passivating
- Moisture resistant

APPLICATIONS

Vishay EFI CTM tapped megohm resistor chips are designed for hybrid packages requiring high value, two resistor combinations.

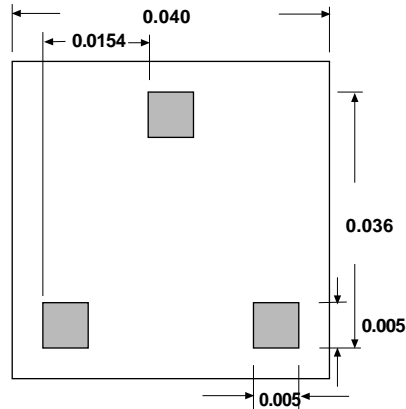
TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



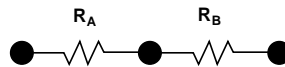
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between resistors	± 5ppm/°C
Ratio/ratio R_A/R_B tolerance	1.0 ± 1% standard
Noise	- 12dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum $\Delta R/R$
Stability, 1000 hours, + 125°C, 10mW	± 0.5% maximum absolute ± 0.05% ratio
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum $\Delta R/R$
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum $\Delta R/R$
Dielectric voltage breakdown	200V
Insulation resistance	10 ¹² minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	20mW each resistor
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum $\Delta R/R$

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DIMENSIONS in inches

SCHEMATIC

$$R_T = R_A + R_B$$


MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.040 x 0.040 ± 0.002 (1.02 x 1.02 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO ₂
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	3
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

OPTIONS: Gold back for eutectic die attach
 Custom Ratios available up to 4:1 R_A/R_B - Consult Vishay EFI Sales
 Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 2 MΩ, ± 1%, ± 100ppm/°C TCR, Aluminum Pads, Class H

P/N:	W	CTM	101	2000	3	F
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts per MIL-STD-883 X = Sample, visually inspected loaded in matrix trays (4% AQL)		See Process Code table	Use first 4 significant digits of resistance (R _T)	2 = 100 3 = 1000 4 = 10000	B = 0.1% C = 0.2% D = 0.5% F = 1.0% G = 2.0% H = 2.5% J = 5.0% K = 10% M = 20% L = 25%