FAIRCHILD SEMICONDUCTOR™

PRELIMINARY
January 1998

FM27C256
262,144-Bit (32K x 8) High Speed CMOS EPROM

General Description

The FM27C256 is a High Performance 32K x 8 UV Erasable EPROM. It is manufactured using an advanced CMOS process technology enabling it to operate at speeds as fast as 35 ns Address Access Time (t_{ACC}) and 35 ns Chip Enable Time (t_{CE}). It was designed utilizing Fairchild's self-aligned split gate EPROM cell, resulting in a low power device with a very cost effective die size. The low standby power capability of this 256K product (200 µA in a CMOS interface environment) is especially attractive.

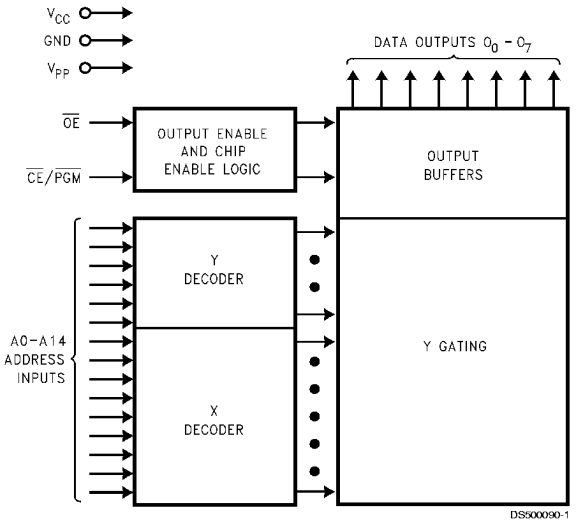
This product, with its high speed capability, is particularly appropriate for use with today's fast DSP processors and high-clock-rate microprocessors. The FM27C256's 35 ns speed enables these advanced processors to operate without introducing any undesirable wait states. The FM27C256 is also ideal for use in modem applications, and is recommended for use in these applications by the leading modem chip set manufacturer.

The FM27C256 is available in a variety of package types including the space saving 300 Mil DIP, the surface mount PLCC, and other windowed and non-windowed options. And its standard JEDEC EPROM pinouts provide for automatic upgrade density paths for current 64K and 128K EPROM users.

Features

- Fast Access Time
  - — t_{ACC} = 35 ns
  - — t_{CE} = 35 ns
- Low Power Consumption
  - — 200 µA Standby I_{CC}
- Immune to Latch-Up
  - — Up to 200 mA
- ESD Protection Exceeds 2000 Volts
- Available in 3090 Mil DIP and PLCC
- DESC SMD No. 5962-86063

Block Diagram



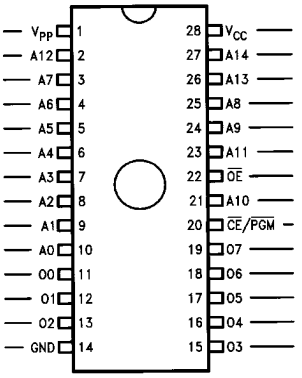
Product Selection Guide

Parameter	27C256-35	27C256-45	27C256-55	27C256-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
NM27C256 Q, N, V 100	15 ns	20 ns	25 ns	30 ns

Connection Diagram

27C080	27C040	27C020	27C010	27C512
A19	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A16	A16	A16	A16	
A15	A15	A15	A15	A15
A12	A12	A12	A12	A12
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O0	O0	O0	O0	O0
O1	O1	O1	O1	O1
O2	O2	O2	O2	O2
GND	GND	GND	GND	GND

DIP
NM27C256



27C512	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/$\overline{PGM}$	XX/$\overline{PGM}$	A18	A18
V_{CC}	XX	A17	A17	A17
A14	A14	A14	A14	A14
A13	A13	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
A11	A11	A11	A11	A11
$\overline{OE}$/V_{PP}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/V_{PP}
A10	A10	A10	A10	A10
$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$/$\overline{PGM}$
O7	O7	O7	O7	O7
O6	O6	O6	O6	O6
O5	O5	O5	O5	O5
O4	O4	O4	O4	O4
O3	O3	O3	O3	O3

DS500090-2

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the FM27C256 pins.

Commercial Temp. Range (0˚C to +70˚C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
FM27C256 Q, N, V 35	35
FM27C256 Q, N, V 45	45
FM27C256 Q, N, V 55	55
FM27C256 Q, N, V 70	70

Extended Temp. Range (–40˚C to +85˚C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
FM27C256 QE, NE, VE 45	45
FM27C256 QE, NE, VE 55	55
FM27C256 QE, NE, VE 70	70

Package Types: FM27C256 Q, N, V XXX

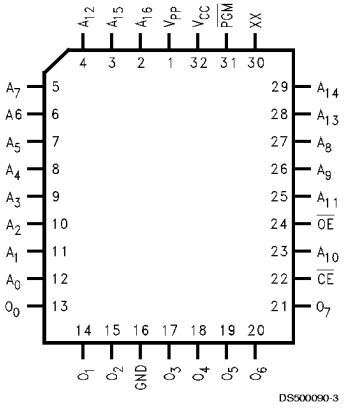
Q = Quartz-Windowed Ceramic DIP package

N = Plastic OTP DIP

V = Surface-Mount PLCC

- All Packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

PLCC



DS500090-3

Top

Pin Names

Symbol	Description
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (during Read)

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65˚C to +150˚C
All Input Voltages except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A_9 with Respect to Ground	−0.6V to +14V
ESD Protection	> 2000V

Operating Range

Range	Temperature	V_{CC}
Commercial	0˚C to +70˚C	+5V ±10%
Industrial	−40˚C to +85˚C	+5V ±10%

Read Operation

DC Electrical Characteristics

Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Voltage	(Note 6)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 6)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V (Note 2)	Comm'l		200	µA
			Industrial		500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH} (Note 3)	Comm'l		3	mA
			Industrial		5	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Note 2) and (Note 4) Outputs not loaded	Comm'l		25	mA
			Industrial		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Note 3) and (Note 4) Outputs not loaded	Comm'l		50	mA
			Industrial		60	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V or GND		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	µA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.

Note 3: TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.

Note 4: Add 3 mA/MHz for AC power component.

Note 5: These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

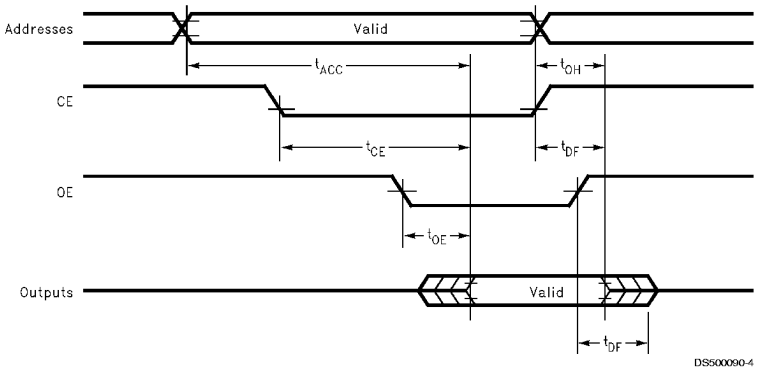
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

AC Read Characteristics

Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	-35		-45		-55		-70		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		35		45		55		70	ns
t_{CE}	$\overline{CE}$ to Output Delay		35		45		55		70	
t_{OE}	$\overline{OE}$ to Output Delay		15		20		25		30	
t_{DF} (Note 6)	Output Disable to Output Float		20		20		25		30	
t_{OH}	Address to Output Hold	0		0		0		0		

AC Waveforms



Capacitance (Note 6)

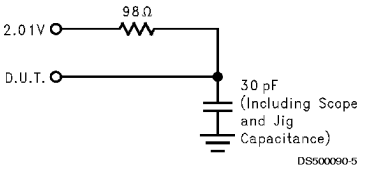
T_A = +25˚C, f = 1 MHz

Symbol	Parameter	Conditions	Typ (Note 7)	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

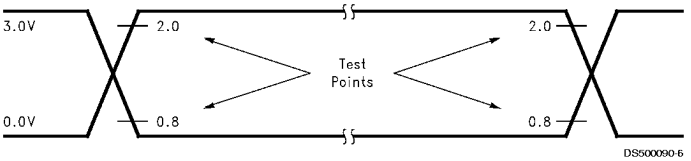
Note 6: This parameter is only sampled and is not 100% tested.

Note 7: Typical values are for T_A = 25˚C and nominal supply voltages.

Test Load (High Impedance Test Systems)



AC Testing Input/Output Waveform



AC testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

Note 8: Provide adequate decoupling capacitance as close as possible to this device to achieve the published AC and DC parameters. A 0.1 microfarad capacitor in parallel with a 0.01 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

DC Programming Characteristics

(T_A = 25°C ± 5°C, V_{CC} = 6.25 ± 0.25 V, V_{PP} = 12.75 ± 0.25V)

Symbol	Parameter	Min	Max	Units
I_{LI}	Input leakage Current (V_{IN} = V_{CC} or GND	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}/\overline{OE}$ = V_{IL})		60	mA
I_{CC}	V_{PP} Supply Current (Note 9)		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = −4 mA)	2.4		V

Note 9: V_{CC} must be applied coincidentally or before V_{PP} and removed coincidentally or after V_{PP}.

Note 10: V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.

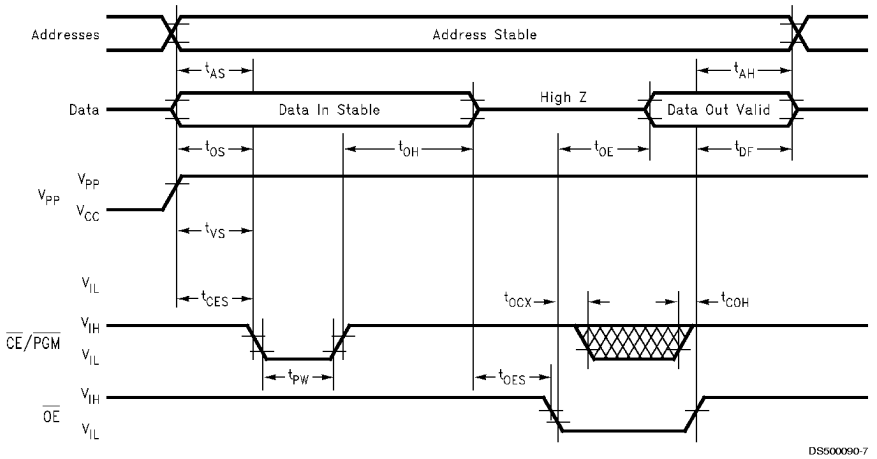
Note 11: During power up the $\overline{PGM}$ pin must be brought high (≥ V_{IH}) either coincident with or before power is applied to V_{PP}.

AC Programming Characteristics

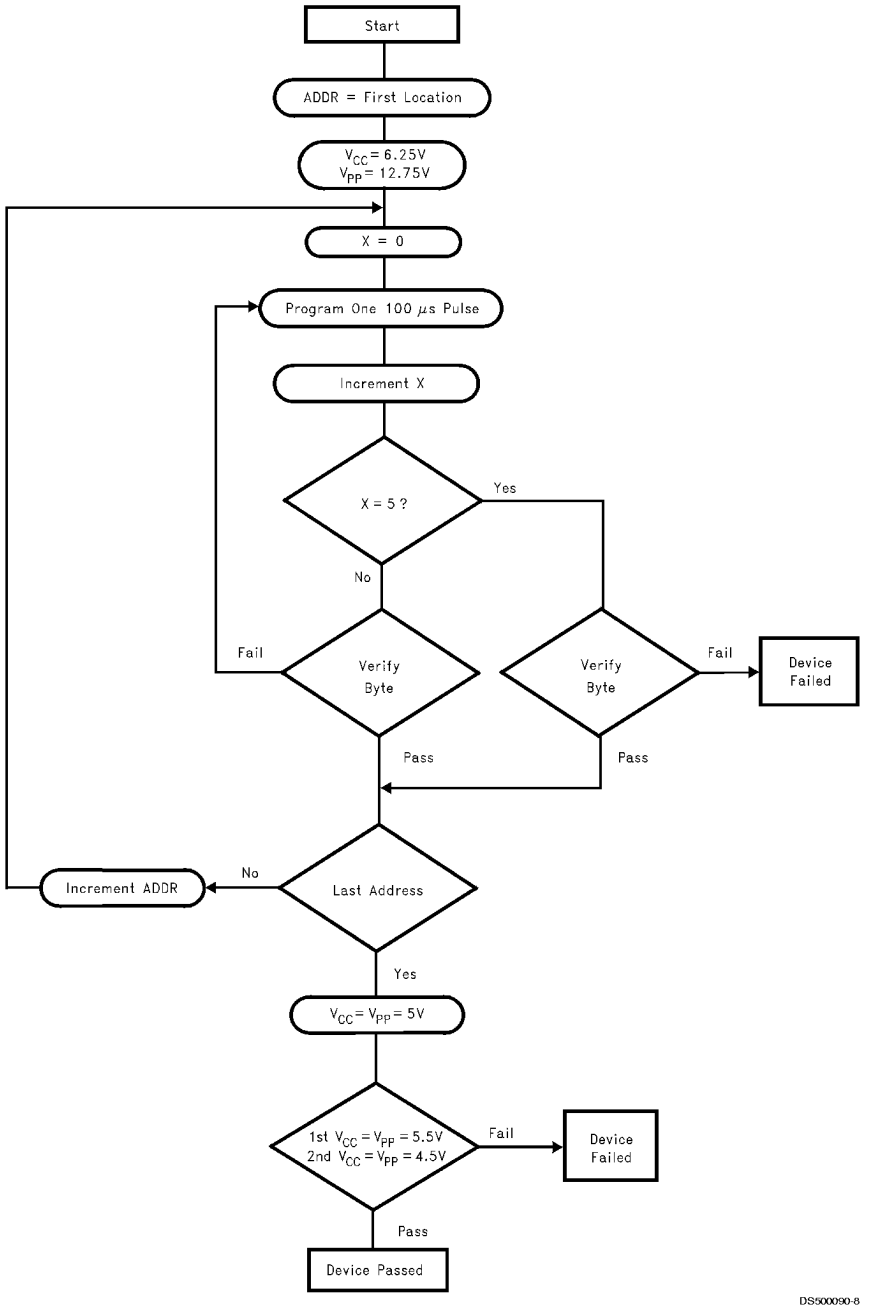
(T_A = 25°C ± 5°C, V_{CC} = 6.25 ± 0.25 V, V_{PP} = 12.75 ± 0.25V)

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Setup Time	2			µs
t_{COH}	$\overline{CE}$ High to $\overline{OE}$ High	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid from Output Enable			130	ns
t_{VS}/t_{CES}	V_{PP} Setup Time/$\overline{CE}$ Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	100		200	µs
t_{OCX}	$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	2			µs

Programming Waveform



Fast Programming Algorithm



Mode Selection

The modes of operation of FM27C256 listed below. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $V_{PP}$and A_9 for device signature.

TABLE 1. Modes Selection

Pins / Mode	$\overline{CE}$ /$\overline{PGM}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	X	X	V_{PP} (Note 13)	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	X	X	V_{PP} (Note 13)	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	V_{PP} (Note 13)	V_{CC}	High Z
Signature (Note 14)	V_{IL}	V_{IL}	V_{IH} (Note 13)	V_{IL}	V_{CC}	V_{CC}	23 H (Note 15)
	V_{IL}	V_{IL}	V_{IH} (Note 13)	V_{IL}	V_{CC}	V_{CC}	EO H (Note 16)

Note 12: X can be V_{IL} or V_{IH}.

Note 13: $V_{IH} = V_{PP} = 12.75 \pm 0.25$ V.

Note 14: A1 - A8, A10 - A14 = V_{IL}.

Note 15: Manufacturer Signature.

Note 16: Device Signature.

Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com