Data Sheet July 1999 File Number 4619.1

Radiation Hardened Octal Bus Transceiver, Three-State, Non-Inverting

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCTS245T is a Radiation Hardened Non-Inverting Octal Bidirectional Bus Transceiver, Three-State, intended for two-way asynchronous communication between data busses. The HCTS245T allows data transmission from the A bus to the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the data direction. The output enable input ($\overline{OE}$) puts the I/O port in the high-impedance state when high.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HCTS245T are contained in SMD 5962-95745. A "hot-link" is provided from our website for downloading**.**
www.intersil.com/spacedefense/newsafclasst.asp

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/quality/manuals.asp

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9574501TRC	HCTS245DTR	-55 to 125
5962R9574501TXC	HCTS245KTR	-55 to 125

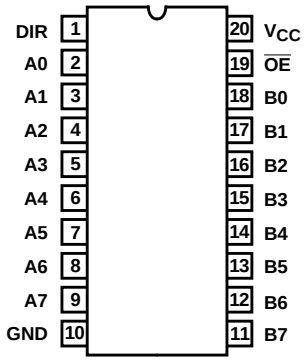
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

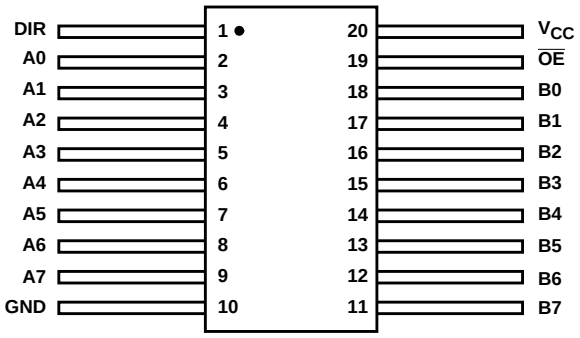
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - Latch-Up Free Under Any Conditions
  - SEP Effective LET No Upsets: >100 MEV-cm^2/mg
  - Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened CMOS SOS
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - V_{IL} = 0.8V Max
  - $V_{IH} = V_{CC/2}$ Min
- Input Current Levels Ii ≤ 5mA at V_{OL}, V_{OH}

Pinouts

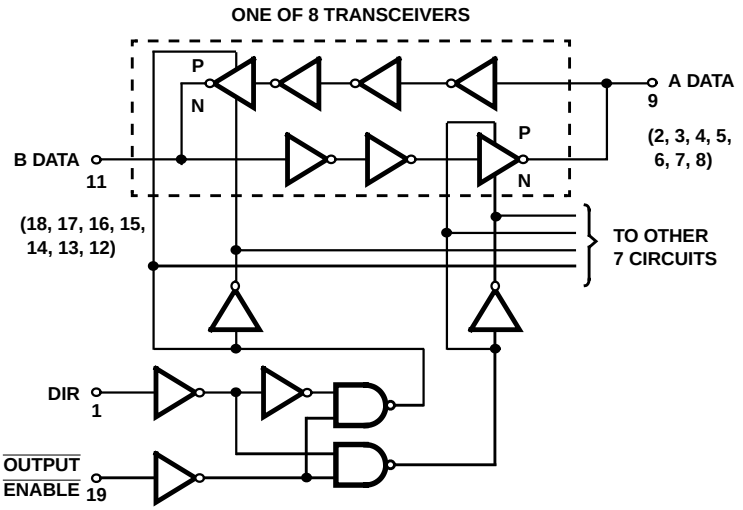
HCTS245DTR (SBDIP), CDIP2-T20
TOP VIEW



HCTS245KTR (FLATPACK), CDFP4-F20
TOP VIEW



Functional Diagram



TRUTH TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = High Voltage Level, L = Low Voltage Level,
X = Immaterial

To prevent excess currents in the High-Z (Isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

Die Characteristics

DIE DIMENSIONS:

(3149µm x 2794µm x 533µm ±51µm)

124 x 110 x 21mils ±2mil

METALLIZATION:

Type: Al Si

Thickness: 11.0kÅ ±1kÅ

SUBSTRATE POTENTIAL:

Unbiased Silicon on Sapphire

BACKSIDE FINISH:

Sapphire

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 13kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

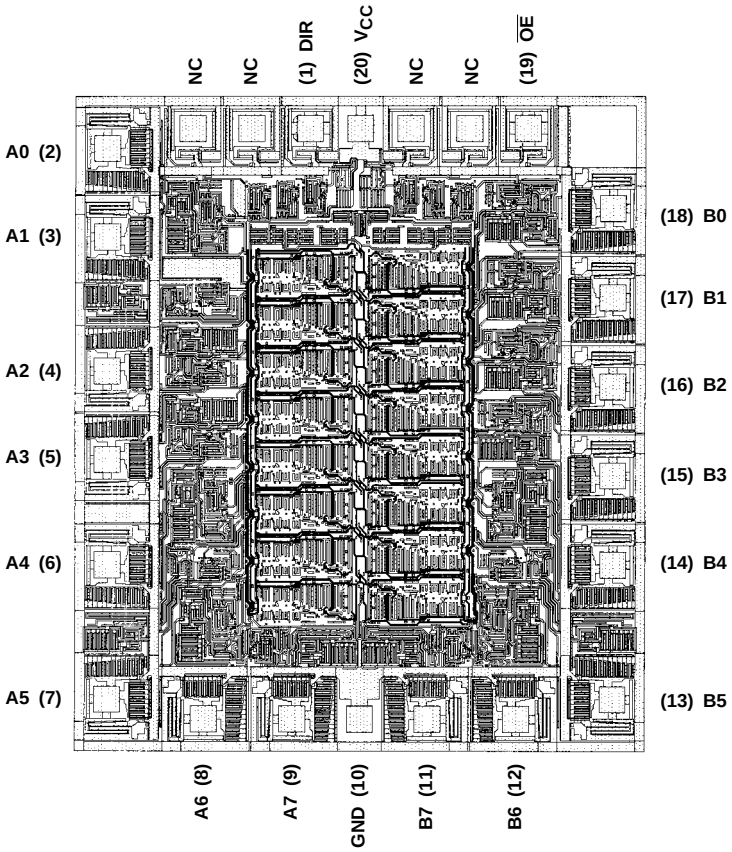
274

PROCESS:

CMOS SOS

Metallization Mask Layout

HCTS245T



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS245 is TA14417A.