

## MEMORY

**CMOS 1M × 4 BIT  
FAST PAGE MODE DYNAMIC RAM****MB81V4400C-60/-70****CMOS 1,048,576 × 4 BIT Fast Page Mode Dynamic RAM****DESCRIPTION**

The Fujitsu MB81V4400C is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 4-bit increments. The MB81V4400C features a "fast page" mode of operation whereby high-speed random access of up to 1,024 × 4-bits of data within the same row can be selected. The MB81V4400C DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81V4400C is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81V4400C is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81V4400C are not critical and all inputs are LVTTTL compatible.

**PRODUCT LINE & FEATURES**

Parameter		MB81V4400C-60	MB81V4400C-70
RAS Access Time		60 ns max.	70 ns max.
CAS Access Time		15 ns min.	20 ns min.
Address Access Time		30 ns max.	35 ns max.
Random Cycle Time		110 ns max.	125 ns max.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Low power Dissipation	Operating current	220 mW max.	195 mW max.
	Standby current	7.2 mW max. (LVTTTL level)/3.6 mW max. (CMOS level)	

- 1,048,576 words × 4 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are LVTTTL compatible
- 1024 refresh cycles every 16.4 ms
- Self refresh function
- Early write or  $\overline{OE}$  controlled write capability
- $\overline{RAS}$ -only,  $\overline{CAS}$ -before- $\overline{RAS}$ , or Hidden Refresh
- Fast page Mode, Read-Modify-Write Capability
- On chip substrate bias generator for high Performance

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

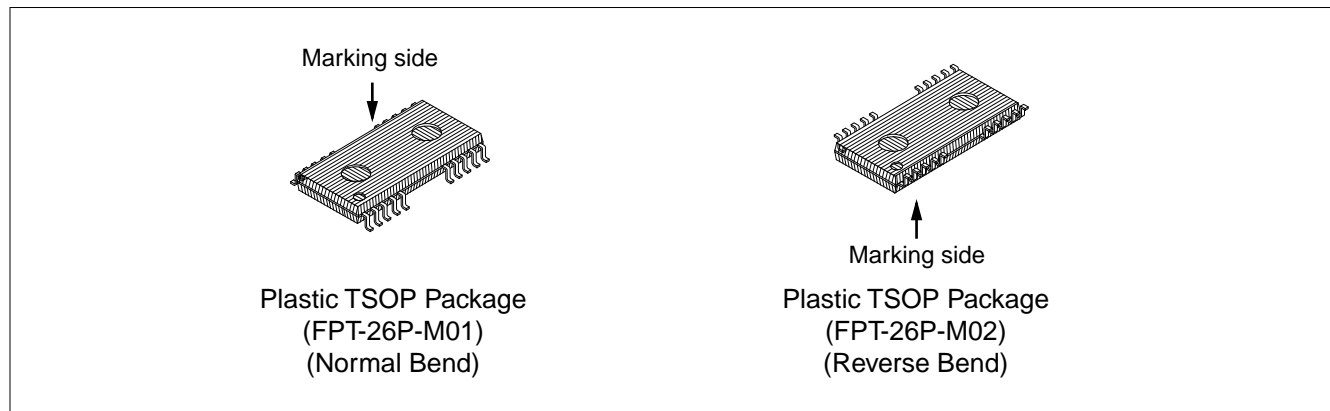
# MB81V4400C-60/MB81V4400C-70

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to +4.6	V
Voltage of $V_{CC}$ supply relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Power Dissipation	$P_D$	1.0	W
Short Circuit Output Current	$I_{OUT}$	-55 to +50	mA
Storage Temperature	$T_{STG}$	-55 to +125	°C

**WARNING:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ■ PACKAGE

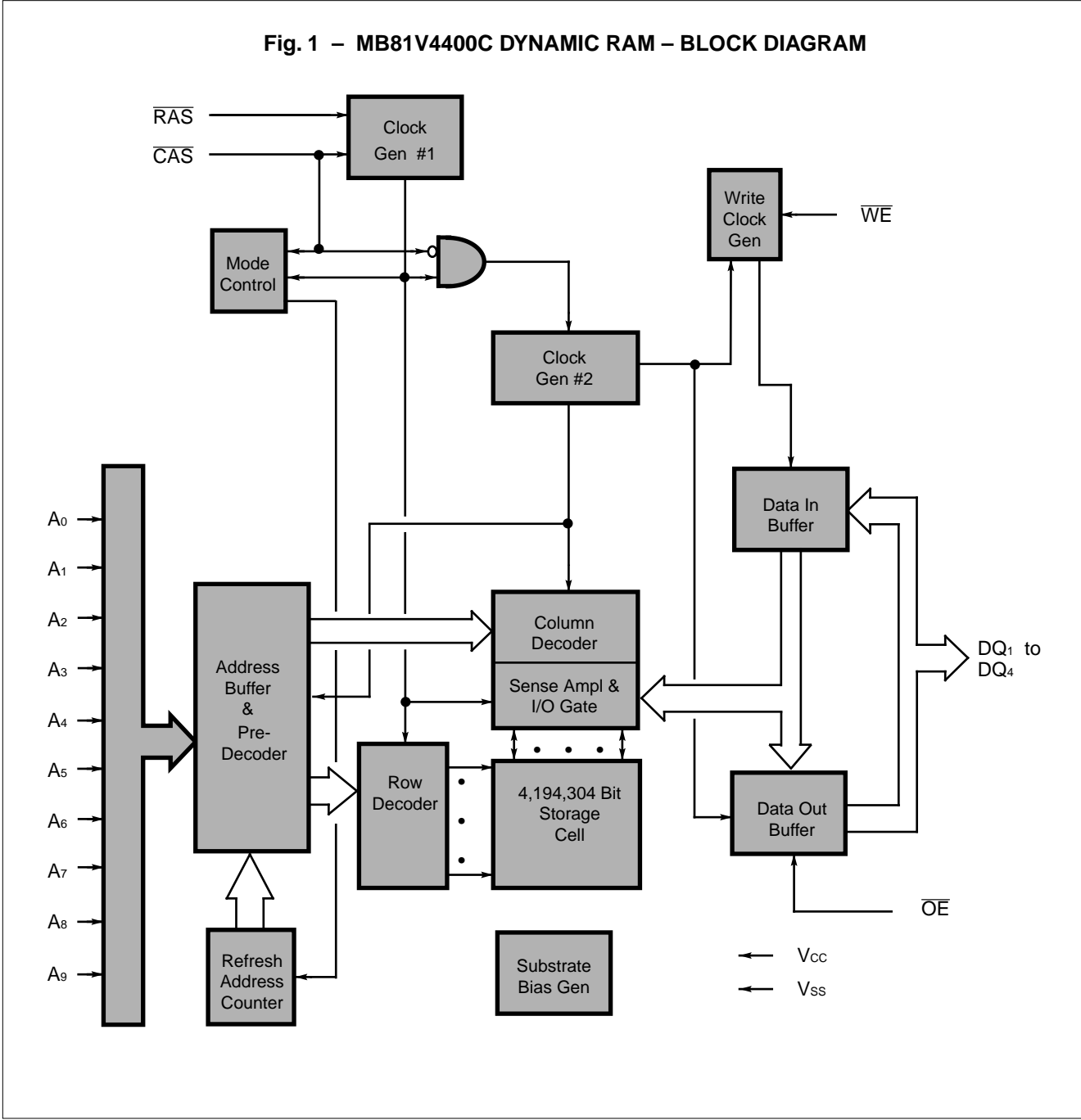


### Package and Ordering Information

- 26-pin plastic (300 mil) TSOP-II with normal bend leads, order as MB81V4400C-xxPFTN
- 26-pin plastic (300 mil) TSOP-II with reverse bend leads, order as MB81V4400C-xxPFTR

# MB81V4400C-60/MB81V4400C-70

**Fig. 1 – MB81V4400C DYNAMIC RAM – BLOCK DIAGRAM**



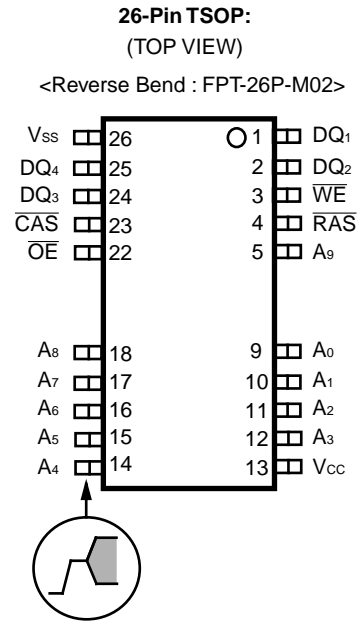
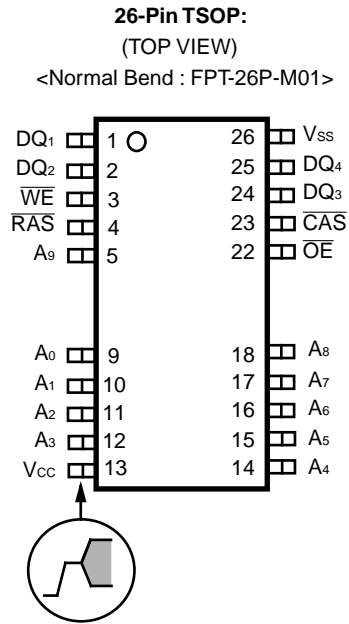
**■ CAPACITANCE**

(T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A <sub>0</sub> to A <sub>9</sub>	C <sub>IN1</sub>	—	5	pF
Input Capacitance, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	C <sub>IN2</sub>	—	7	pF
Input/Output Capacitance, DQ <sub>1</sub> to DQ <sub>4</sub>	C <sub>DQ</sub>	—	7	pF

# MB81V4400C-60/MB81V4400C-70

## ■ PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
DQ <sub>1</sub> to DQ <sub>4</sub>	Data Input/Output.
$\overline{WE}$	Write Enable.
RAS	Row address strobe.
A <sub>0</sub> to A <sub>9</sub>	Address inputs.
V <sub>CC</sub>	+3.3 volt power supply
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
V <sub>SS</sub>	Circuit ground.

# MB81V4400C-60/MB81V4400C-70

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp
Supply Voltage	1	$V_{CC}$	3.0	3.3	3.6	V	0°C to +70°C
		$V_{SS}$	0	0	0		
Input High Voltage, all inputs	1	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	
Input Low Voltage, all inputs*	1	$V_{IL}$	-0.3	—	0.8	V	

\* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

## ■ FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any four of 4,194,304 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by  $\overline{CAS}$  and  $\overline{RAS}$  as shown in Figure 5. First, ten row address bits are input on pins  $A_0$ -through- $A_9$  and latched with the row address strobe ( $\overline{RAS}$ ) then, ten column address bits are input and latched with the column address strobe ( $\overline{CAS}$ ). Both row and column addresses must be stable on or before the falling edge of  $\overline{CAS}$  and  $\overline{RAS}$ , respectively. The flow-through latch type is used for the address latch; thus, address information appearing after  $t_{RAH}$  (min.)+  $t_r$  is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of  $\overline{WE}$ . When  $\overline{WE}$  is active Low, a write cycle is initiated; when  $\overline{WE}$  is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an  $\overline{OE}$  (delayed) write cycle, and a read-modify-write cycle. The falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data ( $DQ_1$ - $DQ_4$ ) is strobed by  $\overline{CAS}$  and the setup/hold times are referenced to the falling edge of  $\overline{CAS}$  because  $\overline{WE}$  goes Low before  $\overline{CAS}$ . In a delayed write or a read-modify-write cycle,  $\overline{WE}$  goes Low after  $\overline{CAS}$ ; thus, input data is strobed by  $\overline{WE}$  and all setup/hold times are referenced to the falling edge of  $\overline{WE}$ .

### DATA OUTPUT

The three-state buffers are LVTTTL compatible with a fanout of one TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- $t_{RAC}$  : from the falling edge of  $\overline{RAS}$  when  $t_{RCD}$  (max.) is satisfied.
- $t_{CAC}$  : from the falling edge of  $\overline{CAS}$  when  $t_{RCD}$  is greater than  $t_{RCD}$  (max.).
- $t_{AA}$  : from column address input when  $t_{RAD}$  is greater than  $t_{RAD}$  (max.).
- $t_{OEA}$  : from the falling edge of  $\overline{OE}$  when  $\overline{OE}$  is brought Low after  $t_{RAC}$ ,  $t_{CAC}$ , or  $t_{AA}$ .

The data remains valid until either  $\overline{CAS}$  or  $\overline{OE}$  returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

### FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions,  $\overline{RAS}$  is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 1,024 × 4-bits can be accessed and, when multiple MB81V4400Cs are used,  $\overline{CAS}$  is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

# MB81V4400C-60/MB81V4400C-70

## ■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min.	Typ.	Max.	
Output high voltage	1	$V_{OH}$	$I_{OH} = -2 \text{ mA}$	2.4	—	—	V
Output low voltage	1	$V_{OL}$	$I_{OL} = 2 \text{ mA}$	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	$0 \text{ V} \leq V_{IN} \leq 3.6 \text{ V}$ $3.0 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$ $V_{SS} = 0 \text{ V}$ ; All other pins not under test = $0 \text{ V}$	-10	—	10	$\mu\text{A}$
Output leakage current		$I_{O(L)}$	$0 \text{ V} \leq V_{OUT} \leq 3.6 \text{ V}$ Data out disabled	-10	—	10	
Operating current (Average Power supply current) 2	MB81V4400C-60	$I_{CC1}$	$\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ cycling; $t_{RC} = \text{min.}$	—	—	61	mA
	MB81V4400C-70					54	
Standby current (Power supply current)	LVTTL level	$I_{CC2}$	$\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$	—	—	2.0	mA
	CMOS level		$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$			1.0	
Refresh current#1 (Average power supply current) 2	MB81V4400C-60	$I_{CC3}$	$\overline{\text{CAS}} = V_{IH}$ , $\overline{\text{RAS}}$ cycling; $t_{RC} = \text{min.}$	—	—	61	mA
	MB81V4400C-70					54	
Fast Page Mode current 2	MB81V4400C-60	$I_{CC4}$	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ cycling; $t_{PC} = \text{min.}$	—	—	41	mA
	MB81V4400C-70					37	
Refresh current#2 (Average power supply current) 2	MB81V4400C-60	$I_{CC5}$	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ ; $t_{RC} = \text{min.}$	—	—	49	mA
	MB81V4400C-70					44	
Refresh current#3 (Average power supply current)	MB81V4400C-60	$I_{CC9}$	$\overline{\text{RAS}} = \overline{\text{CAS}} \geq 0.2 \text{ V}$ Self refresh;	—	—	1000	$\mu\text{A}$
	MB81V4400C-70					1000	

# MB81V4400C-60/MB81V4400C-70

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V4400C-60		MB81V4400C-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t <sub>REF</sub>	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t <sub>RC</sub>	110	—	125	—	ns
3	Read-Modify-Write Cycle Time		t <sub>RWC</sub>	150	—	170	—	ns
4	Access Time from $\overline{\text{RAS}}$	6, 9	t <sub>RAC</sub>	—	60	—	70	ns
5	Access Time from $\overline{\text{CAS}}$	7, 9	t <sub>CAC</sub>	—	15	—	20	ns
6	Column Address Access Time	8, 9	t <sub>AA</sub>	—	30	—	35	ns
7	Output Hold Time		t <sub>OH</sub>	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t <sub>ON</sub>	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t <sub>OFF</sub>	—	15	—	15	ns
10	Transition Time		t <sub>t</sub>	2	50	2	50	ns
11	$\overline{\text{RAS}}$ Precharge Time		t <sub>RP</sub>	40	—	45	—	ns
12	$\overline{\text{RAS}}$ Pulse Width		t <sub>RAS</sub>	60	100000	70	100000	ns
13	$\overline{\text{RAS}}$ Hold Time		t <sub>RSH</sub>	15	—	20	—	ns
14	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t <sub>CRP</sub>	0	—	0	—	ns
15	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	11, 12	t <sub>RCD</sub>	20	45	20	50	ns
16	$\overline{\text{CAS}}$ Pulse Width		t <sub>CAS</sub>	15	10000	20	10000	ns
17	$\overline{\text{CAS}}$ Hold Time		t <sub>CSH</sub>	60	—	70	—	ns
18	$\overline{\text{CAS}}$ Precharge Time (Normal)	19	t <sub>CPN</sub>	10	—	10	—	ns
19	Row Address Set Up Time		t <sub>ASR</sub>	0	—	0	—	ns
20	Row Address Hold Time		t <sub>RAH</sub>	10	—	10	—	ns
21	Column Address Set Up Time		t <sub>ASC</sub>	0	—	0	—	ns
22	Column Address Hold Time		t <sub>CAH</sub>	12	—	12	—	ns
23	$\overline{\text{RAS}}$ to Column Address Delay Time	13	t <sub>RAD</sub>	15	30	15	35	ns
24	Column Address to $\overline{\text{RAS}}$ Lead Time		t <sub>RAL</sub>	30	—	35	—	ns
25	Column Address to $\overline{\text{CAS}}$ Lead Time		t <sub>CAL</sub>	30	—	35	—	ns
26	Read Command Set Up Time		t <sub>RCS</sub>	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	14	t <sub>RRH</sub>	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	14	t <sub>RCH</sub>	0	—	0	—	ns
29	Write Command Set Up Time	15	t <sub>WCS</sub>	0	—	0	—	ns
30	Write Command Hold Time		t <sub>WCH</sub>	10	—	10	—	ns
31	$\overline{\text{WE}}$ Pulse Width		t <sub>WP</sub>	10	—	10	—	ns
32	Write Command to $\overline{\text{RAS}}$ Lead Time		t <sub>RWL</sub>	15	—	18	—	ns
33	Write Command to $\overline{\text{CAS}}$ Lead Time		t <sub>CWL</sub>	15	—	18	—	ns

# MB81V4400C-60/MB81V4400C-70

## ■ AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

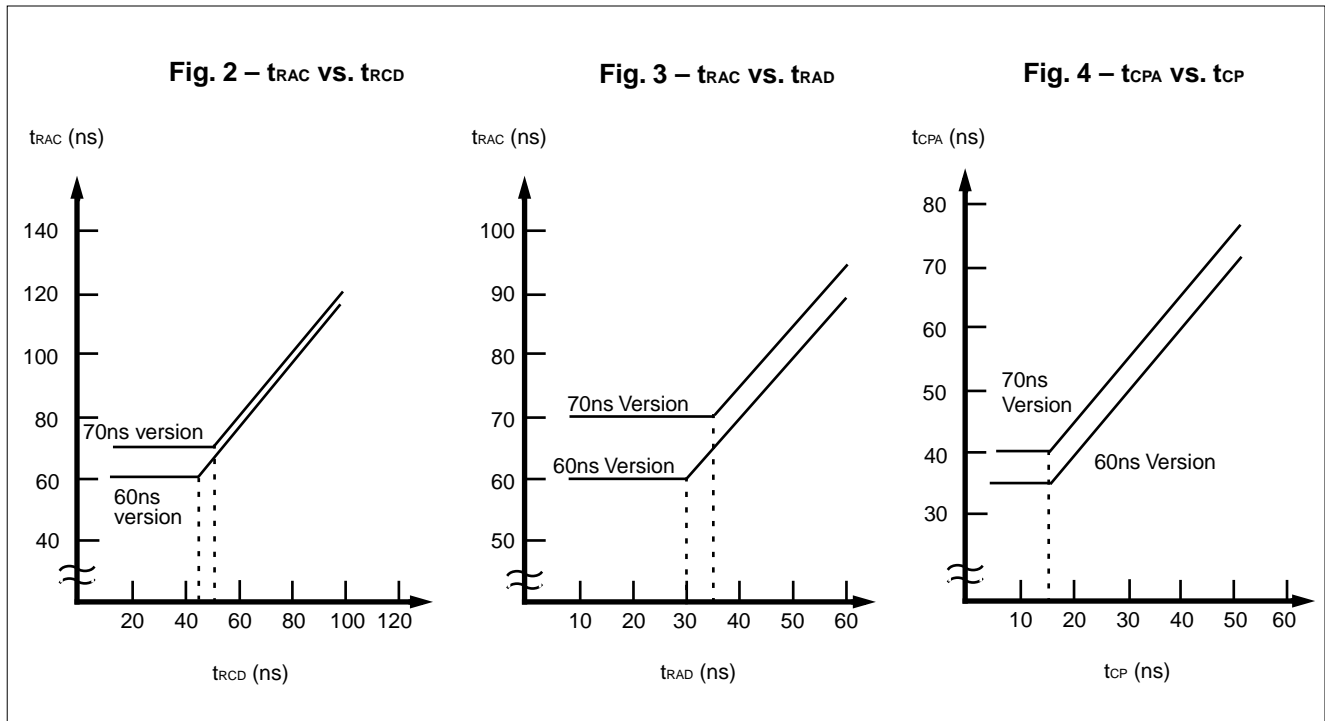
No.	Parameter	Notes	Symbol	MB81V4400C-60		MB81V4400C-70		Unit
				Min.	Max.	Min.	Max.	
34	DIN Set Up Time		t <sub>DS</sub>	0	—	0	—	ns
35	DIN Hold Time		t <sub>DH</sub>	10	—	10	—	ns
36	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time		t <sub>RWD</sub>	80	—	90	—	ns
37	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time		t <sub>CWD</sub>	35	—	40	—	ns
38	Column Address to $\overline{\text{WE}}$ Delay Time		t <sub>AWD</sub>	50	—	55	—	ns
39	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh cycles)		t <sub>RPC</sub>	5	—	5	—	ns
40	$\overline{\text{CAS}}$ Set Up Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh		t <sub>CSR</sub>	0	—	0	—	ns
41	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh		t <sub>CHR</sub>	10	—	10	—	ns
42	$\overline{\text{WE}}$ SetUp Time from $\overline{\text{RAS}}$	20	t <sub>WSR</sub>	0	—	0	—	ns
43	$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$	20	t <sub>WHR</sub>	10	—	10	—	ns
44	Access Time from $\overline{\text{OE}}$	9	t <sub>OEA</sub>	—	15	—	20	ns
45	Output Buffer Turn Off Delay from $\overline{\text{OE}}$	10	t <sub>OEZ</sub>	—	15	—	15	ns
46	$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Lead Time for Valid Data		t <sub>OEL</sub>	10	—	10	—	ns
47	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$	16	t <sub>OEH</sub>	0	—	0	—	ns
48	$\overline{\text{OE}}$ to Data in Delay Time		t <sub>OED</sub>	15	—	15	—	ns
49	DIN to $\overline{\text{CAS}}$ Delay Time	17	t <sub>DZC</sub>	0	—	0	—	ns
50	DIN to $\overline{\text{OE}}$ Delay Time	17	t <sub>DZO</sub>	0	—	0	—	ns
51	Fast Page Mode Read/Write Cycle Time		t <sub>PC</sub>	40	—	45	—	ns
52	Fast Page Mode Read-Modify-Write Cycle Time		t <sub>PRWC</sub>	80	—	85	—	ns
53	Access Time from $\overline{\text{CAS}}$ Precharge	9, 18	t <sub>CPA</sub>	—	35	—	40	ns
54	Fast Page Mode $\overline{\text{CAS}}$ Precharge Time		t <sub>CP</sub>	10	—	10	—	ns
55	Fast Page Mode $\overline{\text{RAS}}$ Pulse width		t <sub>RASP</sub>	—	200000	—	200000	ns
56	Fast Page Mode $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge		t <sub>RHCP</sub>	35	—	40	—	ns
57	Fast Page Mode $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time		t <sub>CPWD</sub>	55	—	60	—	ns



# MB81V4400C-60/MB81V4400C-70

- Notes:
1. Referenced to  $V_{SS}$ .
  2.  $I_{CC}$  depends on the output load conditions and cycle rates; The specified values are obtained with the output open.  
 $I_{CC}$  depends on the number of address change as  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ ,  $V_{IL} > -0.3 V$ .  
 $I_{CC1}$ ,  $I_{CC3}$  and  $I_{CC5}$  are specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .  
 $I_{CC4}$  is specified at one time of address change during one Page cycle.
  3. An Initial pause ( $\overline{RAS} = \overline{CAS} = V_{IH}$ ) of 200  $\mu s$  is required after power-up followed by any eight  $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
  4. AC characteristics assume  $t_T = 5 ns$ .
  5. Input voltage levels are 0 V and 3.0 V, and input reference levels are  $V_{IH}$  (min.) and  $V_{IL}$  (max.) for measuring timing of input signals. Also, the transmission time ( $t_T$ ) is measured between  $V_{IH}$  (min.) and  $V_{IL}$  (max.). The output reference levels are  $V_{OH} = 2.0 V$  and  $V_{OL} = 0.8 V$ .
  6. Assumes that  $t_{RCD} \leq t_{RCD} (max.)$ ,  $t_{RAD} \leq t_{RAD} (max.)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds the value shown. Refer to Fig. 2 and 3.
  7. If  $t_{RCD} \geq t_{RCD} (max.)$ ,  $t_{RAD} \geq t_{RAD} (max.)$ , and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{CAC}$ .
  8. If  $t_{RAD} \geq t_{RAD} (max.)$  and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{AA}$ .
  9. Measured with a load equivalent to one TTL loads and 100 pF.
  10.  $t_{OFF}$  and  $t_{OEZ}$  is specified that output buffer change to high impedance state.
  11. Operation within the  $t_{RCD} (max.)$  limit ensures that  $t_{RAC} (max.)$  can be met.  $t_{RCD} (max.)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD} (max.)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  12.  $t_{RCD} (min.) = t_{RAH} (min.) + 2t_T + t_{ASC} (min.)$ .
  13. Operation within the  $t_{RAD} (max.)$  limit ensures that  $t_{RAC} (max.)$  can be met.  $t_{RAD} (max.)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD} (max.)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  14. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
  15.  $t_{WCS}$  is specified as a reference point only. If  $t_{WCS} \geq t_{WCS} (min.)$  the data output pin will remain High-Z state through entire cycle.
  16. Assumes that  $t_{WCS} < t_{WCS} (min.)$ .
  17. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
  18.  $t_{CPA}$  is access time from the selection of a new column address (that is caused by changing  $\overline{CAS}$  from "L" to "H"). Therefore, if  $t_{CP}$  is long,  $t_{CPA}$  is longer than  $t_{CPA} (max.)$ .
  19. Assumes that  $\overline{CAS}$ -before- $\overline{RAS}$  refresh.
  20. Assumes that Test mode function.

# MB81V4400C-60/MB81V4400C-70



## FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes*	$t_{\text{RCS}} \geq t_{\text{RCS}} (\text{min.})$
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes*	$t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min.})$
Read-Modify- Write Cycle	L	L	H → L	L → H	Valid	Valid	Valid	Valid	Yes*	$t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min.})$
$\overline{\text{RAS}}$ -only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	Yes	
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle	L	L	H	X	—	—	—	High-Z	Yes	$t_{\text{CSR}} \geq t_{\text{CSR}} (\text{min.})$
Hidden Refresh Cycle	H → L	L	H	L	—	—	—	Valid	Yes	Previous data is kept.
Test mode Set Cycle (CBR)	L	L	L	X	—	—	—	High-Z	Yes	$t_{\text{CSR}} \geq t_{\text{CSR}} (\text{min.})$ $t_{\text{WSR}} \geq t_{\text{WSR}} (\text{min.})$
Test mode Set Cycle (Hidden)	H → L	L	L	X	—	—	—	Valid	Yes	$t_{\text{CSR}} \geq t_{\text{CSR}} (\text{min.})$ $t_{\text{WSR}} \geq t_{\text{WSR}} (\text{min.})$

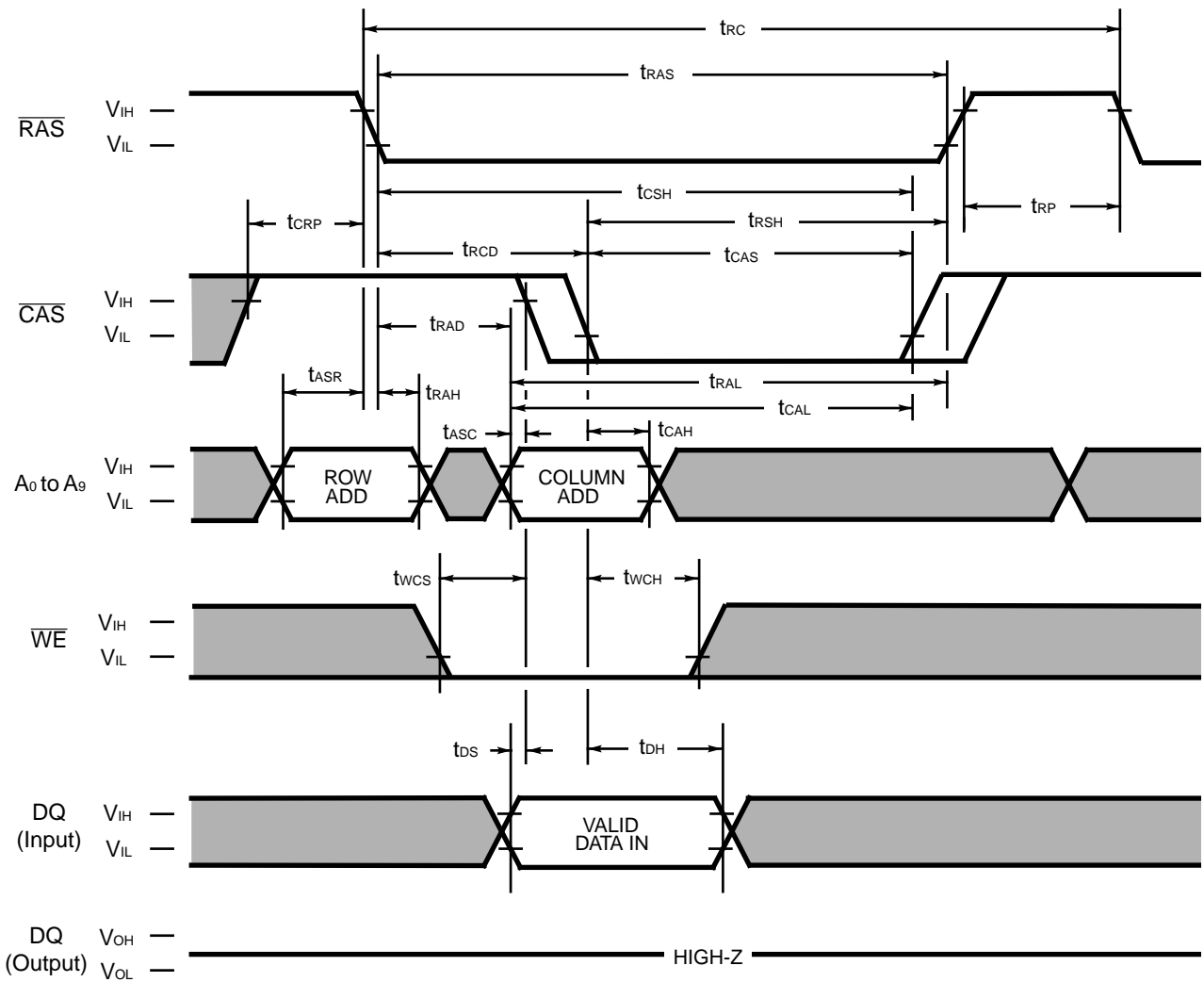
X; "H" or "L"

\*; It is impossible in Fast Page Mode.



# MB81V4400C-60/MB81V4400C-70

Fig. 6 – EARLY WRITE CYCLE ( $\overline{OE}$ ="H" or "L")



■ "H" or "L"

**DESCRIPTION**

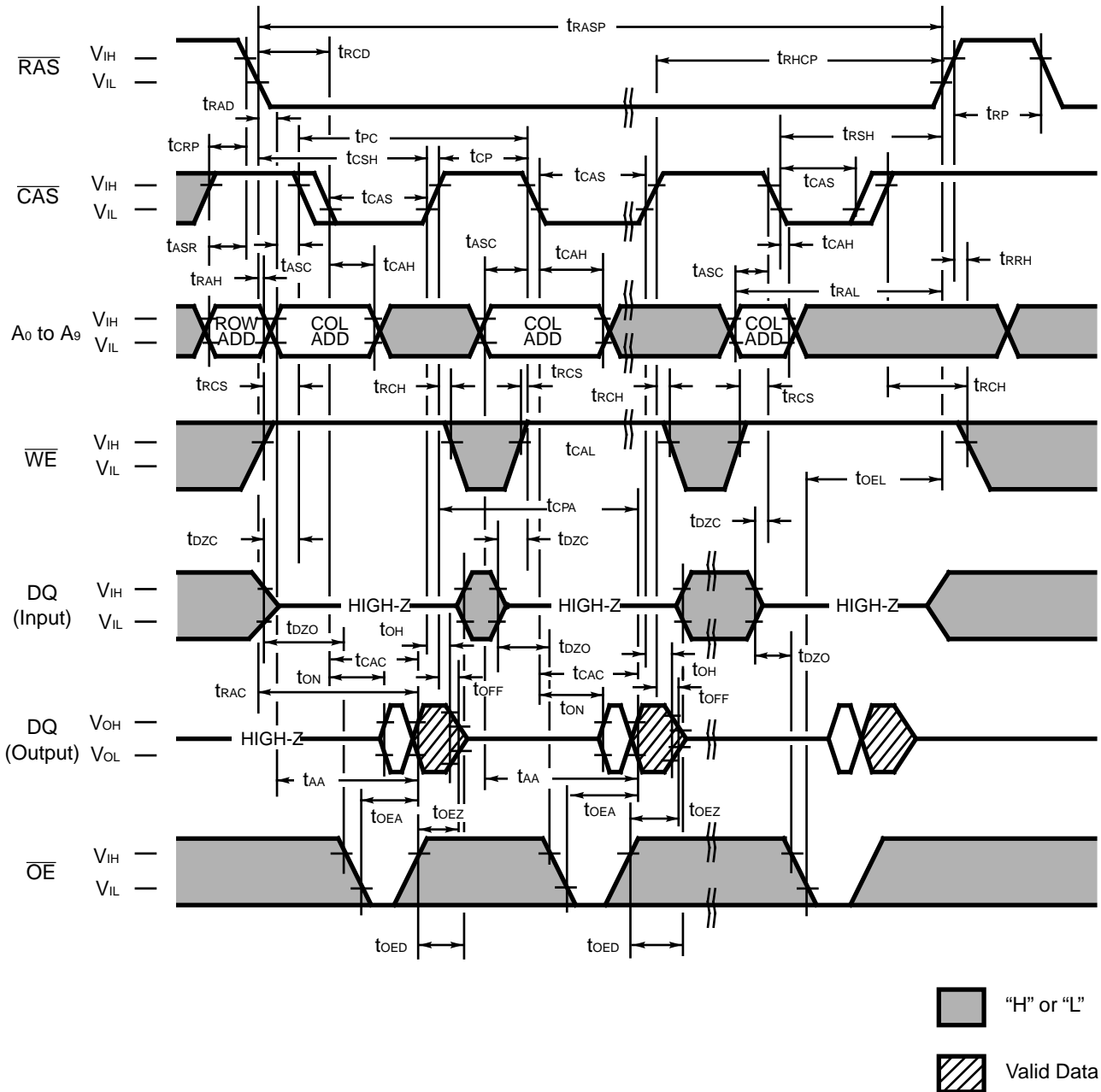
A write cycle is similar to a read cycle except  $\overline{WE}$  is set to a Low state and  $\overline{OE}$  is a "H" or "L" signal. A write cycle can be implemented in either of three ways—early write,  $\overline{OE}$  write (delayed write), or read-modify-write. During all write cycles, timing parameters  $t_{RWL}$ ,  $t_{CWL}$  and  $t_{RAL}$  must be satisfied. In the early write cycle shown above  $t_{WCS}$  satisfied, data on the DQ pin is latched with the falling edge of CAS and written into memory.





# MB81V4400C-60/MB81V4400C-70

Fig. 9 – FAST PAGE MODE READ CYCLE

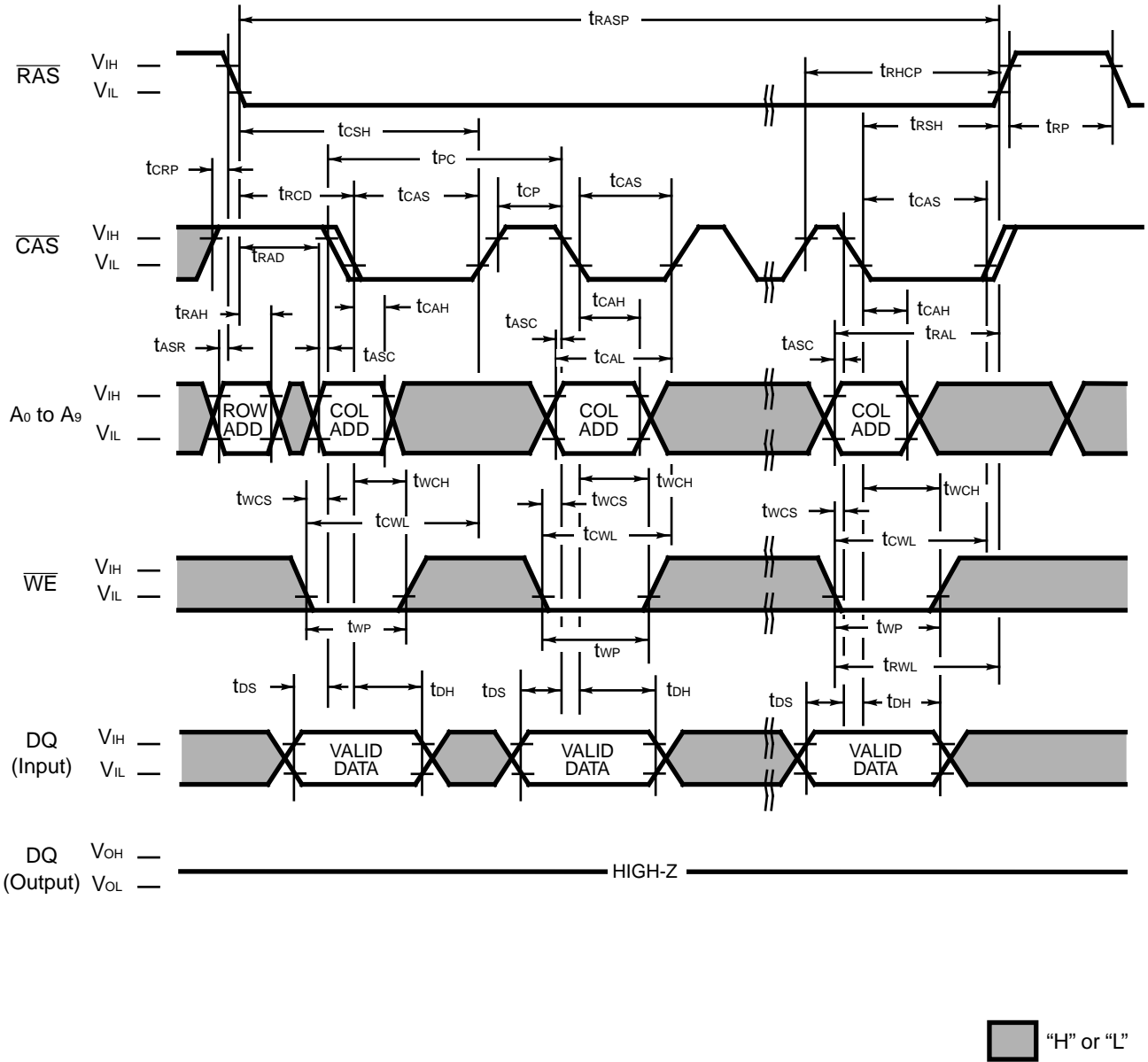


**DESCRIPTION**

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining  $\overline{RAS}$  at a Low level and  $\overline{WE}$  at a High level during all successive memory cycles in which the row address is latched. The access time is determined by  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ , or  $t_{OEA}$ , whichever one is the latest in occurring.

# MB81V4400C-60/MB81V4400C-70

Fig. 10 – FAST PAGE MODE WRITE CYCLE ( $\overline{OE}$ ="H" or "L")

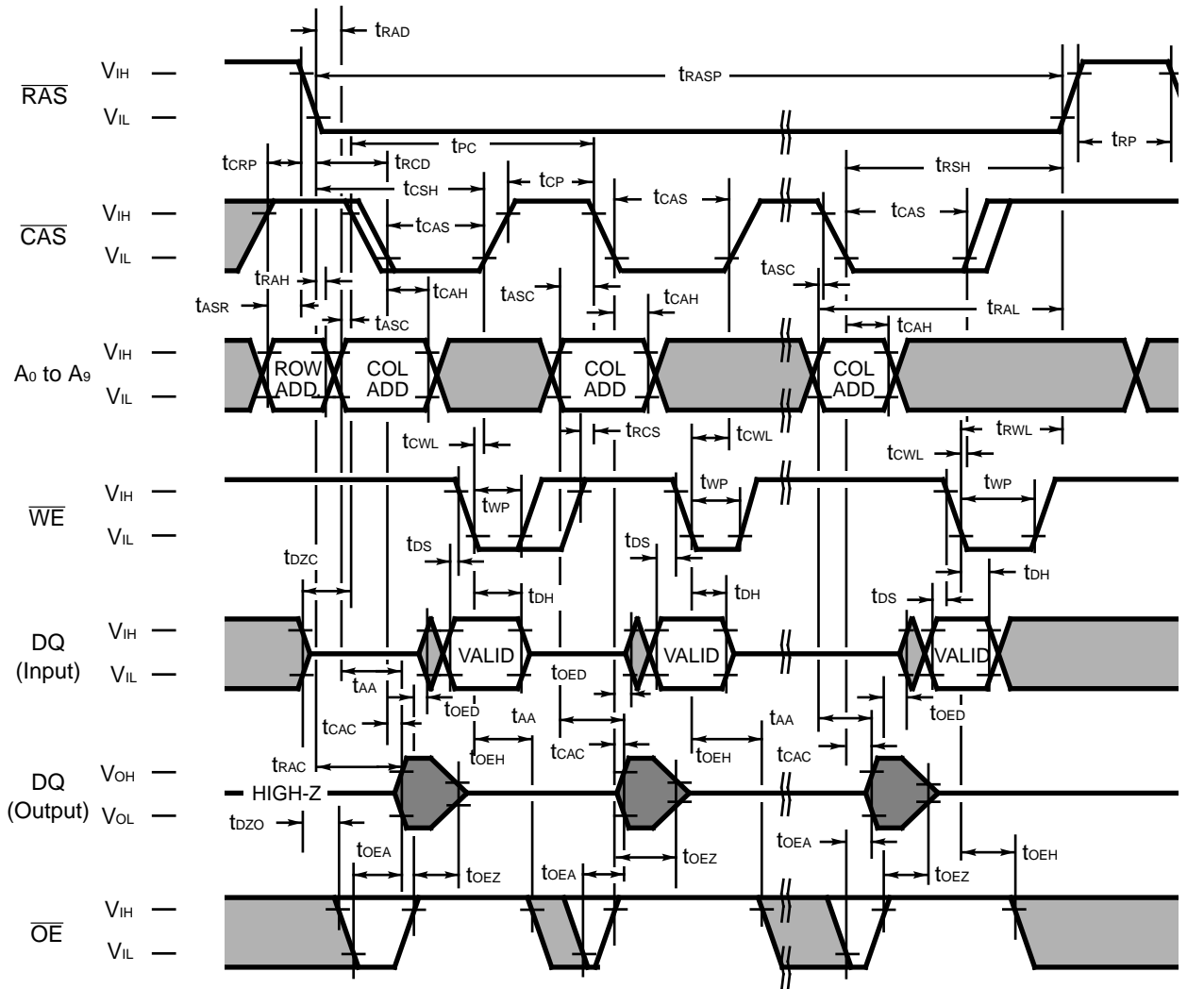


## DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of  $\overline{WE}$  and  $\overline{OE}$  are reversed. Data appearing on the  $DQ$  pins is latched on the falling edge of  $\overline{CAS}$  and written into memory. During the fast page mode write cycle, including the delayed ( $\overline{OE}$ ) write and read-modify-write cycles,  $t_{CWL}$  must be satisfied.



**Fig. 11 – FAST PAGE MODE  $\overline{OE}$  WRITE CYCLE**



"H" or "L"  
 Invalid Data

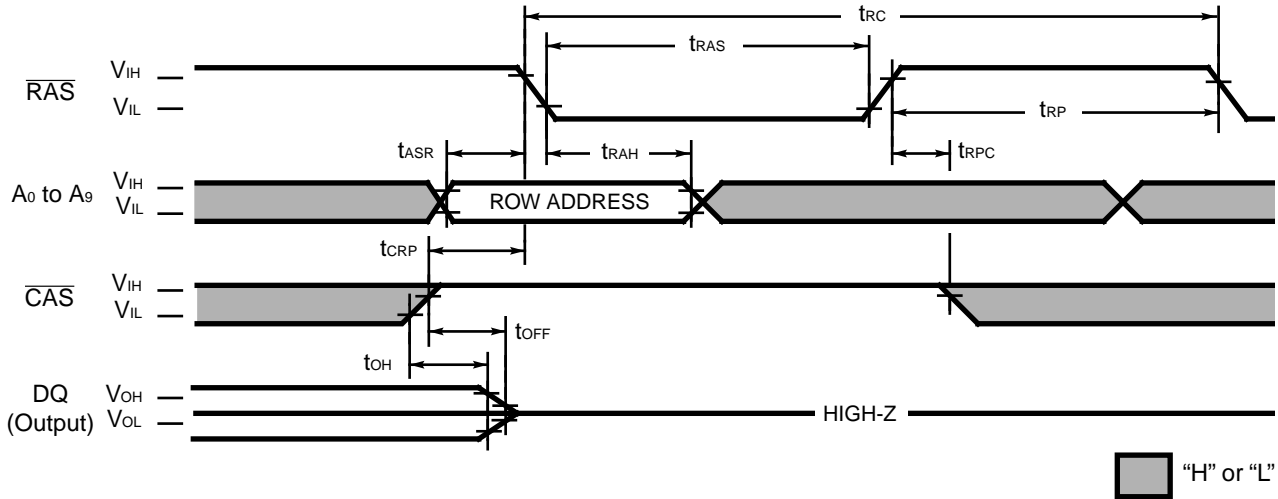
**DESCRIPTION**

The fast page mode  $\overline{OE}$  (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of  $\overline{WE}$  and  $\overline{OE}$ . Input data on the DQ pins are latched on the falling edge of  $\overline{WE}$  and written into memory. In the fast page mode delayed write cycle,  $\overline{OE}$  must be changed from Low to High before  $\overline{WE}$  goes Low ( $t_{OED} + t_r + t_{DS}$ ).



# MB81V4400C-60/MB81V4400C-70

Fig. 13 –  $\overline{\text{RAS}}$ -ONLY REFRESH ( $\overline{\text{WE}} = \overline{\text{OE}} = \text{“H” or “L”}$ )

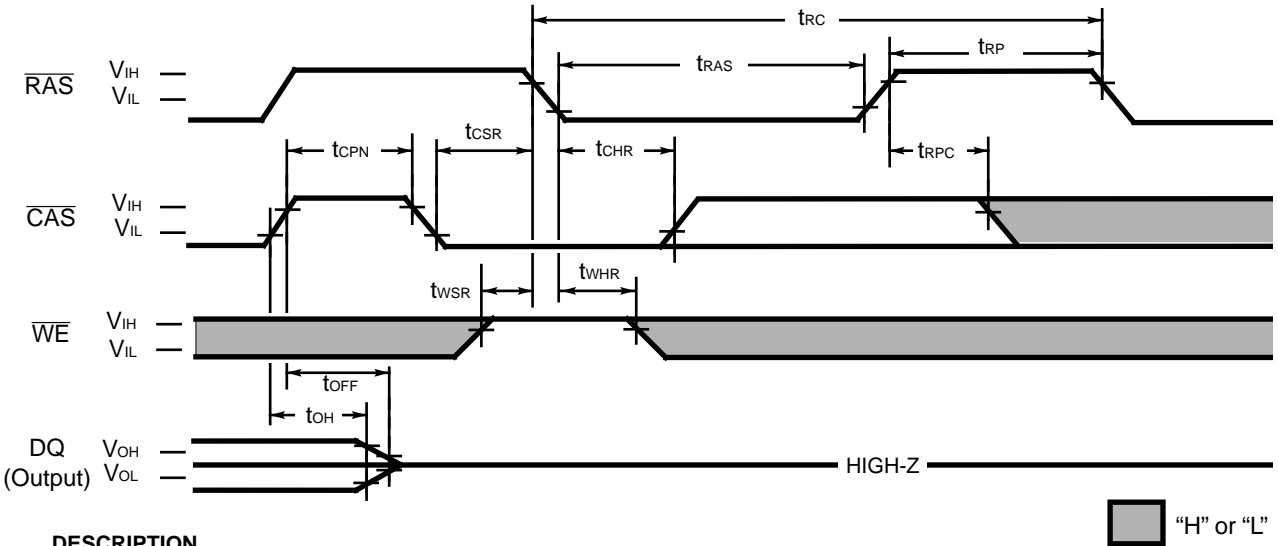


**DESCRIPTION**

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1024 row addresses every 16.4-milliseconds. Three refresh modes are available:  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh, and hidden refresh.

$\overline{\text{RAS}}$ -only refresh is performed by keeping  $\overline{\text{RAS}}$  Low and  $\overline{\text{CAS}}$  High throughout the cycle; the row address to be refreshed is latched on the falling edge of  $\overline{\text{RAS}}$ . During  $\overline{\text{RAS}}$ -only refresh, DQ pin is kept in a high-impedance state.

Fig. 14 –  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH ( $\text{A}_0$  to  $\text{A}_9 = \overline{\text{OE}} = \text{“H” or “L”}$ )



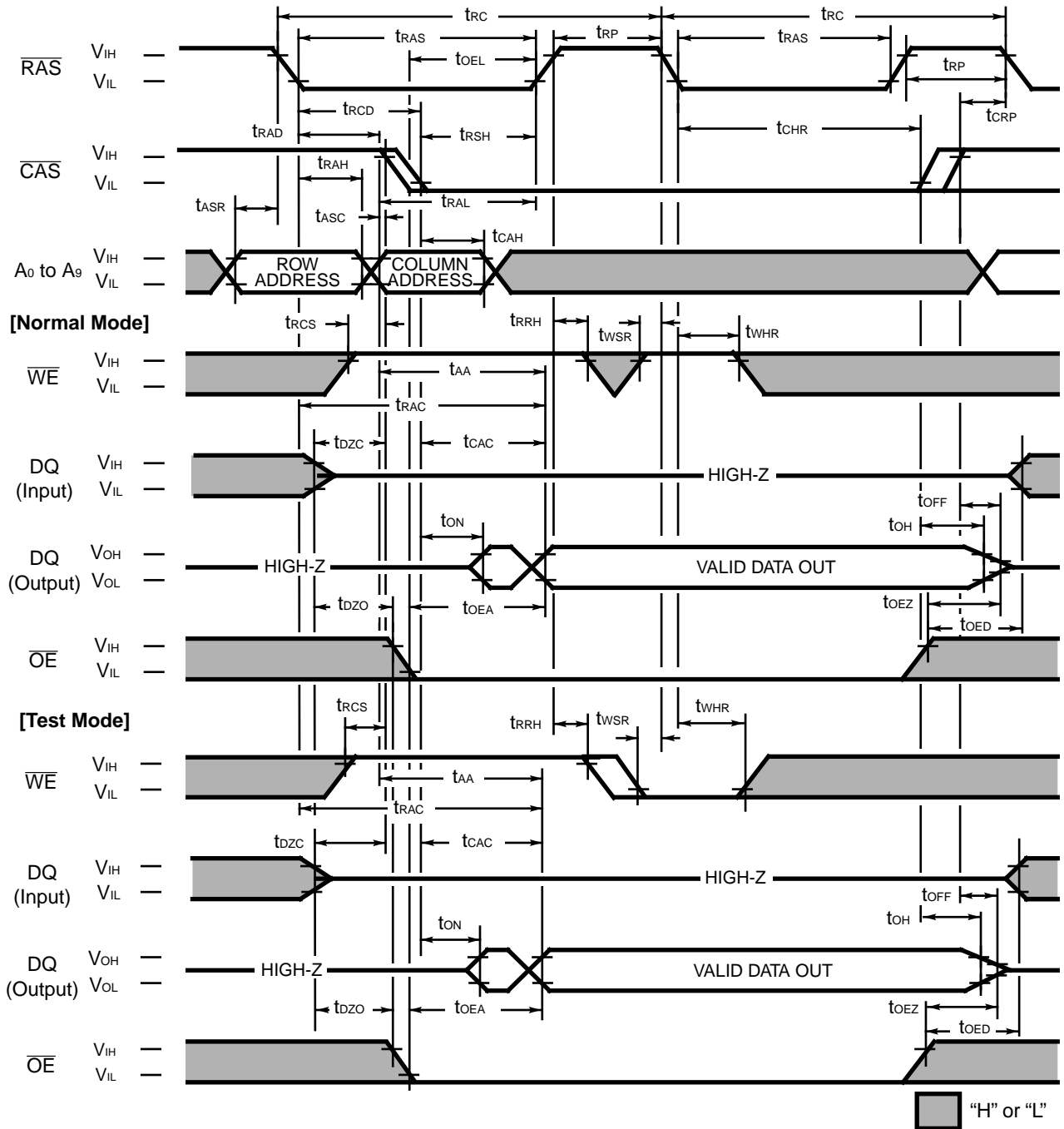
**DESCRIPTION**

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{\text{CAS}}$  is held Low for the specified setup time ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh operation.

$\overline{\text{WE}}$  must be held High for the specified set up time ( $t_{\text{WSR}}$ ) before  $\overline{\text{RAS}}$  goes low in order not to enter "test mode".

# MB81V4400C-60/MB81V4400C-70

Fig. 15 – HIDDEN REFRESH CYCLE

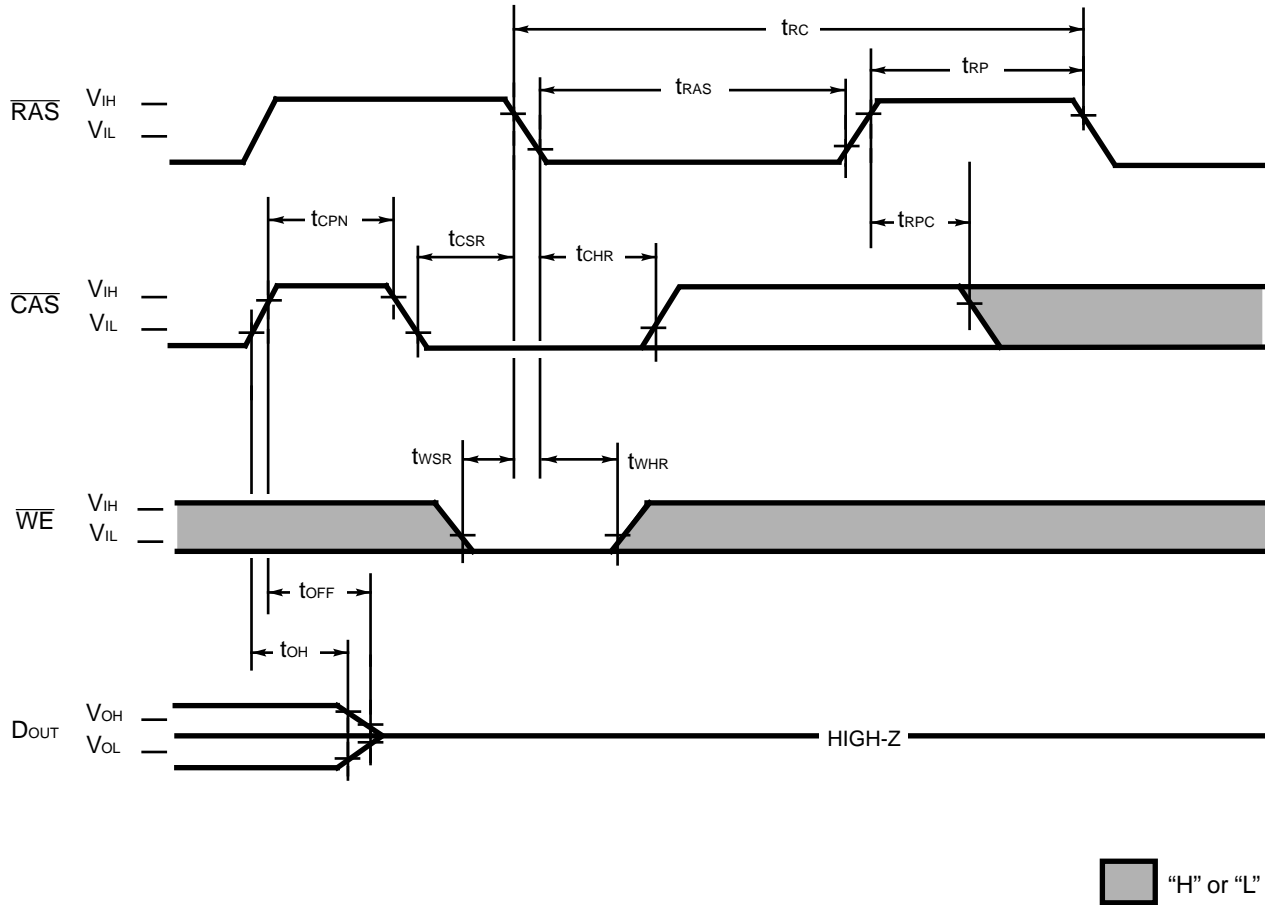


**DESCRIPTION**

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of  $\overline{\text{CAS}}$  and cycling  $\overline{\text{RAS}}$ . The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability.

$\overline{\text{WE}}$  must be held High for the specified set up time ( $t_{\text{WSR}}$ ) before  $\overline{\text{RAS}}$  goes Low in order not to enter "test mode".

Fig. 16 – TEST MODE SET CYCLE ( $A_0$  to  $A_9$ ,  $\overline{OE}$  = "H" or "L")



## DESCRIPTION

Test Mode ;

The purpose of this test mode is to reduce device test time to half of that required to test the device conventionally. The test mode function is entered by performing a  $\overline{WE}$  and  $\overline{CAS}$ -before- $\overline{RAS}$  (WCBR) refresh for the entry cycle. In the test mode, read and write operations are executed in units of eight bits which are selected by the address combination of  $CA_0$ . In the write mode, data is written into eight cells simultaneously. But the data must be input from all DQ pins. In the read mode, the data of eight cells at the selected addresses are read out from DQ and checked in the following manner

- When the eight bits are all "L" or all "H", a "H" level is output.
- When the eight bits show a combination of "L" and "H", a "L" level is output.

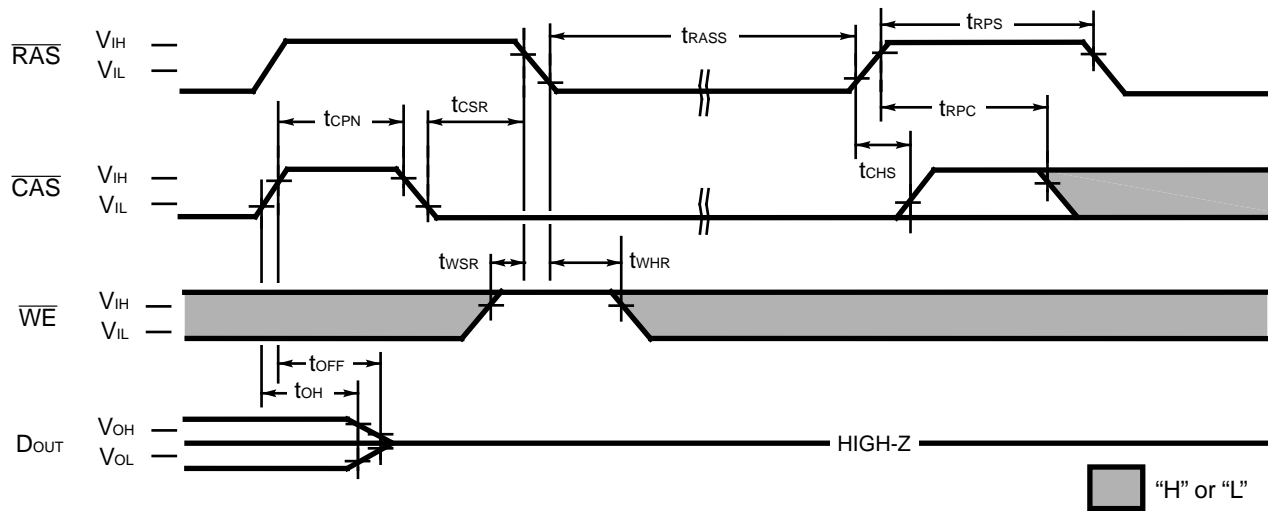
The test mode function is exited by performing a  $\overline{RAS}$ -only refresh or a  $\overline{CAS}$ -before- $\overline{RAS}$  refresh for the exit cycle. In test mode operation, the following parameters are delayed approximately 5ns from the specified value in the data sheet.

$t_{RC}$ ,  $t_{RWC}$ ,  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{RAS}$ ,  $t_{CSH}$ ,  $t_{RAL}$ ,  $t_{RWD}$ ,  $t_{AWD}$ ,  $t_{PC}$ ,  $t_{PRWC}$ ,  $t_{CPA}$ ,  $t_{RHC}$ ,  $t_{CPWD}$



# MB81V4400C-60/MB81V4400C-70

Fig. 18 – SELF REFRESH CYCLE ( $A_0-A_9 = \overline{OE} = \text{“H” or “L”}$ )



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4400C-60		MB81V4400C-70		Unit
			Min.	Max.	Min.	Max.	
100	RAS Pulse Width	$t_{RASS}$	100	—	100	—	$\mu\text{s}$
101	RAS Precharge Time	$t_{RPS}$	110	—	125	—	ns
102	CAS Hold Time	$t_{CHS}$	-50	—	-50	—	ns

Note. Assumes self refresh cycle only

## DESCRIPTION

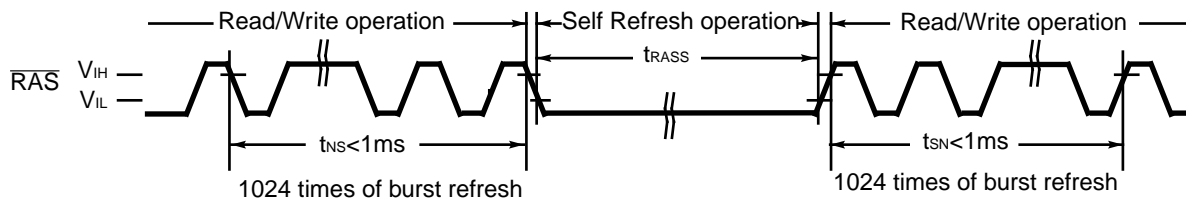
The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter. If CAS goes to "L" before RAS goes to "L" (CBR) and the condition of CAS "L" and RAS "L" is kept for term of  $t_{RASS}$  (more than 100  $\mu\text{s}$ ), the device can be entered the self refresh cycle. And after that, refresh operation is automatically executed per fixed interval using internal refresh address counter during "RAS=L" and "CAS=L".

And exit from self refresh cycle is performed by toggling of RAS and CAS to "H" with specifying  $t_{CHS}$  min.

Restriction for Self refresh operation ;

For self refresh operation, the notice below must be considered.

- 1) In the case that distribute CBR refresh are operated in read/write cycles  
Self refresh cycles can be executed without special rule if 1024 cycles of distribute CBR refresh are executed within  $t_{REF}$  max..
- 2) In the case that burst CBR refresh or RAS-only refresh are operated in read/write cycles  
1024 times of burst CBR refresh or 1024 times of burst RAS-only refresh must be executed before and after Self refresh cycles.

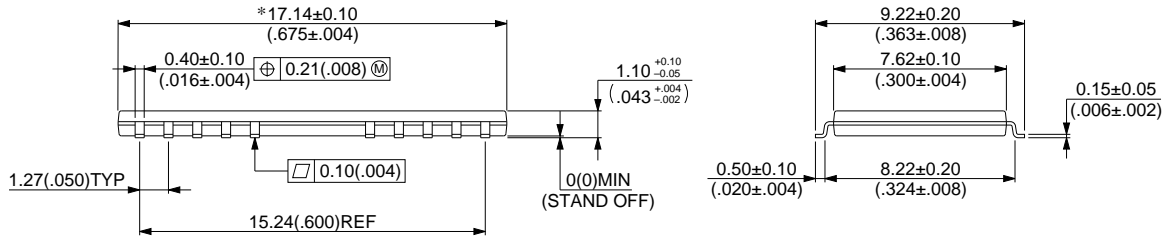
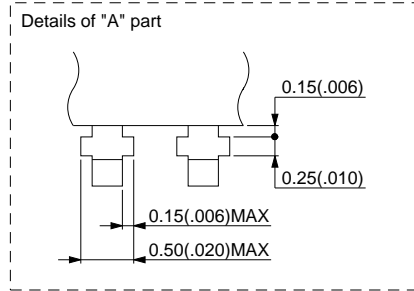
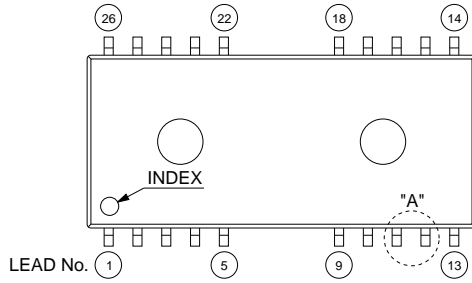


# MB81V4400C-60/MB81V4400C-70

## ■ PACKAGE DIMENSIONS

(Suffix : -PFTN)

26 pin, Plastic TSOP(II)  
(FPT-26P-M01)



Dimensions in mm(inches).

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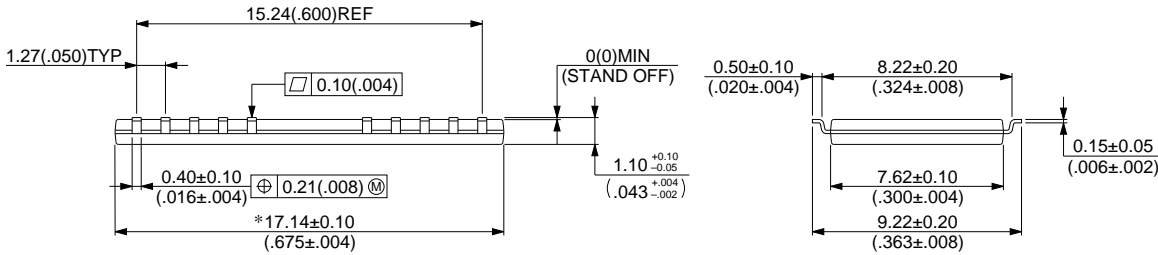
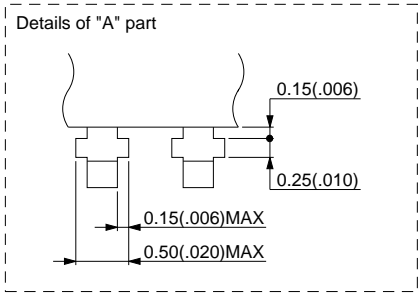
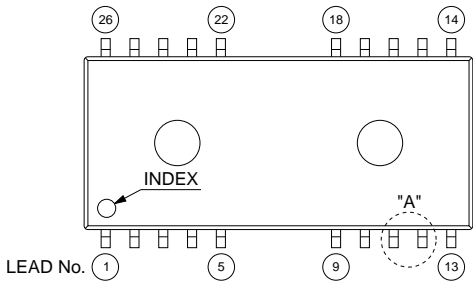


# MB81V4400C-60/MB81V4400C-70

## ■ PACKAGE DIMENSIONS (Continued)

(Suffix : -PFTR)

26 pin, Plastic TSOP(II)  
(FPT-26P-M02)



Dimensions in mm(inches).

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