FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-29118-2E

Spread Spectrum Clock Generator

MB88153

■ DESCRIPTION

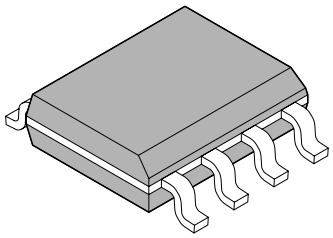
MB88153 is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. It corresponds to both of the center spread which modulates input frequency as Middle Centered and down spread which modulates so as not to exceed input frequency.

■ FEATURE

- Power down pin : 600 µA (Max) consumption current at power down
- Input frequency : 16.6 MHz to 134 MHz
- Output frequency : 16.6 MHz to 134 MHz (One-fold input frequency)
- Modulation rate can select from ± 0.5%, ± 1.5% – 1.0% or – 3.0%. (For center spread / down spread.)
- Modulation clock output Duty : 40% to 60%
- Modulation clock Cycle-Cycle Jitter : Less than 100 ps
- Low current consumption by CMOS process : 4.0 mA (24 MHz : Typ-sample, no load)
- Power supply voltage : 3.3 V ± 0.3 V
- Operating temperature : – 40 °C to +85 °C
- Package : SOP 8-pin

■ PACKAGE

8-pin plastic SOP



(FPT-8P-M02)

FUJITSU

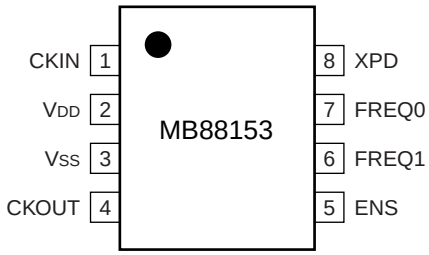
■ PRODUCT LINEUP

MB88153 has four kinds of modulation rate and modulation type (center/down spread).

Product	Modulation rate	Modulation type
MB88153-100	–1.0%	Down
MB88153-101	–3.0%	
MB88153-110	±0.5%	Center
MB88153-111	±1.5%	

■ PIN ASSIGNMENT

TOP VIEW

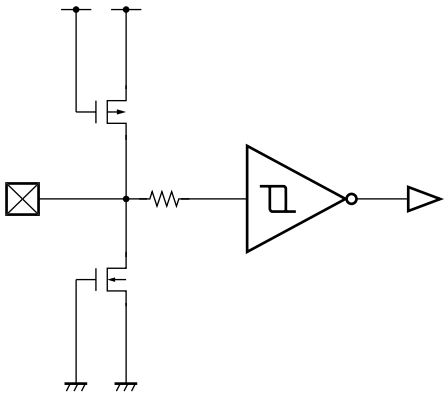
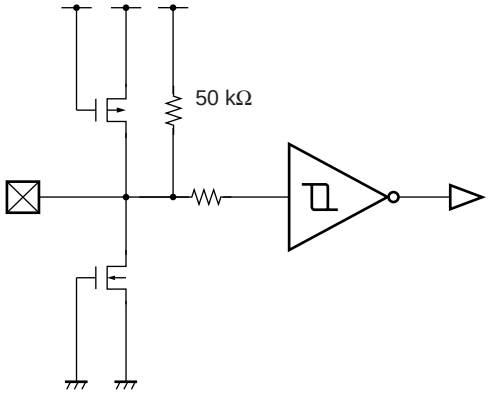
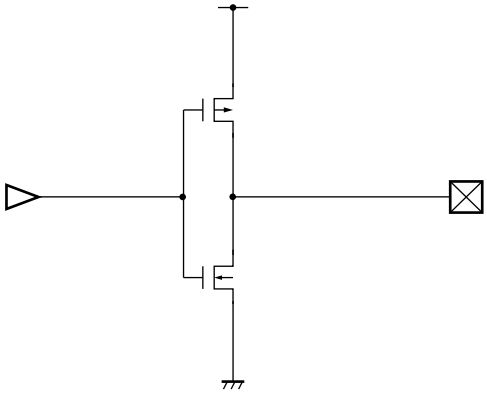


FPT-8P-M02

■ PIN DESCRIPTION

Pin name	I/O	Pin no.	Description
CKIN	I	1	Clock input pin
V_{DD}	—	2	Power supply voltage pin
V_{SS}	—	3	GND pin
CKOUT	O	4	Modulated clock output pin “L” output at power down
ENS	I	5	Modulation enable setting pin
FREQ1	I	6	Frequency setting pin
FREQ0	I	7	Frequency setting pin (with pull-up resistor)
XPD	I	8	Power down pin (with pull-up resistor) Power down at “L” input

■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
CKIN, ENS, FREQ1		• CMOS hysteresis input
FREQ0, XPD		• CMOS hysteresis input with pull-up resistor 50 kΩ (typ)
CKOUT		• CMOS output • “L” output at power down

■ HANDLING DEVICES

Preventing Latchup

A latchup can occur if, on this device, (a) a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input or output pin or (b) a voltage higher than the rating is applied between V_{DD} and V_{SS}. The latchup, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

Unused output pin should be opened.

Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between V_{SS} and V_{DD} near the device, as a bypass capacitor.

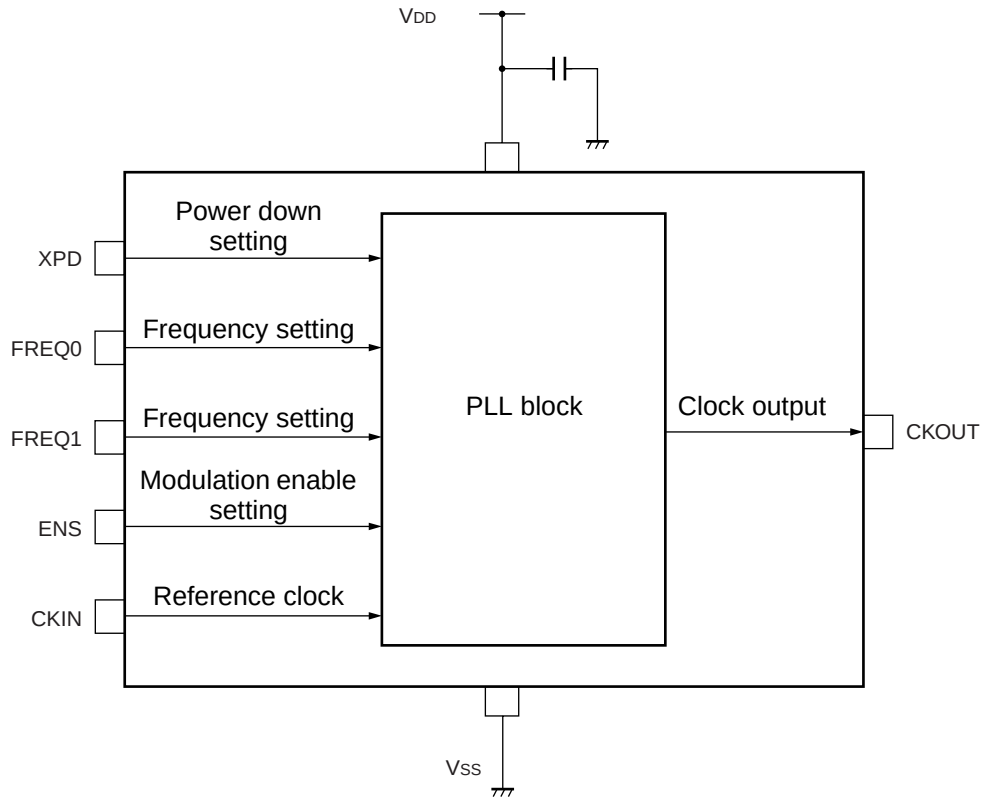
Clock I/O circuit

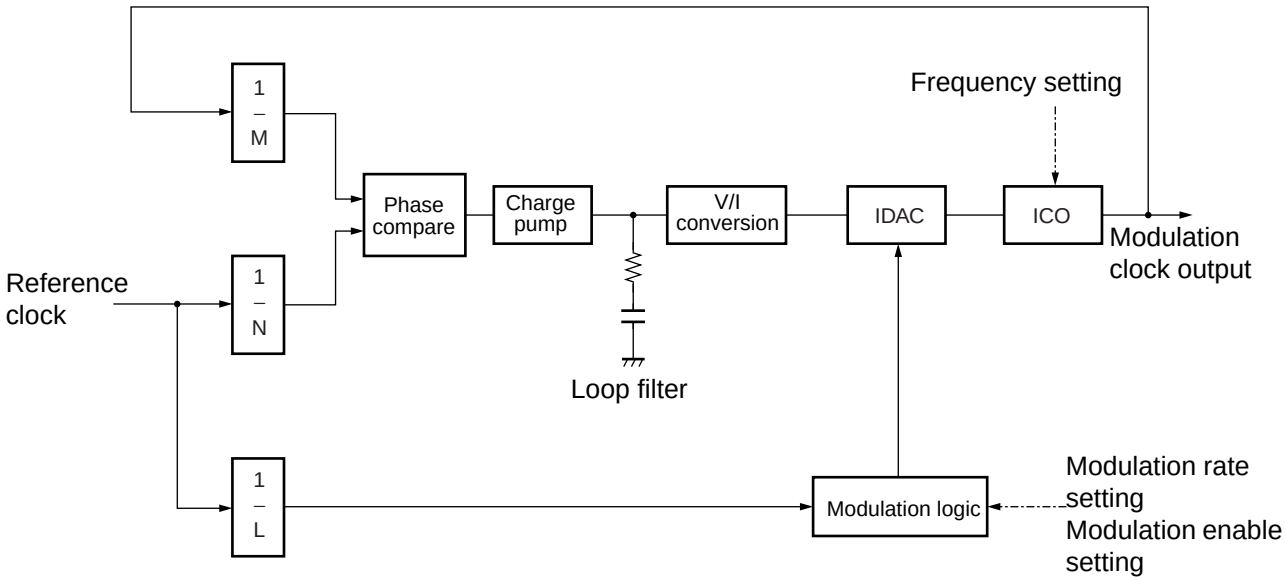
Noise near the CKIN pin may cause the device to malfunction. Design the printed circuit board so that the wiring for the clock input does not intersect any other wiring.

Please pay attention so that an overshoot and an undershoot do not occur to an input clock of CKIN pin.

Design the printed circuit board that surrounds the CKIN and CKOUT pins with ground.

■ BLOCK DIAGRAM





MB88153 PLL block

A glitchless IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

■ PIN SETTING

When changing the pin setting, the stabilization wait time for the modulation clock required. The stabilization wait time for the modulation clock takes the maximum value of Lock-Up time in "■ ELECTRICAL CHARACTERISTICS • AC characteristics".

ENS modulation enable setting

ENS	Modulation
L	No modulation
H	Modulation

Note : Spectrum does not spread when "L" is set to ENS. The clock with low jitter can be obtained.

FREQ0, FREQ1 frequency setting

FREQ0	FREQ1	Input frequency range
L	L	16.6 MHz to 40 MHz
L	H	66 MHz to 134 MHz
H	L	33 MHz to 67 MHz
H	H	40 MHz to 80 MHz

Note : It is set according to the frequency of the clock input to the device. Set FREQ0 pin to "H" for the pin opened because FREQ0 pin has pull-up resistor.

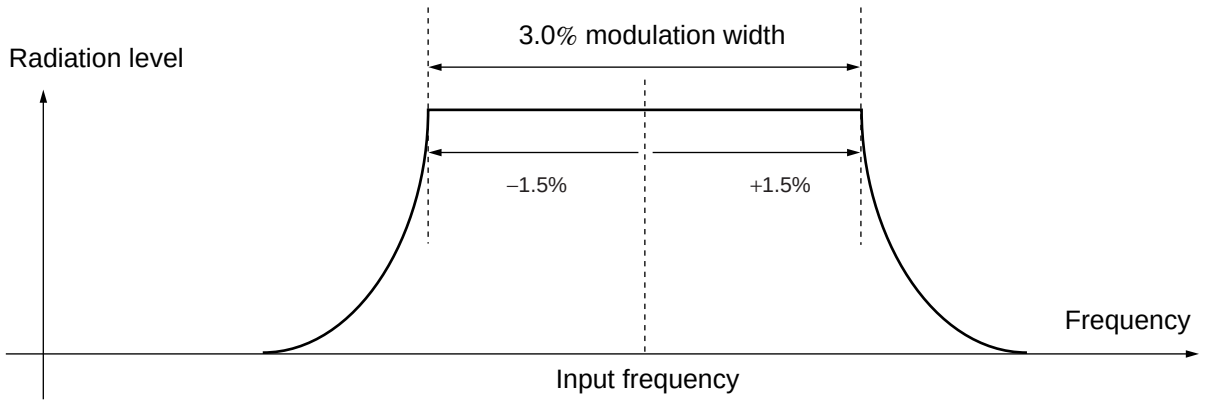
XPD power down setting

XPD	Power down
L	Power down
H	Normal operation

Note : When "L" is set to XPD pin, the power down operation is implemented and "L" is output to CKOUT pin. When "H" is input to XPD pin or XPD pin is opened, normal operation is implemented because the XPD pin has pull-up resistor.

• Center spread

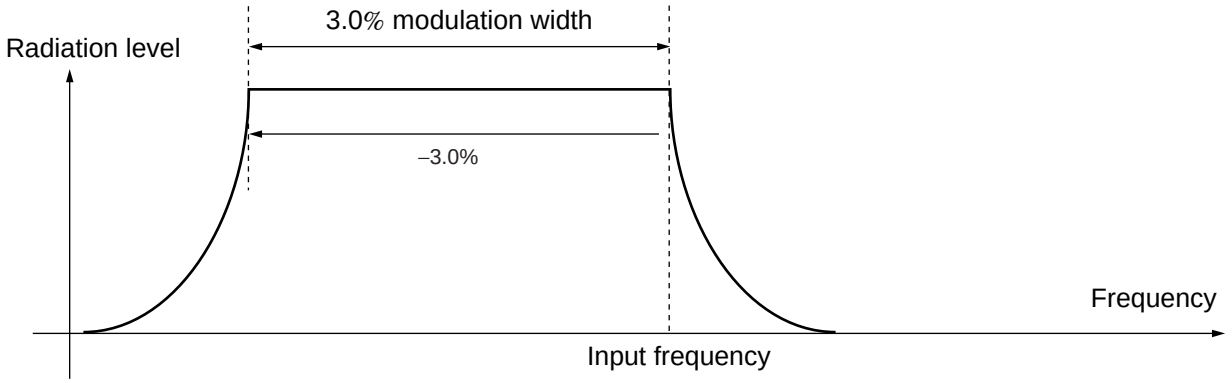
Spectrum is spread (modulated) by centering on the input frequency.



Center spread example of ± 1.5% modulation rate

• Down spread

Spectrum is spread (modulated) below the input frequency.



Down spread example of – 3.0% modulation rate

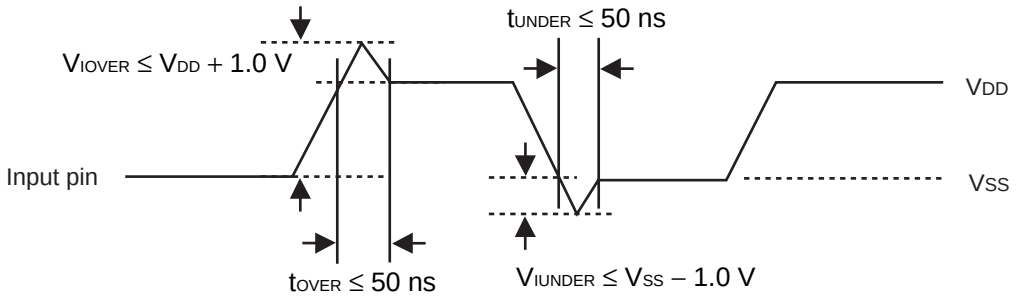
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	– 0.5	+ 4.0	V
Input voltage*	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	– 55	+ 125	°C
Operation junction temperature	T_J	– 40	+ 125	°C
Output current	I_O	– 14	+ 14	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 (t_{OVER} ≤ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS} – 1.0 (t_{UNDER} ≤ 50 ns)	—	V

* : The parameter is based on V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0.0 V)

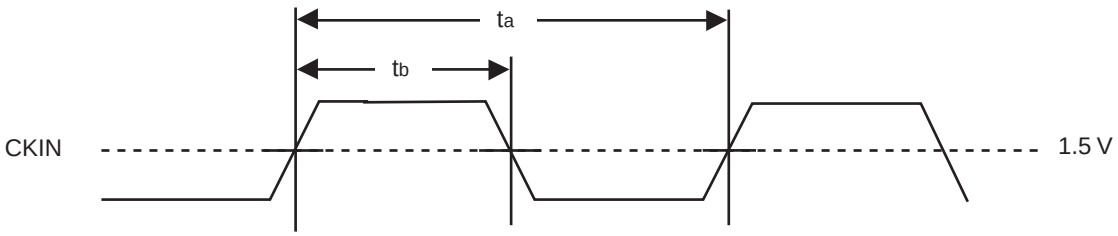
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	—	3.0	3.3	3.6	V
"H" level input voltage	V_{IH}	CKIN, ENS, FREQ0, FREQ1, XPD	—	$V_{DD} \times 0.80$	—	$V_{DD} + 0.3$	V
"L" level input voltage	V_{IL}	CKIN, ENS, FREQ0, FREQ1, XPD	—	V_{SS}	—	$V_{DD} \times 0.20$	V
Input clock duty cycle	t_{DCI}	CKIN	16.6 MHz to 134 MHz	40	50	60	%
Operating temperature	Ta	—	—	− 40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b/t_a$)



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

(Ta = – 40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Output voltage	V_{OH}	CKOUT	"H" level output I_{OH} = – 4 mA	V_{DD} – 0.5	—	V_{DD}	V
	V_{OL}	CKOUT	"L" level output I_{OL} = 4 mA	V_{SS}	—	0.4	V
Output impedance	Z_O	CKOUT	16.6 MHz to 134 MHz	—	45	—	Ω
Input capacitance	C_{IN}	CKIN, ENS, FREQ0, FREQ1, XPD	Ta = + 25 °C, V_{DD} = V_I = 0.0 V, f = 1 MHz	—	—	16	pF
Load capacitance	C_L	CKOUT	16.6 MHz to 67 MHz	—	—	15	pF
			67 MHz to 100 MHz	—	—	10	
			100 MHz to 134 MHz	—	—	7	
Input Pull-up resistance	R_{PU}	FREQ0, XPD	V_{IL} = 0.0 V	25	50	200	kΩ
Power supply current	I_{CC}	V_{DD}	No load capacitance at 24 MHz output	—	4.0	6.0	mA
Power down current	Ipd	V_{DD}	Input clock stopping	—	—	600	μA

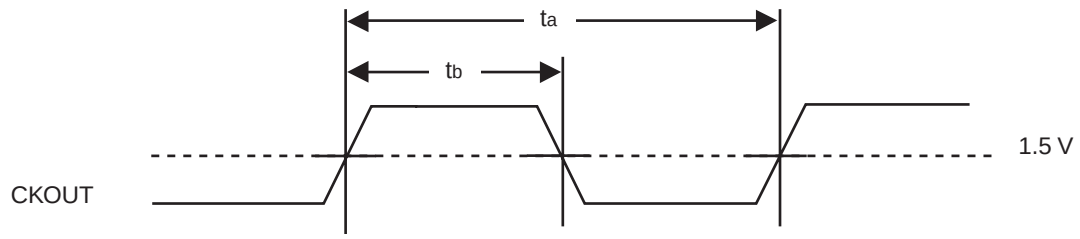
• AC Characteristics

(Ta = – 40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

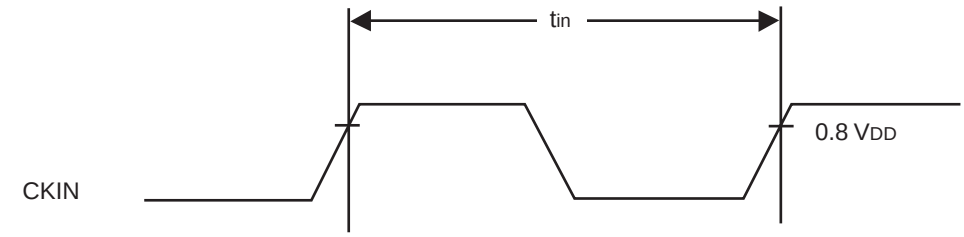
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Input frequency	f_{in}	CKIN	—	16.6	—	134	MHz
Output frequency	f_{OUT}	CKOUT	—	16.6	—	134	MHz
Output slew rate	SR	CKOUT	Load capacitance 15 pF 0.4 V to 2.4 V	0.4	—	4.0	V/ns
Output clock duty cycle	t_{DCC}	CKOUT	1.5 V	40	—	60	%
Modulation frequency	f_{MOD}	CKOUT	—	—	12.5	—	kHz
Lock-up time	t_{LK}	CKOUT	—	—	2	5	ms
Cycle-cycle jitter	t_{JC}	CKOUT	No load capacitance, Ta = + 25 °C, V_{DD} = 3.3 V, Standard deviation σ	—	—	100	ps

Note : The modulation clock stabilization wait time is required after the power is turned on, the IC recovers from power saving, or after FREQ (frequency range) or ENS (modulation ON/OFF) setting is changed. For the modulation clock stabilization wait time, assign the maximum value for lock-up time.

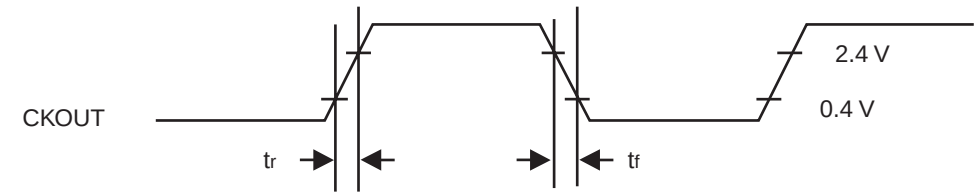
■ OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b/t_a$)



■ INPUT FREQUENCY ($f_{in} = 1/t_{in}$)



■ OUTPUT SLEW RATE (SR)



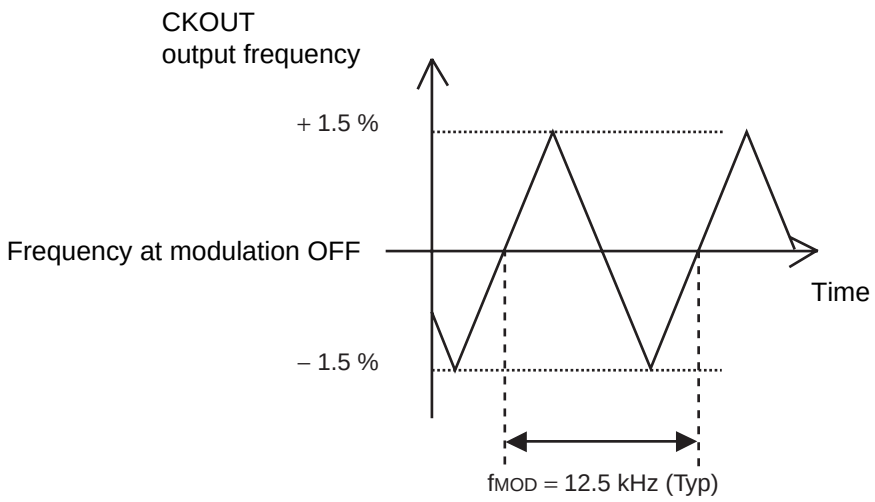
Note : SR = (2.4–0.4) /t_r, SR = (2.4–0.4) /t_f

■ CYCLE-CYCLE JITTER

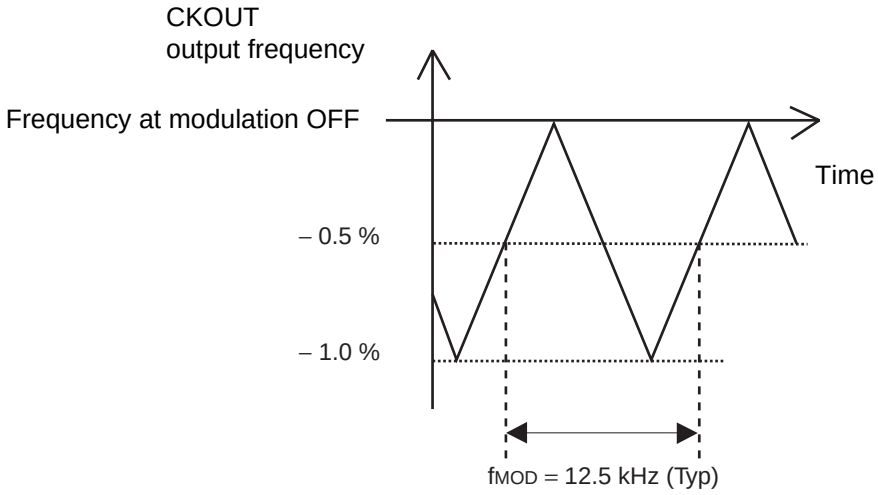
Note : Cycle-cycle jitter is defined the difference between a certain cycle and immediately after (or, immediately before) .

■ MODULATION WAVEFORM

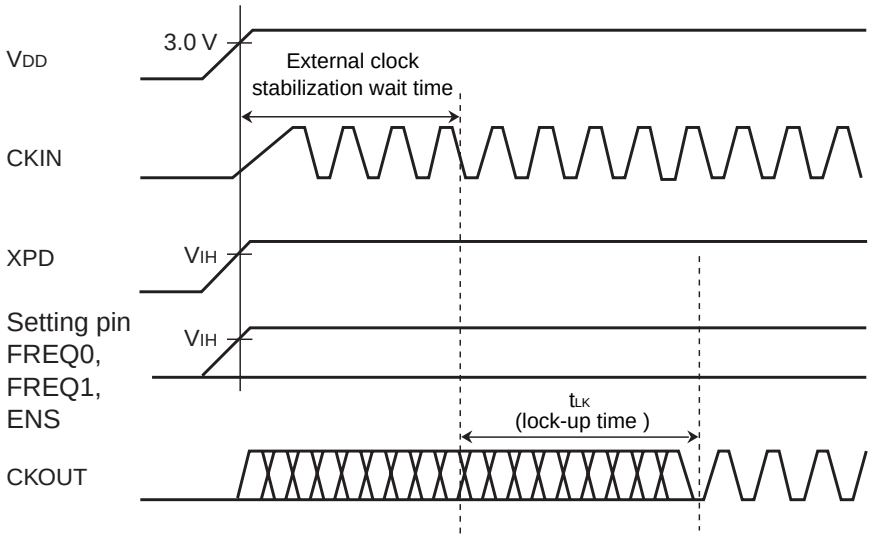
- ±1.5% modulation rate, Example of center spread



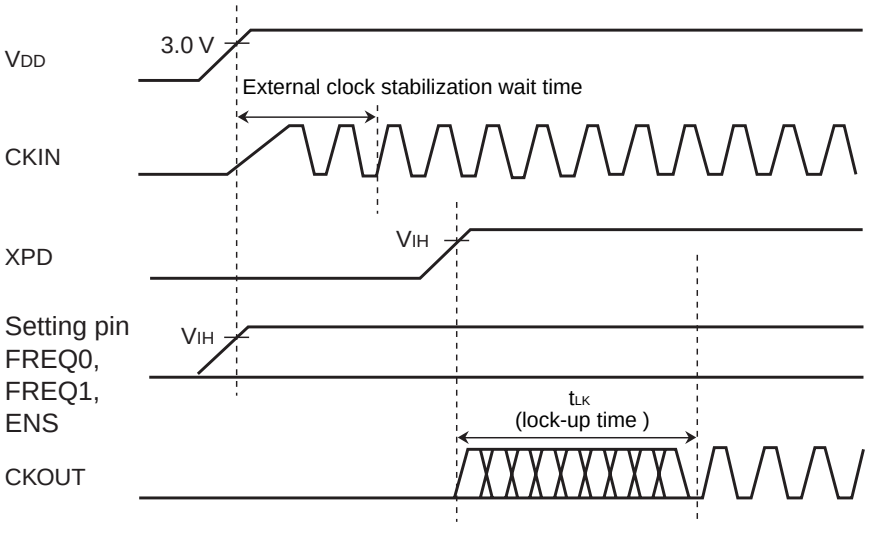
- –1.0% modulation rate, Example of down spread



■ LOCK-UP TIME

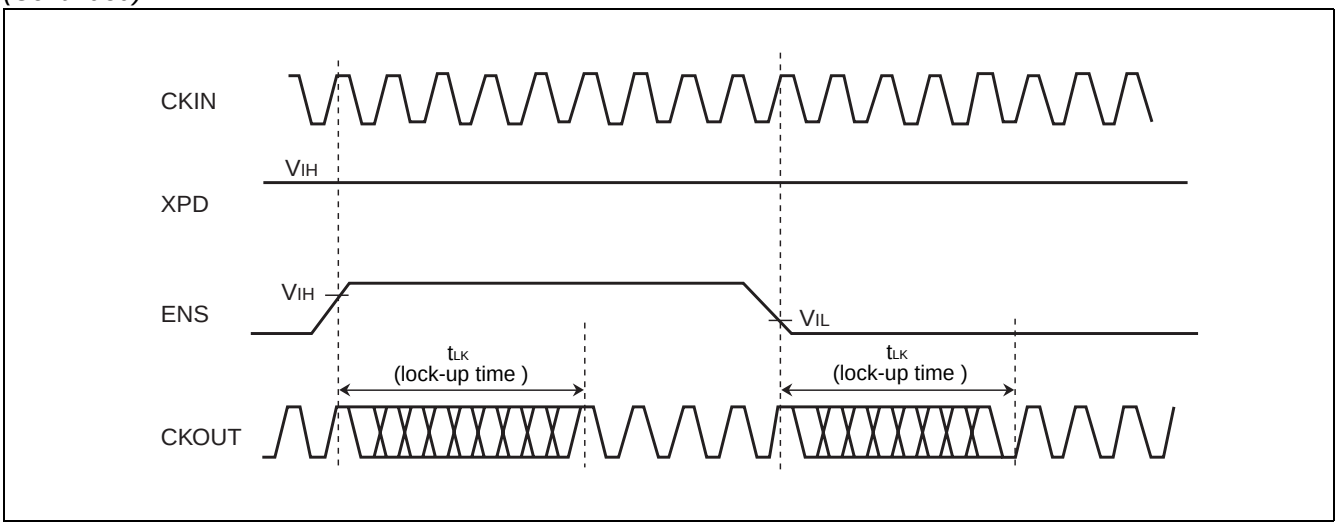


If the XPD pin is fixed at the “H” level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to CKIN pin) + (the lock-up time “t_{LK}”). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.



When XPD pin controls the power-down, stable clock is output from CKOUT pin after becoming XPD pin = “H” level (in the maximum after lock-Up time (t_{LK})).

(Continued)

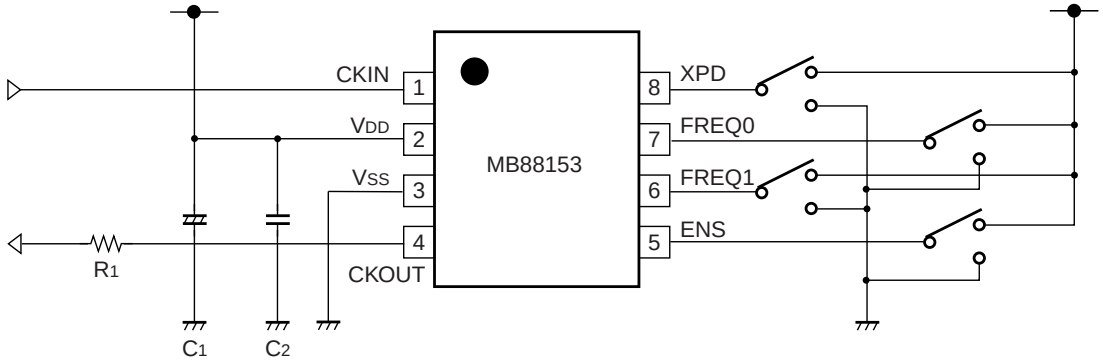


When ENS pin is controlled for enable modulation, it is necessary for the stably clock output from CKOUT pin to wait lock-up time (t_{LK}) .

Note : In the following cases, it is necessary for the stably clock output from CKOUT pin, to wait lock-up time (t_{LK}) .
- After releasing power-down
- When you change other terminal settings

Output frequency, output clock duty cycle, modulation frequency, and cycle-cycle jitter are not guaranteed until the output clock is stable. It is recommended to take procedure to release of reset after. lock-up time (t_{LK}) on the device using the modulation clock or etc.

■ INTERCONNECTION CIRCUIT EXAMPLE



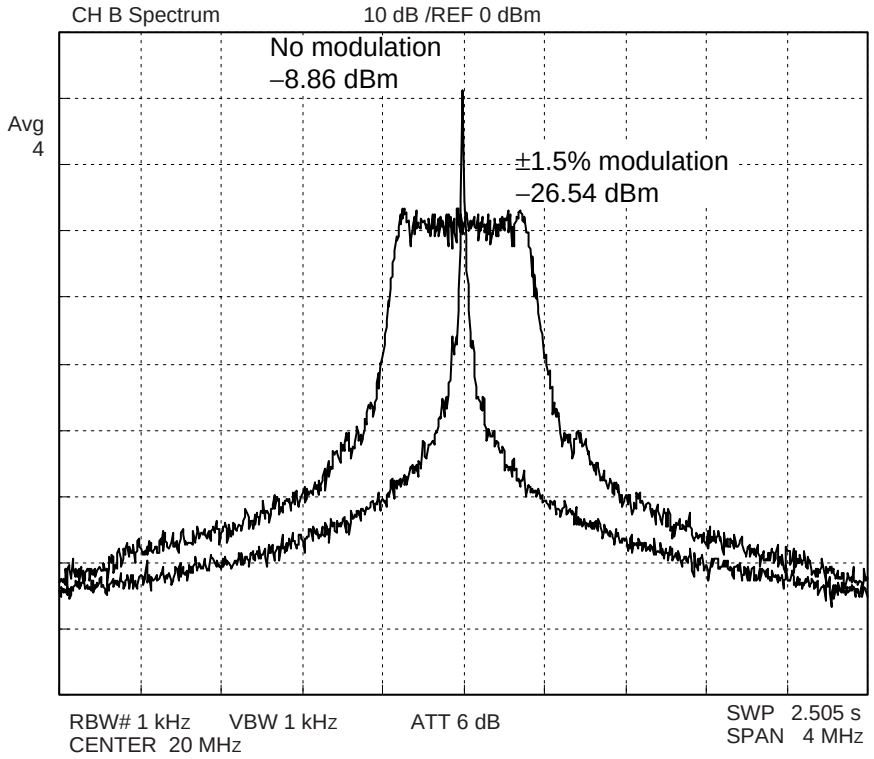
C_1 : Capacitor of 10 μF or higher

C_2 : Capacitor of approximately 0.01 μF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)

R_1 : Impedance matching resistor for a circuit on a board

■ SPECTRUM EXAMPLE CHARACTERISTICS

The condition of the examples of the characteristic is shown as follows: Input frequency = 20 MHz (Output frequency = 20 MHz), use for MB88153-111.
Power-supply voltage = 3.3 V, None load capacity. Modulation rate = ± 1.5% (center spread).
Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with RBW = 1 kHz (ATT use for −6 dB) .



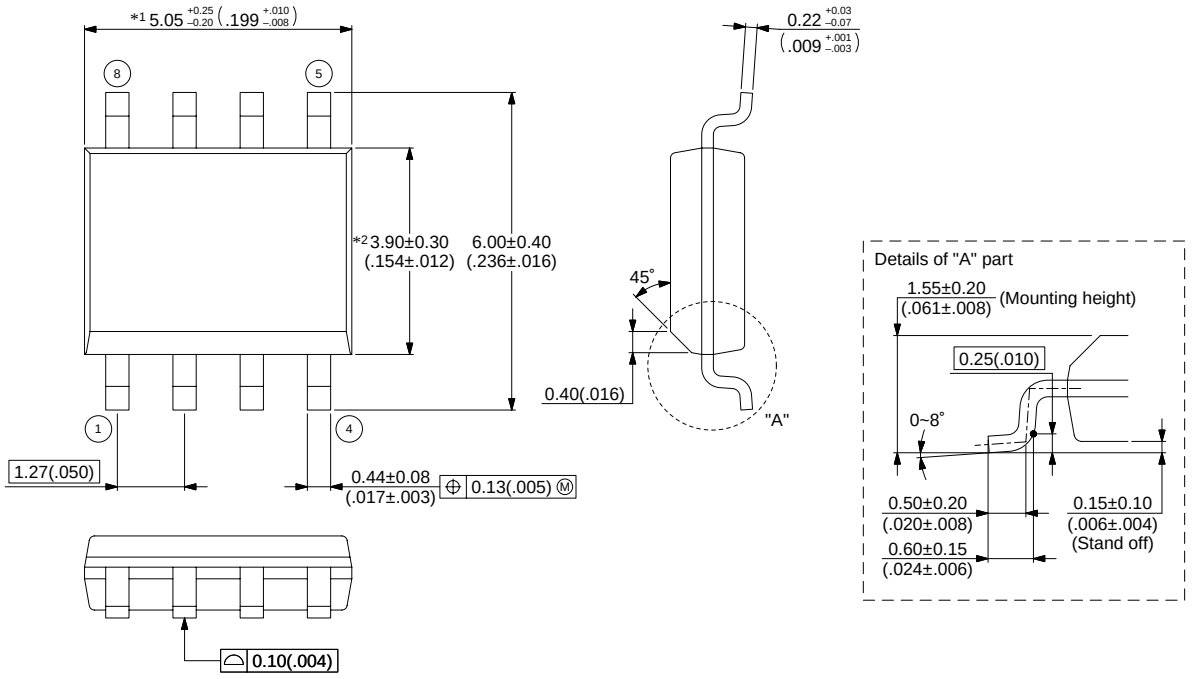
■ ORDERING INFORMATION

Part number	modulation rate	modulation type	Package	Remarks
MB88153PNF-G-100-JNE1	−1.0%	Down	8-pin plastic SOP (FPT-8P-M02)	
MB88153PNF-G-101-JNE1	−3.0%	Down		
MB88153PNF-G-110-JNE1	±0.5%	Center		
MB88153PNF-G-111-JNE1	±1.5%	Center		
MB88153PNF-G-100-JN-EFE1	−1.0%	Down	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (EF type)
MB88153PNF-G-101-JN-EFE1	−3.0%	Down		
MB88153PNF-G-110-JN-EFE1	±0.5%	Center		
MB88153PNF-G-111-JN-EFE1	±1.5%	Center		
MB88153PNF-G-100-JN-ERE1	−1.0%	Down	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (ER type)
MB88153PNF-G-101-JN-ERE1	−3.0%	Down		
MB88153PNF-G-110-JN-ERE1	±0.5%	Center		
MB88153PNF-G-111-JN-ERE1	±1.5%	Center		

■ PACKAGE DIMENSION

8-pin plastic SOP
(FPT-8P-M02)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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