SONY

CXP5010

CMOS 4-bit 1 Chip Microcomputer

Piggyback type

Description

CXP5010 is a CMOS 4-bit 1 chip microcomputer of piggyback/evaluator combined type which has been developed for functional evaluation of the CXP5014/5016.

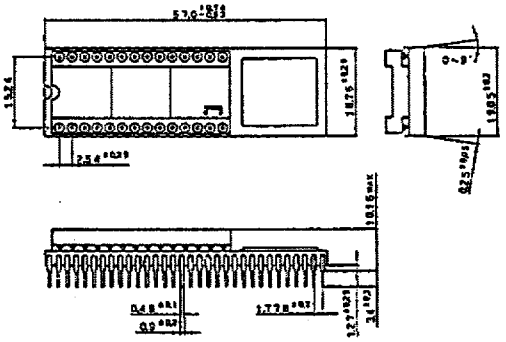
Features

- It has compatibility of the instructions, functions, and pins with those of the CXP5014/5016.
- Instruction cycle
  3.8 µs/4.19MHz (CXP5010)
  1.9 µs/4.19MHz (CXP5010H)
- ROM capacity Maximum 8K bytes
  (EPROM 27C64 LCC/DIP)
- RAM capacity 288 × 4 bits
- 32 general purpose I/O ports
- Fluorescent display tube controller/driver
  (Ables to display maximum 144 segments)
  — 1 to 16 digits dynamic scan display
  — Page mode/variable mode
  — Dimmer function
  — High tension proof output (40V)
  — Selection possible for incorporating pull-down resistance (mask option)
- 14-bit PWM output for D/A conversion
- Remote control receiving circuit
- 2 external interruption input pins
  (Except for QFP)
- 8-bit/4-bit variable serial I/O
- 8-bit timer, 8-bit timer/event counter and 18-bit time base timer, independently controlled
- Arithmetic and logical operations possible between the entire RAM area, I/O area and the accumulator by means of memory mapped I/O
- Reference to the entire ROM area is possible with the table look-up instruction
- 2 kinds of power down modes of sleep and stop
- Power on reset circuit (mask option)
- 64-pin ceramic SDIP/QFP

Package Outline

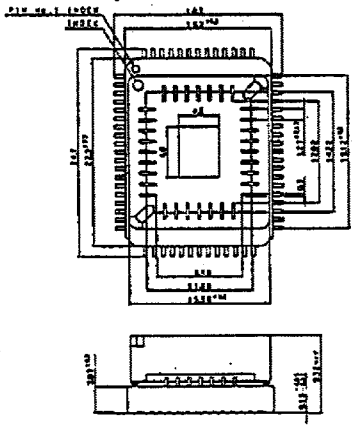
Unit : mm

64 pin SDIP (Ceramic)



PSDIP-64C-021

64 pin QFP (Ceramic)



PQFP-64C-L01

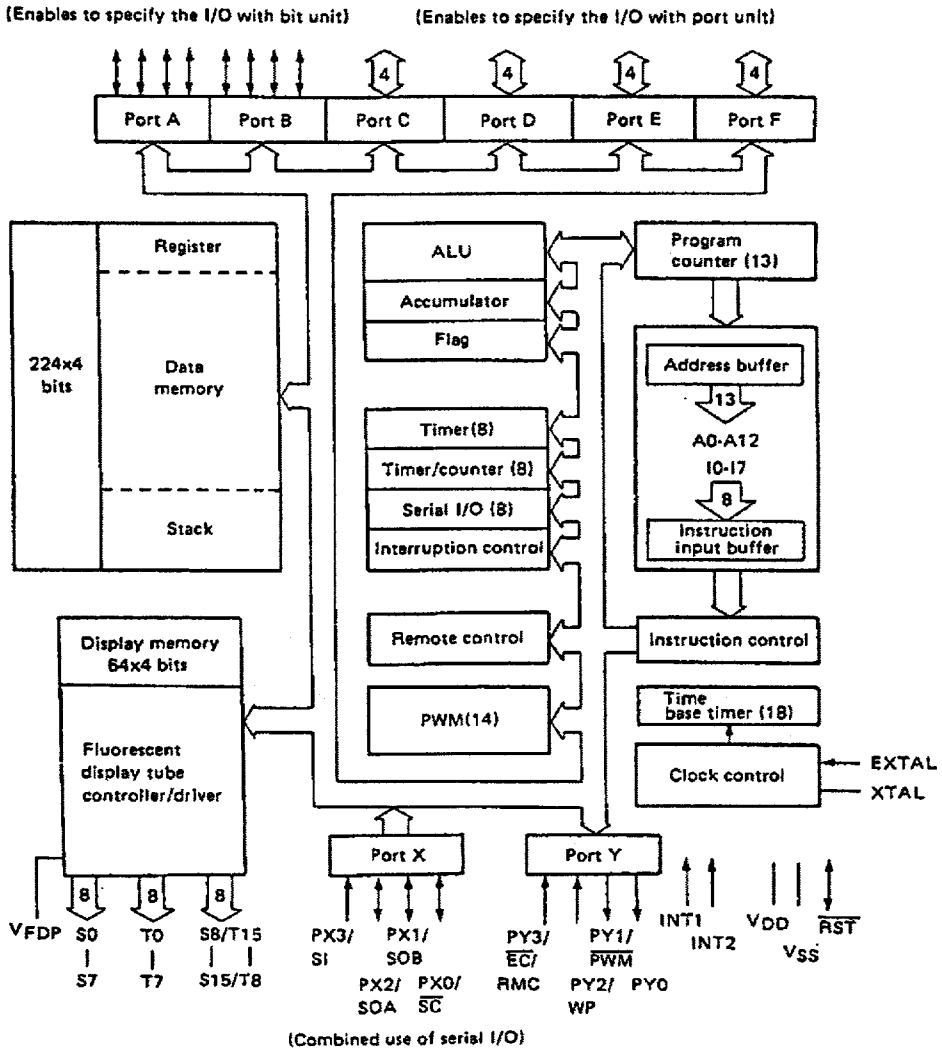
Note) Mask options are determined according to the CXP5010 category.
For details refer to the product list.

Structure

Silicon gate CMOS IC

60178A – ST

Block Diagram

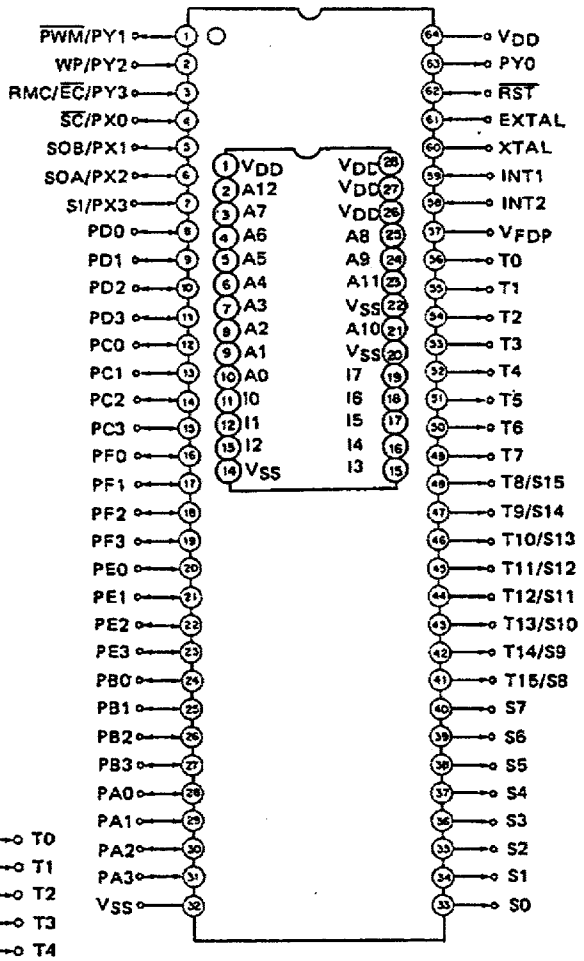


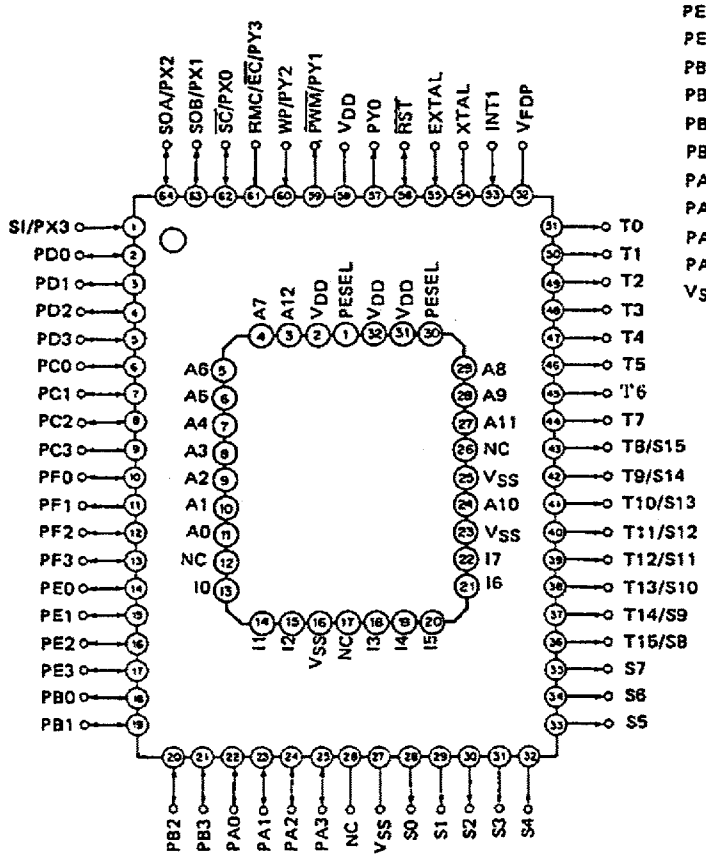
Pin Configuration Diagram (Top View)

Note 1) PESEL pin serves to switch the I/O signal of the socket on top of the package from interface with the evaluator (Eva mode) to interface with EPROM (Piggyback mode). Setting PESEL pin to H level brings Eva mode to enable the connection with the evaluator. Setting it to L level brings piggy mode to enable the mounting of EPROM. For QFP piggyback this switching is executed on the evaluator side. All there is to change is the plugging of EVACAP and EPROM otherwise no special measure is required.

2) Do not make any connections to NC pin

3) INT2 pin 58 SDIP can not be used with pin 64 QFP.





Absolute Maximum Ratings Ta = −20°C to +75°C, V_{SS} = 0V

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD}	−0.3 to +7.0	V	
Input voltage	V_{IN}	−0.3 to +7.0*1	V	
Output voltage	V_{OUT}	−0.3 to +7.0*1	V	
Display output voltage	V_{OD}	V_{DD} − 40 to V_{DD} + 0.3	V	As P channel transistor is open drain, V_{DD} voltage is determined as standard.
High level output current	I_{OH}	−10	mA	Other than display output pins*2 : per pin
	I_{ODH1}	−15	mA	Display output S0 to S7 : per pin
	I_{ODH2}	−30	mA	Display output T0 to T7, T8/S15 to T15/S8 : per pin
High level total output current	ΣI_{OH}	−40	mA	Total of other than display output pins
	ΣI_{ODH}	−60	mA	Total of display output pins
Low level output current	I_{OL}	17	mA	Port 1 pin
Low level total output current	ΣI_{OL}	50	mA	Entire pin total
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +150	°C	
Allowable power dissipation	P_D	1000	mW	SDIP
		600	mW	QFP

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operation conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1) V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2) Specifies the output current of the general purpose I/O port PA to PF, PX0 to PX2, PY0 and PY1.

Recommended Operating Condition V_{SS} = 0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range during operation
		3.5	5.5	V	Guaranteed data hold operation range during STOP
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*1
	V_{IHEX}	V_{DD}−0.4	V_{DD}+0.3	V	EXTAL pin*2
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*1
	V_{ILEX}	−0.3	0.4	V	EXTAL pin*2
Operating temperature	Topr	−20	+75	°C	

*1) They are the respective pins of INT1, INT2, PX0, PX3, PY2, PY3 and $\overline{RST}$.

*2) Specified only during external clock input.

Electrical Characteristics

DC characteristics

Ta = −20°C to +75°C, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PF, PX0 to PX2, PY0, PY1, $\overline{RST}$ (V_{OL} only)	V_{DD} = 4.5V, I_{OH} = −0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = −1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
Input current	I_{IH}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	μA
	I_{ILE}	EXTAL	V_{DD} = 5.5V, V_{IL} = 0.4V	−0.5		−40	μA
	I_{ILR}	$\overline{RST}$ *2	V_{DD} = 5.5V, V_{IL} = 0.4V	−1.5		−400	μA
High impedance I/O leakage current	I_{IZ}	PA to PF, PX0 to PX3, PY2, PY3, INT1, INT2, $\overline{RST}$ *2	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	μA
Display output current	I_{OH}	S0 to S7	V_{DD} = 4.5V, V_{OH} = V_{DD} − 2.5V	−7			mA
		S8/T15 to S15/T8, T0 to T7		−15			mA
Open drain output leakage current (P-CH Tr OFF in state)	I_{LOL}	S0 to S7, S8/T15 to S15/T8, T0 to T7	V_{DD} = 5.5V, V_{OL} = V_{DD} − 35V			−20	μA
Pull-down resistance*1	R_L	S0 to S7, S8/T15 to S15/T8, T0 to T7	V_{DD} = 5V, V_{FDP} = V_{DD} − 35V	60		270	kΩ
Supply current*4	I_{DD}	V_{DD}	Crystal oscillation (C1 = C2 = 22pF) of V_{DD} = 5.5V, 4.19MHz entire output pins open		5 (7)*3	15 (20)*3	mA
	I_{DDSP}	V_{DD}	SLEEP mode		3 (5)*3	9 (12)*3	mA
	I_{DDS}	V_{DD}	STOP mode			10	μA
Input capacity	C_{IN}	Other than S0 to S7, S8/T15 to S15/T8, T0 to T7, V_{SS}, V_{DD} pins	Clock 1MHz, 0V other than the measured pins		10	20	pF

*1) In case the incorporated pull-down resistance has been selected with mask option.

*2) $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when nonresistance is selected.

*3) Specifies the power supply current of the high speed version.

*4) However, except for EPROM power supply current.

AC Characteristics

(1) Clock timing

Ta = − 20°C to + 75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1	5	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	90		ns
System clock input rising and falling times	t_{CR} t_{CF}				200	ns
Event count clock input pulse width	t_{EL} t_{EH}	$\overline{EC}$	Fig. 3	tsys*1 +0.05		µs
Event count clock input rising and falling times	t_{ER} t_{EF}	$\overline{EC}$	Fig. 3		20	ms

*1) tsys in the standard version is tsys = 16/fc
tsys in the high speed version is tsys = 8/fc

Note) When adjusting the frequency accurately, there may be cases in which they may differ from Fig. 2.

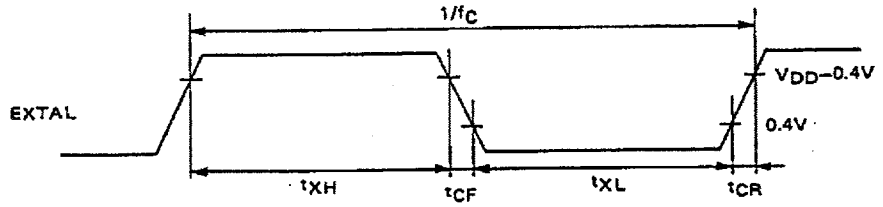


Fig. 1 Clock timing

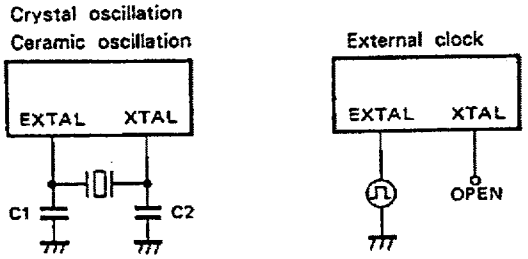


Fig. 2 Clock applying condition

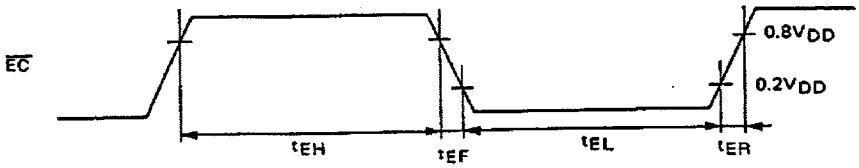


Fig. 3 Event count clock timing

(2) Serial transfer

Ta = −20°C to +75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Serial transfer clock ($\overline{SC}$) cycle time	t_{KCY}	$\overline{SC}$	Input mode	tsys/4 +1.42		µs
			Output mode	tsys		µs
Serial transfer clock ($\overline{SC}$) high and low level widths	t_{KH} t_{KL}	$\overline{SC}$	Input mode	tsys/8 +0.7		µs
			Output mode	tsys/2 −0.1		µs
Serial data input setup time (against $\overline{SC}$ ↑)	t_{SIK}	SI	$\overline{SC}$ input mode	0.1		µs
			$\overline{SC}$ output mode	0.2		µs
Serial data input hold time (against $\overline{SC}$ ↑)	t_{KSI}	SI	$\overline{SC}$ input mode	tsys/8 +0.5		µs
			$\overline{SC}$ output mode	0.1		µs
Data delay time from $\overline{SC}$ falling	t_{KSOA}	SOA			tsys/8 +0.5	µs
	t_{KSOB}	SOB			tsys/8 +0.5	µs

Note 1) tsys in the standard version is tsys = 16/fc
tsys in the high speed version is tsys = 8/fc
2) The Load of data output delay is 50pF + 1TTL

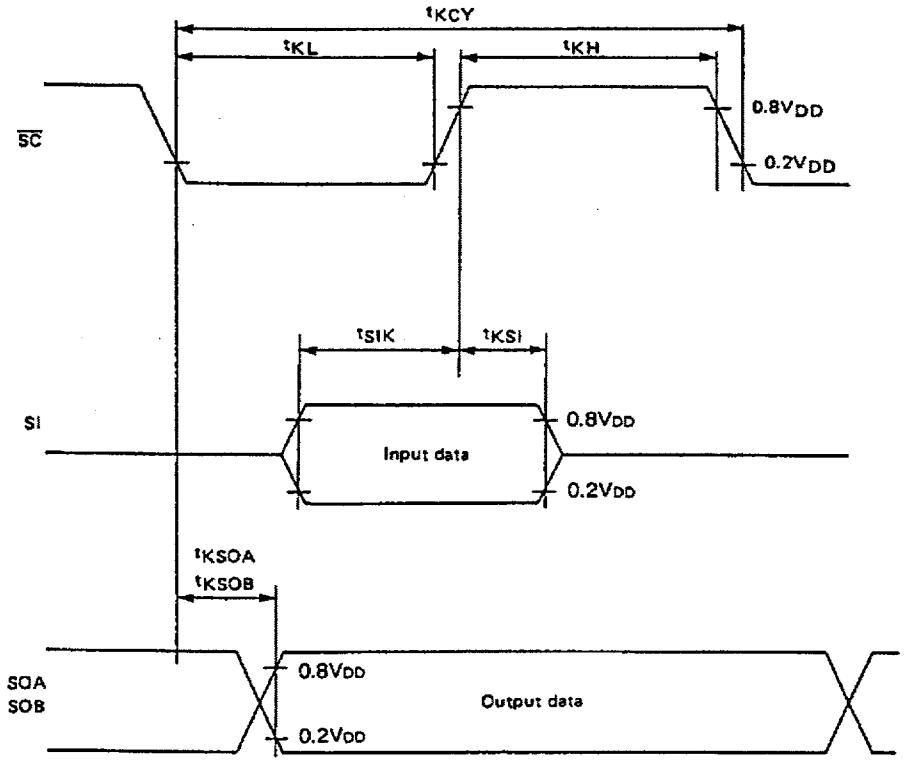


Fig. 4 Serial transfer timing

(3) Others

Ta = − 20°C to + 75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{I1H}, t_{I1L}	INT1	During edge detection mode	tsys + 0.05		µs
	t_{I2H}, t_{I2L}	INT2*1		tsys + 0.05		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		2tsys		µs
Wake-up input high level width	t_{WPH}	WP	STOP mode	500		ns
			SLEEP mode	tsys + 0.05		µs

Note) tsys in the standard version is tsys = 16/fc
tsys in the high speed version is fsys = 8/fc

*1) Specified only SDIP type.

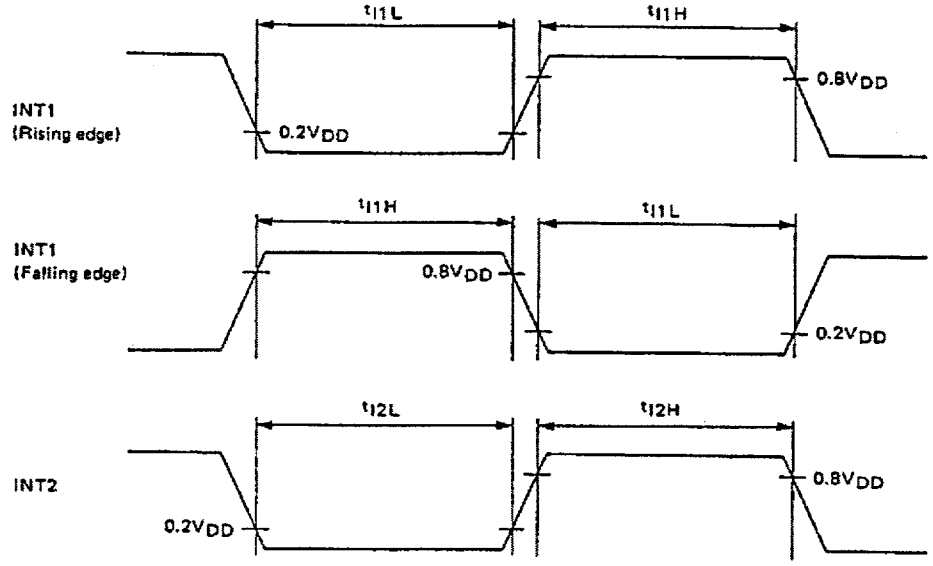


Fig. 5 Interruption input timing

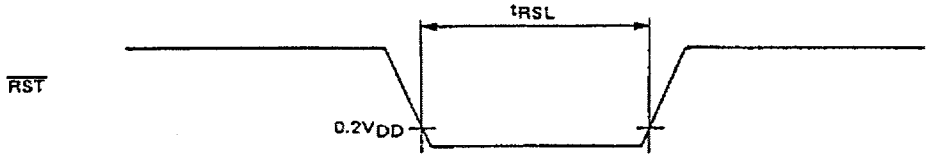


Fig. 6 Reset input timing

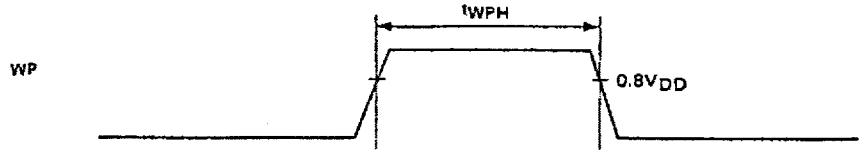


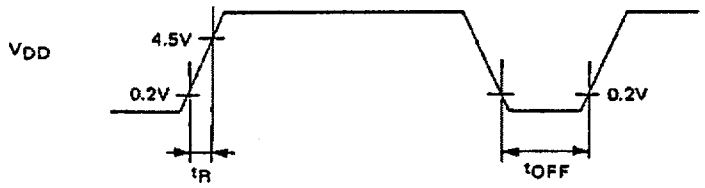
Fig. 7 Wake-up input timing

Power on reset *

$Ta = -20°C$ to $+75°C$, $V_{SS} = 0V$

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.



Raise the power supply smoothly.

Fig. 8 Power on reset

Notes on Application

See Fig. 9, Additive capacity calculation chart, when using the crystal oscillator and select the appropriate capacity.

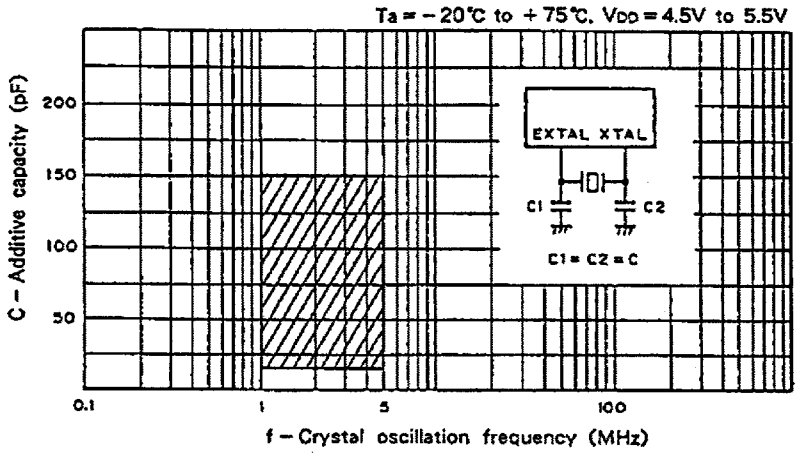


Fig. 9 Crystal oscillation circuit additive capacity calculation chart

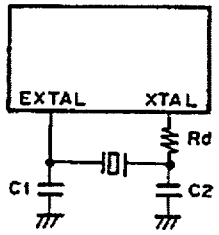
Note) The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

Fig. 10 shows recommended circuits and oscillators.

Use the trimmer capacitor to C1, in the case of accurate adjustment of the oscillation frequency.

1. Main clock

4.19MHz



Ceramic resonator

Manufacturer	Model	Frequency range(MHz)	C1(pF)	C2(pF)	Rd(Ω)
MURATA MFG CO., LTD.	CSA4.19MG040	4.19	100	100	—
	CSA4.19MGW040		built in	built in	—

Crystal oscillator

Manufacturer	Model	Frequency range(MHz)	C1(pF)	C2(pF)	Rd(Ω)
CITIZEN WATCH CO., LTD.	CSA309	4.19	10 (20 trimmer)	10	—
NIHON DEMPA KOGYO CO., LTD.	AT-51		15 (20 trimmer)	15	6.8k
KINSEKI LTD.	HC-49/U-S		22 (20 trimmer)	22	3.3k

Fig. 10 Recommended oscillation circuit

EPROM read timing Ta = −20°C to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Min.	Max.	Unit
Address→data input delay time	t_{ACC}	A0 to A12, I0 to I7		300	ns
Address→input holding time	t_{IH}	A0 to A12, I0 to I7	0		ns

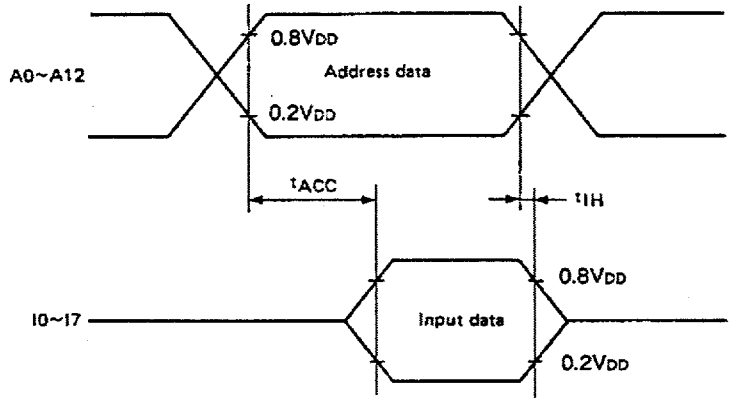


Fig. 11 EPROM timing

Products List

Optional item	Mass product	CXP5010-E01AS CXP5010-P01AS	CXP5010-U01AQ	CXP5010H-E02AS CXP5010H-P02AS	CXP5010H-U02AQ
Package	64-pin plastics SDIP/QFP	64-pin ceramic SDIP	64-pin ceramic QFP	64-pin ceramic SDIP	64-pin ceramic QFP
ROM capacity	CXP5014 : 4K-byte CXP5016 : 6K-byte	EPROM 8K-byte	EPROM 8K-byte	EPROM 8K-byte	EPROM 8K-byte
Speed	Standard /High speed	Standard	Standard	High speed	High speed
Pull-up resistance of reset pin	Existent /non-existent	Existent	Existent	Existent	Existent
Remote control input polarity	Normal/inverse	Normal	Normal	Normal	Normal
High tension proof pull-down resistance	Existent /non-existent	Non-existent	Non-existent	Non-existent	Non-existent

Note) E01AS, E02AS ; Evaluator chip
P01AS, P02AS ; Piggyback
U01AQ, U02AQ ; Piggyback/evaluator is combined chips