Single Supply 16-Bit, 100ksps, Sampling ADCs

FEATURES

- Sample Rate: 100ksps
- **Complete 16-Bit Solution on a Single 5V Supply**
- **Unipolar Input Range: 0V to 4V (LTC1605-1)**
- **Bipolar Input Range: ±4V (LTC1605-2)**
- **Power Dissipation: 55mW Typ**
- Signal-to-Noise Ratio: 86dB Typ
- Operates with Internal or External Reference
- Internal Synchronized Clock
- 28-Pin 0.3" PDIP and SSOP Packages

APPLICATIONS

- Industrial Process Control
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition for PCs
- Digital Signal Processing

DESCRIPTION

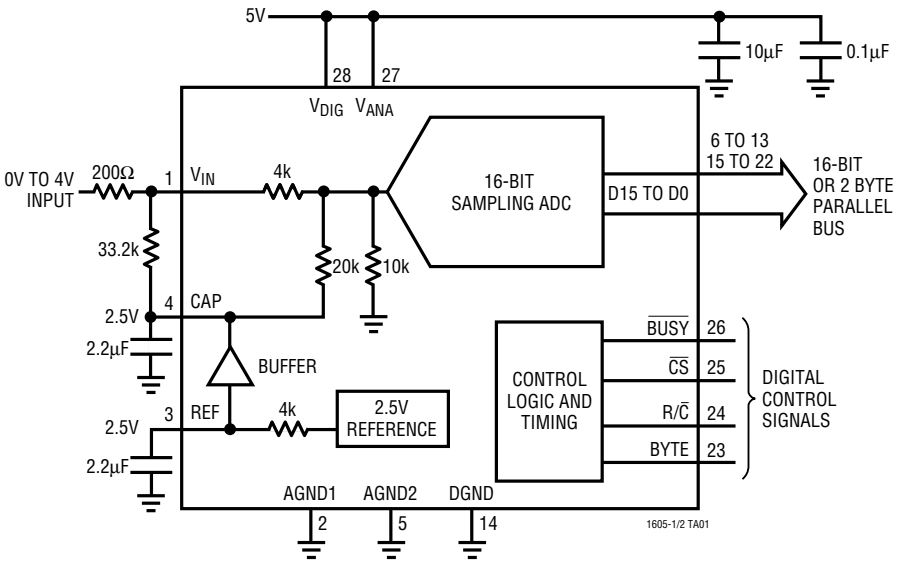
The LTC®1605-1/LTC1605-2 are 100ksps, sampling 16-bit A/D converters that draw only 55mW (typical) from a single 5V supply. These easy-to-use devices include a sample-and-hold, precision reference, switched capacitor successive approximation A/D and trimmed internal clock.

The LTC1605-1's input range is 0V to 4V while the LTC1605-2's input range is ±4V. An external reference can be used if greater accuracy over temperature is needed.

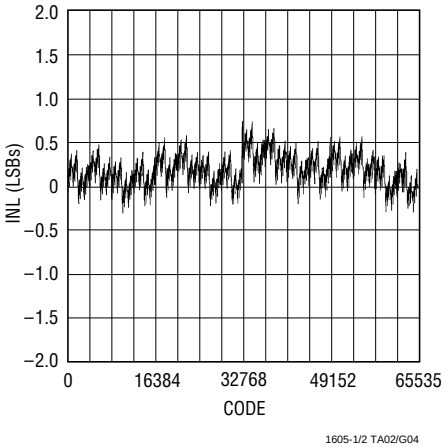
The ADC has a microprocessor compatible, 16-bit or two byte parallel output port. A convert start input and a data ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

LTC1605-1 Low Power, 100kHz, 16-Bit Sampling ADC on 5V Supply



Typical INL Curve

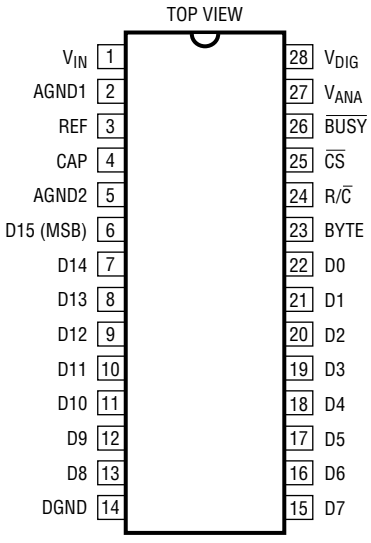


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{ANA} 7V
V_{DIG} to V_{ANA} 0.3V
V_{DIG} 7V
Ground Voltage Difference
DGND, AGND1 and AGND2 ..... ±0.3V
Analog Inputs (Note 3)
V_{IN} ..... ±25V
CAP ..... V_{ANA} + 0.3V to AGND2 – 0.3V
REF ..... Indefinite Short to AGND2
Momentary Short to V_{ANA}
Digital Input Voltage (Note 4) ..... V_{DGND} – 0.3V to 10V
Digital Output Voltage ..... V_{DGND} – 0.3V to V_{DIG} + 0.3V
Power Dissipation 500mW
Operating Ambient Temperature Range
LTC1605-1C/LTC1605-2C ..... 0°C to 70°C
LTC1605-1I/LTC1605-2I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

N PACKAGE
28-LEAD PDIP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 130°C/W (N)

ORDER PART NUMBER
LTC1605-1CG
LTC1605-1IG
LTC1605-2CG
LTC1605-2IG
LTC1605-1CN
LTC1605-1IN
LTC1605-2CN
LTC1605-2IN

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With external reference (Notes 5, 6).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution		●	16			Bits
No Missing Codes		●	15			Bits
Transition Noise				1		LSB_{RMS}
Integral Linearity Error	(Note 7)	●			±3	LSB
Zero Error	Ext. Reference = 2.5V (Note 8)	●			±10	mV
Zero Error Drift				±2		ppm/°C
Full-Scale Error Drift				±7		ppm/°C
Full-Scale Error	Ext. Reference = 2.5V (Notes 12, 13)	●			±0.50	%
Full-Scale Error Drift	Ext. Reference = 2.5V			±2		ppm/°C
Power Supply Sensitivity $V_{ANA} = V_{DIG} = V_{DD}$	V_{DD} = 5V ±5% (Note 9)				±8	LSB

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{ANA} ≤ 5.25V, 4.75V ≤ V_{DIG} ≤ 5.25V					
		LTC1605-1	●		0 to 4		V
		LTC1605-2	●		±4		V
C_{IN}	Analog Input Capacitance				10		pF
R_{IN}	Analog Input Impedance				10		kΩ

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 5, 14)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	1kHz Input Signal (Note 14) 10kHz Input Signal 20kHz, –60dB Input Signal			87 85 30		dB dB dB
THD	Total Harmonic Distortion	1kHz Input Signal, First 5 Harmonics 10kHz Input Signal, First 5 Harmonics			–101 –92		dB dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal 10kHz Input Signal			–101 –92		dB dB
	Full-Power Bandwidth	(Note 15)			275		kHz
	Aperture Delay				40		ns
	Aperture Jitter				Sufficient to Meet AC Specs		
	Transient Response	Full-Scale Step (Note 9)				2	µs
	Overvoltage Recovery	(Note 16)			150		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0	●	2.470	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0			±5		ppm/°C
Internal Reference Source Current				1		µA
External Reference Voltage for Specified Linearity	(Notes 9, 10)		2.30	2.50	2.70	V
External Reference Current Drain	Ext. Reference = 2.5V (Note 9)	●			100	µA
CAP Output Voltage	I_{OUT} = 0			2.50		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V		●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V		●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}		●			±10	µA
C_{IN}	Digital Input Capacitance					5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V	I_O = –10µA			4.5		V
			I_O = –200µA	●	4.0			V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V	I_O = 160µA			0.05		V
			I_O = 1.6mA	●		0.10	0.4	V
I_{OZ}	Hi-Z Output Leakage D15 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High		●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D15 to D0	$\overline{CS}$ High (Note 9)		●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V				–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}				10		mA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	100			kHz
t_{CONV}	Conversion Time		●			8	µs
t_{ACQ}	Acquisition Time		●			2	µs
t_1	Convert Pulse Width	(Note 11)	●	40			ns
t_2	Data Valid Delay After R/$\overline{C}$↓	(Note 9)	●			8	µs
t_3	$\overline{BUSY}$ Delay from R/$\overline{C}$↓	C_L = 50pF	●			65	ns
t_4	$\overline{BUSY}$ Low					8	µs
t_5	$\overline{BUSY}$ Delay After End of Conversion				220		ns
t_6	Aperture Delay				40		ns
t_7	Bus Relinquish Time		●	10	35	83	ns
t_8	$\overline{BUSY}$ Delay After Data Valid		●	50	200		ns
t_9	Previous Data Valid After R/$\overline{C}$↓				7.4		µs
t_{10}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	(Notes 9, 10)		10			ns
t_{11}	Time Between Conversions			10			µs
t_{12}	Bus Access and Byte Delay	(Notes 9, 10)		10		83	ns

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Notes 9, 10)		4.75		5.25	V
I_{DD}	Positive Supply Current		●		11	16	mA
P_{DIS}	Power Dissipation				55	80	mW

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND1 and AGND2 wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below ground or above V_{ANA} = V_{DIG} = V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below ground or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below ground, they will be clamped by internal diodes. This product can handle input currents of 90mA below ground without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, f_{SAMPLE} = 100kHz, t_r = t_f = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a V_{IN} input with respect to ground.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual end points of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Zero error for the LTC1605-1 is the voltage measured from 0.5LSB when the output code flickers between 0000 0000 0000 0000 and 0000 0000 0000 0001. Zero error for the LTC1605-2 is the voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

Note 11: With $\overline{CS}$ low the falling R/$\overline{C}$ edge starts a conversion. If R/$\overline{C}$ returns high at a critical point during the conversion it can create small errors. For best results ensure that R/$\overline{C}$ returns high within 3µs after the start of the conversion.

Note 12: As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer.

Note 13: Full-scale error is the untrimmed deviation from ideal last code transition, divided by the full-scale range and includes the effect of offset error.

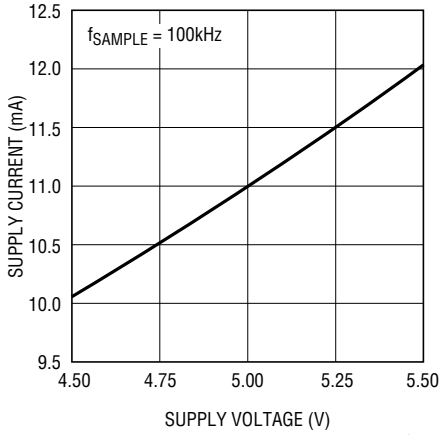
Note 14: All specifications in dB are referred to a full-scale 4V input for the LTC1605-1 and to ±4V input for the LTC1605-2.

Note 15: Full-power bandwidth is defined as full-scale input frequency at which a signal-to-(noise + distortion) degrades to 60dB or 10 bits of accuracy.

Note 16: Recovers to specified performance after (±20V) input overvoltage for the LTC1605-1 and ±15V for the LTC1605-2.

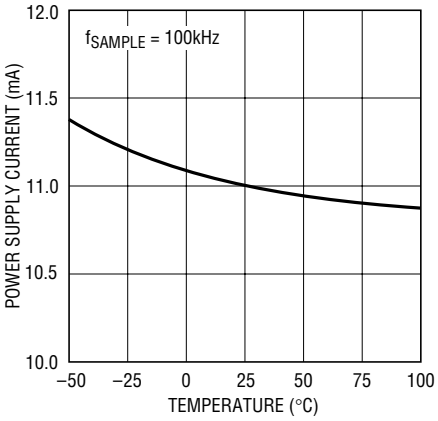
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



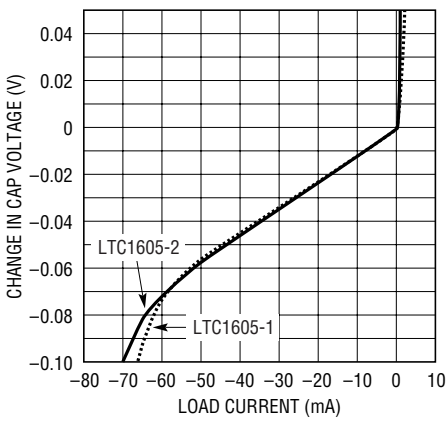
1605-1/2 G01

Supply Current vs Temperature



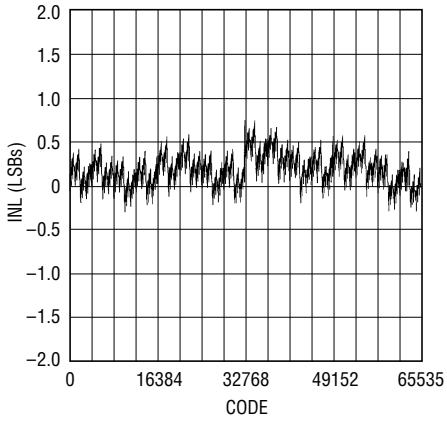
1605-1/2 G02

Change in CAP Voltage vs Load Current



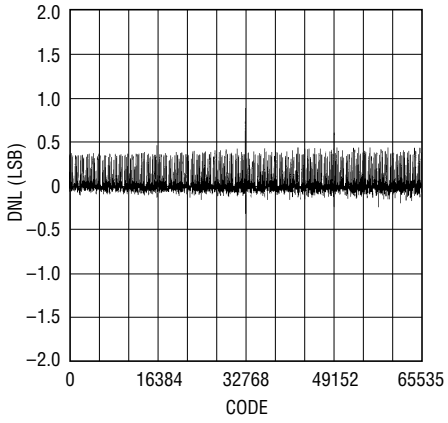
1605-1/2 G03

Typical INL Curve



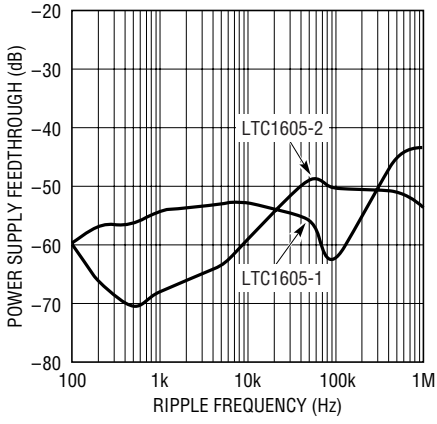
1605-1/2 TA02/G04

Typical DNL Curve



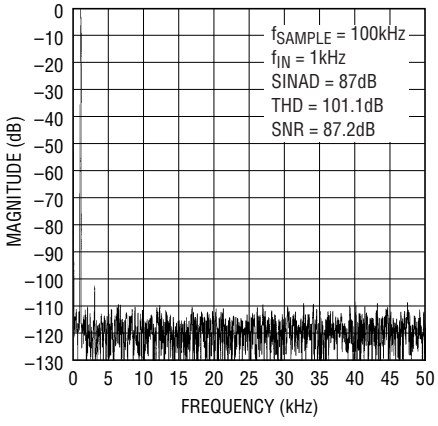
1605-1/2 G05

Power Supply Feedthrough vs Ripple Frequency



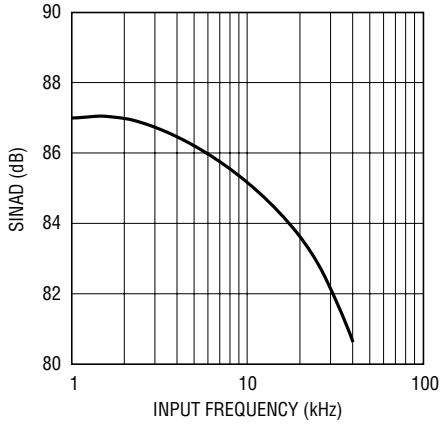
LTXXXX GXX

LTC1605-2 Nonaveraged 4096-Point FFT Plot



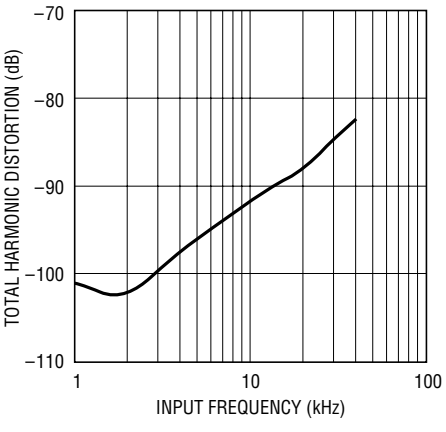
1605-1/2 G07/F11

SINAD vs Input Frequency (LTC1605-2)



1605-1/2 G08

Total Harmonic Distortion vs Input Frequency (LTC1605-2)



1605-1/2 G09

PIN FUNCTIONS

V_{IN} (Pin 1): Analog Input. Connect through a 200Ω resistor to the analog input. Full-scale input range is 0V to 4V for the LTC1605-1 and ±4V for the LTC1605-2.

AGND1 (Pin 2): Analog Ground. Tie to analog ground plane.

REF (Pin 3): 2.5V Reference Output. Bypass with 2.2µF tantalum capacitor. Can be driven with an external reference.

CAP (Pin 4): Reference Buffer Output. Bypass with 2.2µF tantalum capacitor.

AGND2 (Pin 5): Analog Ground. Tie to analog ground plane.

D15 to D8 (Pins 6 to 13): Three-State Data Outputs. Hi-Z state when $\overline{CS}$ is high or when R/$\overline{C}$ is low.

DGND (Pin 14): Digital Ground.

D7 to D0 (Pins 15 to 22): Three-State Data Outputs. Hi-Z state when $\overline{CS}$ is high or when R/$\overline{C}$ is low.

BYTE (Pin 23): Byte Select. With BYTE low, data will be output with Pin 6 (D15) being the MSB and Pin 22 (D0) being the LSB. With BYTE high the upper eight bits and the lower eight bits will be switched. The MSB is output on Pin 15 and bit 8 is output on Pin 22. Bit 7 is output on Pin 6 and the LSB is output on Pin 13.

R/$\overline{C}$ (Pin 24): Read/$\overline{Convert}$ Input. With $\overline{CS}$ low, a falling edge on R/$\overline{C}$ puts the internal sample-and-hold into the hold state and starts a conversion. With $\overline{CS}$ low, a rising edge on R/$\overline{C}$ enables the output data bits.

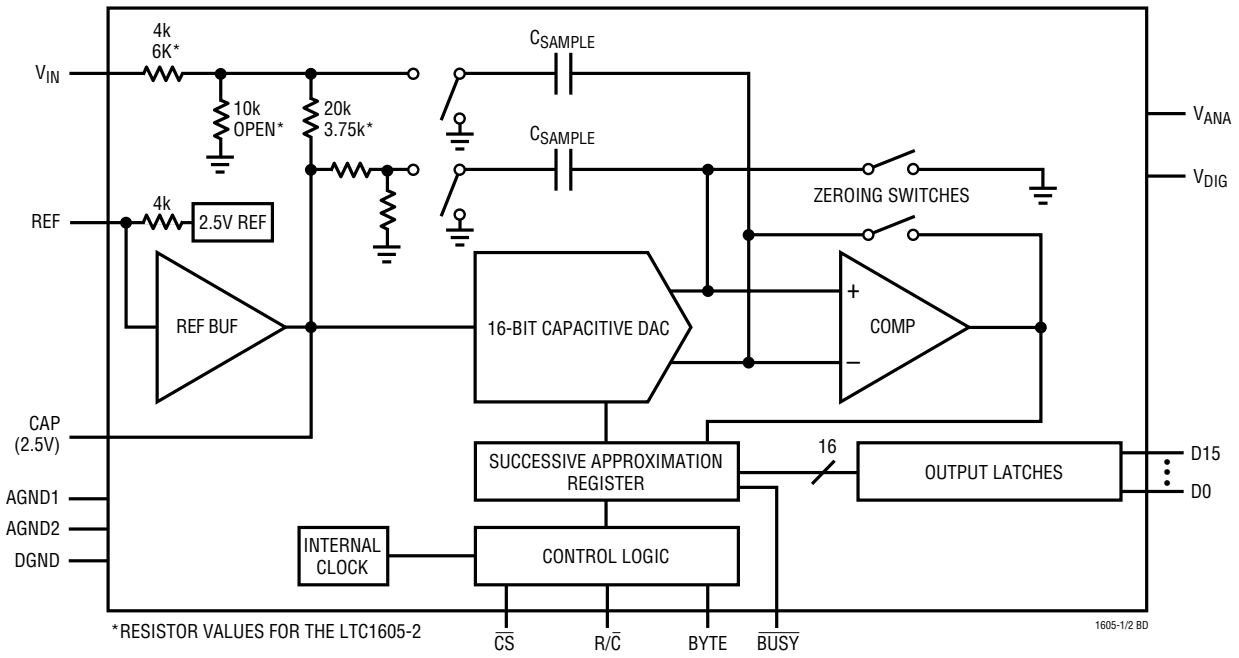
$\overline{CS}$ (Pin 25): $\overline{Chip\ Select}$. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ low, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ high, a falling edge on $\overline{CS}$ will enable the output data.

$\overline{BUSY}$ (Pin 26): Output Shows Converter Status. It is low when a conversion is in progress. Data valid on the rising edge of $\overline{BUSY}$. $\overline{CS}$ or R/$\overline{C}$ must be high when $\overline{BUSY}$ rises or another conversion will start without time for signal acquisition.

V_{ANA} (Pin 27): 5V Analog Supply. Bypass to ground with a 0.1µF ceramic and a 10µF tantalum capacitor.

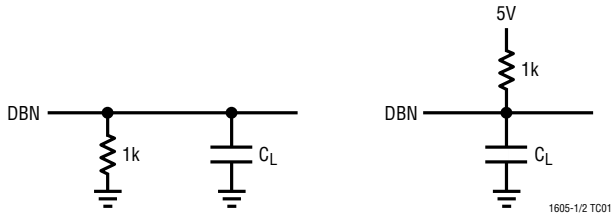
V_{DIG} (Pin 28): 5V Digital Supply. Connect directly to Pin 27.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

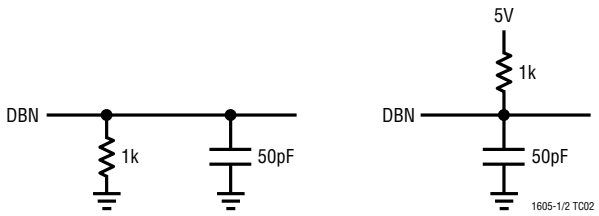
Load Circuit for Access Timing



A. HI-Z TO V_{OH} AND V_{OL} TO V_{OH}

B. HI-Z TO V_{OL} AND V_{OH} TO V_{OL}

Load Circuit for Output Float Delay



A. V_{OH} TO HI-Z

B. V_{OL} TO HI-Z

APPLICATIONS INFORMATION

Conversion Details

The LTC1605-1/LTC1605-2 use a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 16-bit or two byte parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and R/$\overline{C}$ inputs. At the start of conversion, the successive approximation register (SAR) is reset. Once a conversion cycle has begun, it cannot be restarted.

During the conversion, the internal 16-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, V_{IN} is connected through the resistor divider and S1 to the sample-and-hold capacitor during the acquire phase and the comparator offset is nulled by the autozero switch, S3. In this acquire phase, a minimum delay of 2µs will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, S3 opens, putting the comparator into the compare mode. The input switch S2 switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the V_{IN} input charge. The SAR contents (a 16-bit data word) that represents the V_{IN} are loaded into the 16-bit output latches.

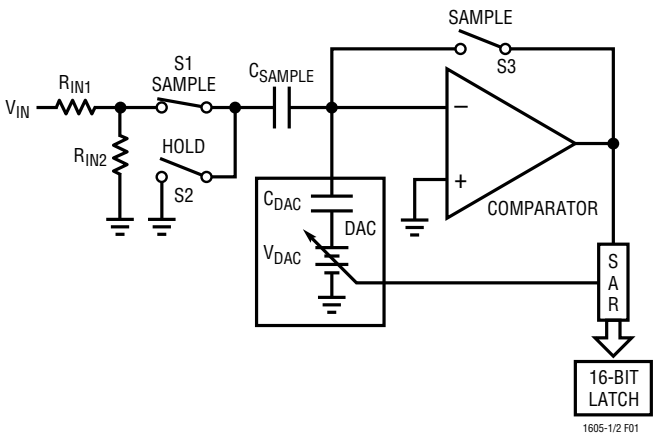


Figure 1. LTC1605-1/LTC1605-2 Simplified Equivalent Circuit

Driving the Analog Inputs

The nominal input range for the LTC1605-1 is 0V to 4V or ($1.6V_{REF}$) and for the LTC1605-2 the input range is ±4V or ($\pm 1.6V_{REF}$). The inputs are overvoltage protected to ±25V. The input impedance is typically 10kΩ; therefore, it should be driven by a low impedance source. Wideband noise coupling into the input can be minimized by placing a 1000pF capacitor at the input as shown in Figure 2. An NPO-type capacitor gives the lowest distortion. Place the capacitor as close to the device input pin as possible. If an amplifier is to be used to drive the input, care should be taken to select an amplifier with adequate accuracy, linearity and noise for the application. The following list is a summary of the op amps that are suitable for driving the LTC1605-1/LTC1605-2. More detailed information is available in the Linear Technology data books and LinearView™ CD-ROM.

LinearView is a trademark of Linear Technology Corporation

APPLICATIONS INFORMATION

LT®1007 - Low noise precision amplifier. 2.7mA supply current ±5V to ±15V supplies. Gain bandwidth product 8MHz. DC applications.

LT1097 - Low cost, low power precision amplifier. 300µA supply current. ±5V to ±15V supplies. Gain bandwidth product 0.7MHz. DC applications.

LT1227 - 140MHz video current feedback amplifier. 10mA supply current. ±5V to ±15V supplies. Low noise and low distortion.

LT1360 - 37MHz voltage feedback amplifier. 3.8mA supply current. ±5V to ±15V supplies. Good AC/DC specs.

LT1363 - 50MHz voltage feedback amplifier. 6.3mA supply current. Good AC/DC specs.

LT1364/LT1365 - Dual and quad 50MHz voltage feedback amplifiers. 6.3mA supply current per amplifier. Good AC/DC specs.

LT1468 - 90MHz, 22V/µs 16-Bit Accurate Amplifier

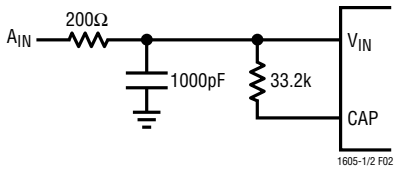


Figure 2. Analog Input Filtering

Internal Voltage Reference

The LTC1605-1/LTC1605-2 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.50V. The full-scale range of the ADC is equal to ($1.6V_{REF}$) or nominally 0V to 4V for the LTC1605-1 and ($\pm 1.6V_{REF}$) or nominally ±4V for the LTC1605-2. The output of the reference is connected to the input of a unity-gain buffer through a 4k resistor (see Figure 3). The input to the buffer or the output of the reference is available at REF (Pin 3). The internal reference can be overdriven with an external reference if more accuracy is needed. The buffer output drives the internal DAC and is available at CAP (Pin 4). The CAP pin can be used to drive a steady DC load of less than 2mA. Driving an AC load is not recommended because it can cause the performance of the converter to degrade.

For minimum code transition noise the REF pin and the CAP pin should each be decoupled with a capacitor to filter wideband noise from the reference and the buffer (2.2µF tantalum).

Offset and Gain Adjustments

The LTC1605-1/LTC1605-2 offset and full-scale errors have been trimmed at the factory with the external resistors shown in Figure 4. This allows for external adjustment of offset and full scale in applications where absolute accuracy is important. See Figure 5 for the offset and gain trim circuit for the LTC1605-1/LTC1605-2. First adjust the offset to zero by adjusting resistor R3. Apply an input voltage of 30.5µV (0.5LSB) and adjust R3 so the code is changing between 0000 0000 0000 0001 and 0000 0000 0000 0000. The gain error is trimmed by adjusting resistor R4. An input voltage of 3.999908V (FS – 1.5LSB) is applied to V_{IN} and R4 is adjusted until the output code is changing between 1111 1111 1111 1110 and 1111 1111 1111 1111. Figure 6a shows the unipolar transfer characteristic of the LTC1605-1.

For the LTC1605-2, first adjust the offset to zero by adjusting resistor R3. Apply an input voltage of –61µV (–0.5LSB) and adjust R3 so the code is changing between 1111 1111 1111 1111 and 0000 0000 0000 0000. The gain error is trimmed by adjusting resistor R4. An input voltage of 3.999817V (+FS – 1.5LSB) is applied to V_{IN} and R4 is adjusted until the outut code is changing between 0111 1111 1111 1110 and 0111 1111 1111 1111. Figure 6b shows the bipolar transfer characteristics of the LTC1605-2.

DC Performance

One way of measuring the transition noise associated with a high resolution ADC is to use a technique where a DC signal is applied to the input of the ADC and the resulting output codes are collected over a large number of conversions. For example, in Figure 7 the distribution of output code is shown for a DC input that has been digitized 10000 times. The distribution is Gaussian and the RMS code transition is about 1LSB.

APPLICATIONS INFORMATION

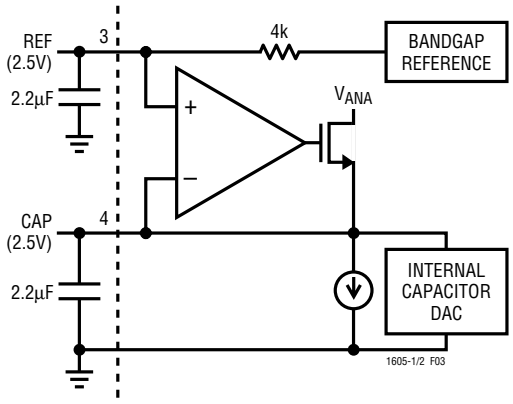


Figure 3. Internal or External Reference Source

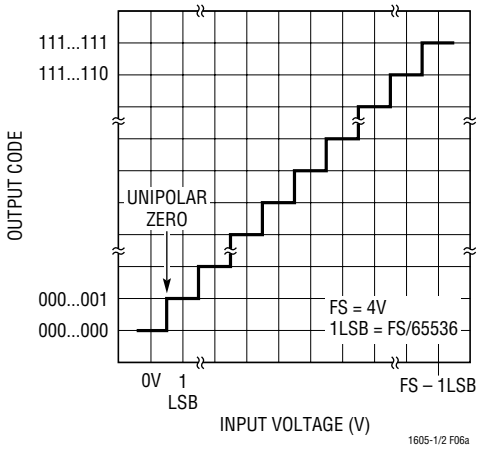


Figure 6a. LTC1605-1 Unipolar Transfer Characteristics

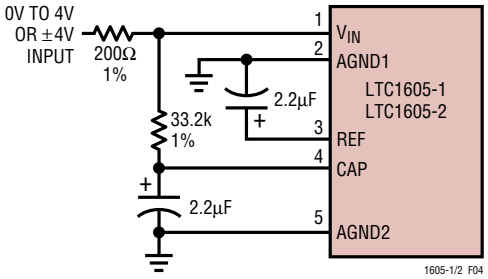


Figure 4. 0V to 4V Input for the LTC1605-1 and ±4V for the LTC1605-2 Without Trim

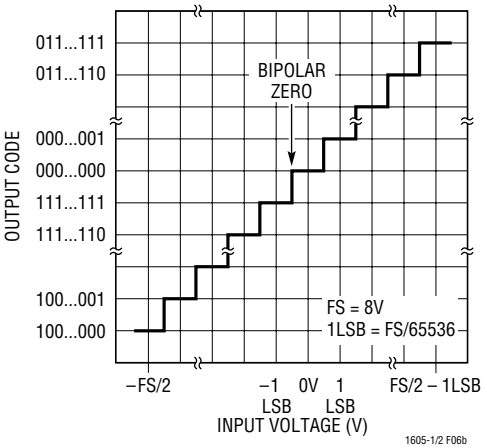


Figure 6B. LTC1605-2 Bipolar Transfer Characteristics

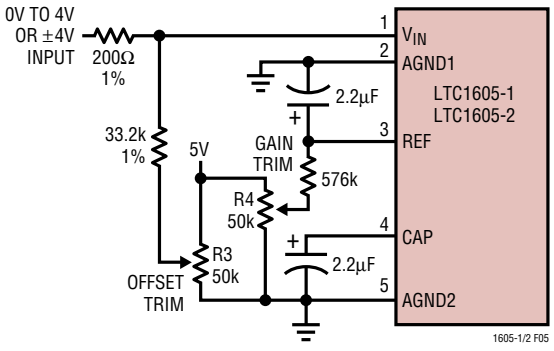


Figure 5. 0V to 4V Input for the LTC1605-1 and ±4V for the LTC1605-2 with Offset and Gain Trim

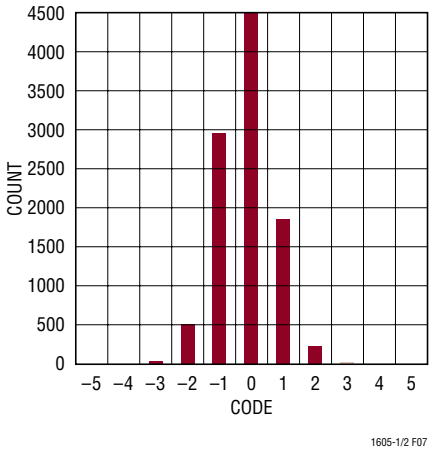


Figure 7. Histogram for 10000 Conversions

APPLICATIONS INFORMATION

DIGITAL INTERFACE

Internal Clock

The ADC has an internal clock that is trimmed to achieve a typical conversion time of 7µs. No external adjustments are required and, with the typical acquisition time of 1µs, throughput performance of 100ksps is assured.

Timing and Control

Conversion start and data read are controlled by two digital inputs: $\overline{CS}$ and R/$\overline{C}$. To start a conversion and put the sample-and-hold into the hold mode, bring $\overline{CS}$ and R/$\overline{C}$ low for no less than 40ns. Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output and this is low while the conversion is in progress.

There are two modes of operation. The first mode is shown in Figure 8. The digital input R/$\overline{C}$ is used to control the start of conversion. $\overline{CS}$ is tied low. When R/$\overline{C}$ goes low, the sample-and-hold goes into the hold mode and a conversion is started. $\overline{BUSY}$ goes low and stays low during the conversion and will go back high after the conversion has been completed and the internal output shift registers have been updated. R/$\overline{C}$ should remain low for no less than 40ns. During the time R/$\overline{C}$ is low, the digital outputs are in a Hi-Z state. R/$\overline{C}$ should be brought back high within 3µs after the start of the conversion to ensure that no errors occur in the digitized result. The second mode, shown in Figure 9, uses the $\overline{CS}$ signal to control the start of a conversion and the reading of the digital output. In this mode, the R/$\overline{C}$ input signal should be brought low no less than 10ns before the falling edge of $\overline{CS}$. The minimum pulse width for $\overline{CS}$ is 40ns. When $\overline{CS}$ falls, $\overline{BUSY}$ goes low and will stay low until the end of the conversion. $\overline{BUSY}$ will go high after the conversion has been completed. The new data is valid when $\overline{CS}$ is brought back low again to initiate a read. Again, it is recommended that both R/$\overline{C}$ and $\overline{CS}$ return high within 3µs after the start of the conversion.

Output Data

The output data can be read as a 16-bit word or it can be read as two 8-bit bytes. The format of the output data is straight binary for the LTC1605-1 and two's complement for the LTC1605-2. The digital input pin BYTE is used to control the two byte read. With the BYTE pin low, the first eight MSBs are output on the D15 to D8 pins and the eight LSBs are output on the D7 to D0 pins. When the BYTE pin is taken high, the eight LSBs replace the eight MSBs (Figure 10).

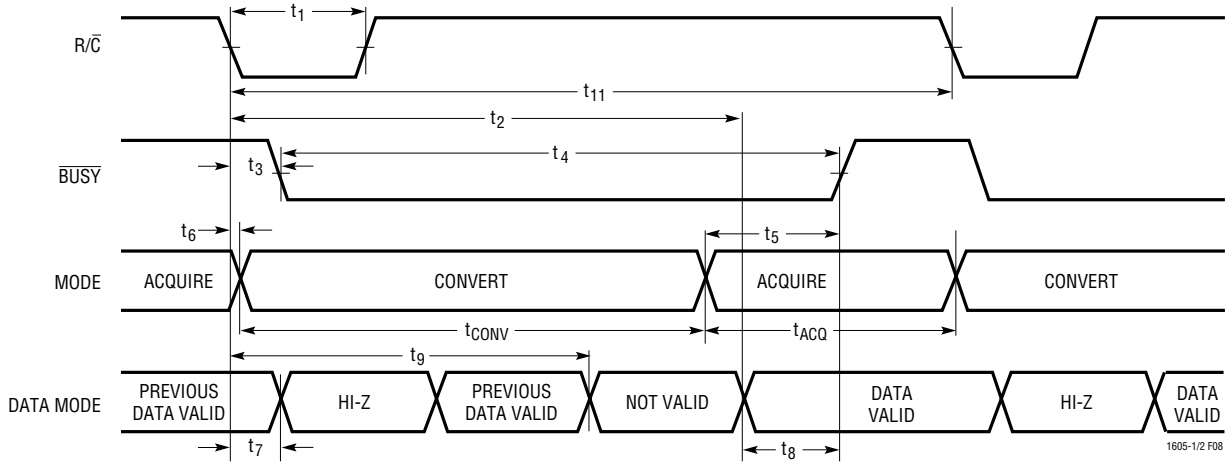


Figure 8. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low)

APPLICATIONS INFORMATION

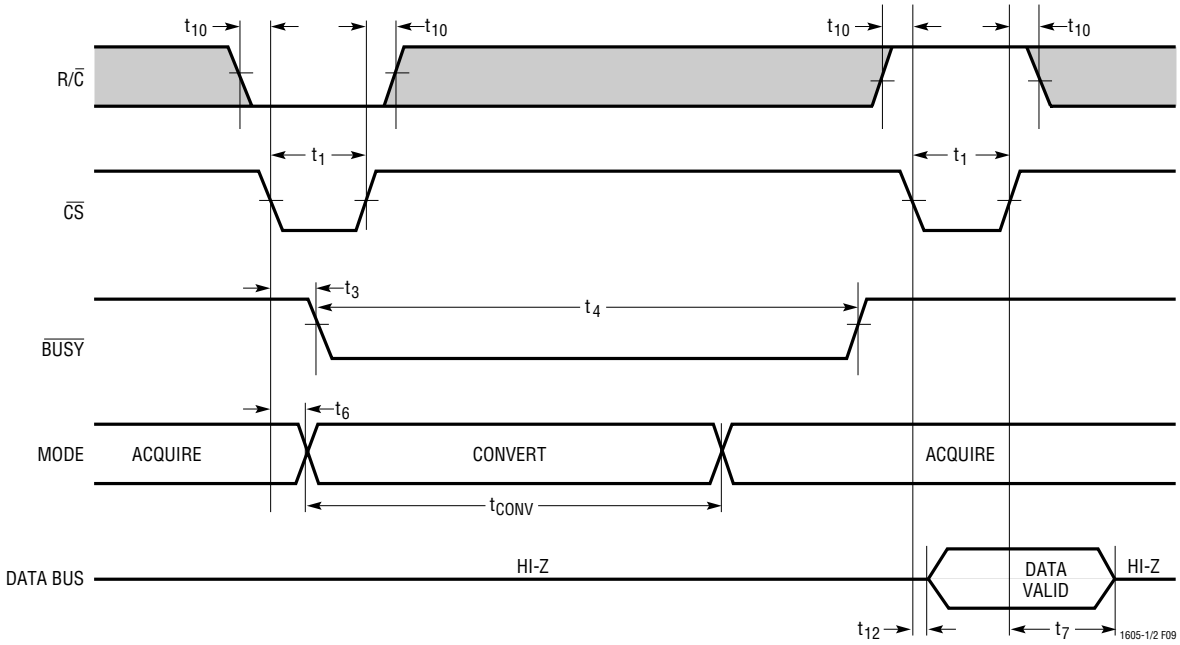


Figure 9. Using $\overline{CS}$ to Control Conversion and Read Timing

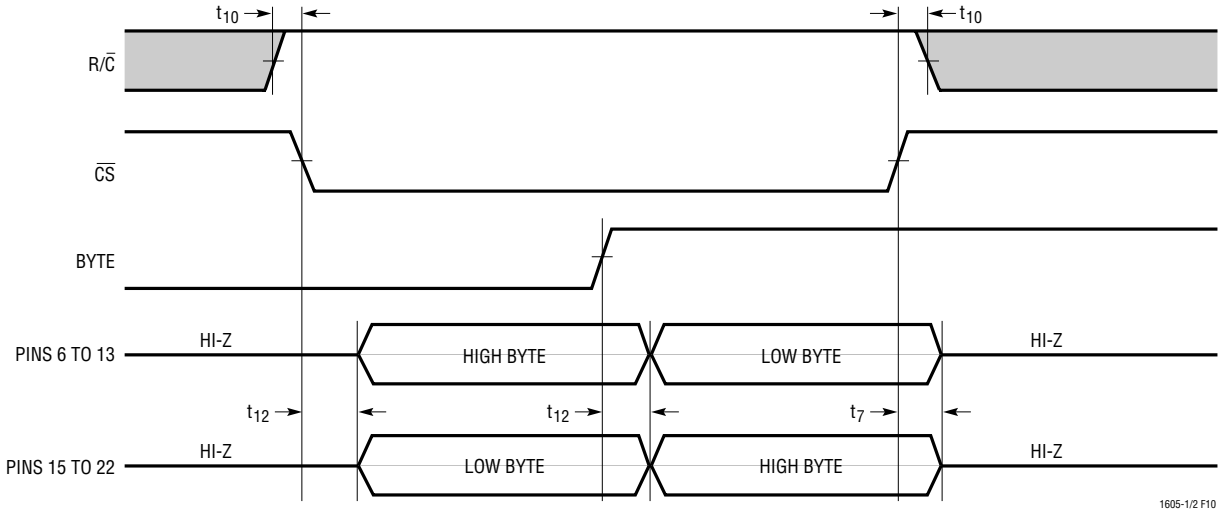


Figure 10. Using $\overline{CS}$ and BYTE to Control Data Bus Read Timing

APPLICATIONS INFORMATION

Dynamic Performance

FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 11 shows a typical LTC1605-2 FFT plot which yields a SINAD of 87dB and THD of –101.1dB.

Signal-to-Noise Ratio

The Signal-to-Noise and Distortion Ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 11 shows a typical SINAD of 87dB with a 100kHz sampling rate and a 1kHz input.

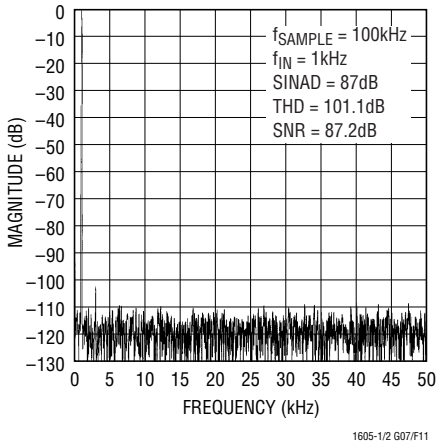


Figure 11. LTC1605-2 Nonaveraged 4096-Point FFT Plot

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

Board Layout, Power Supplies and Decoupling

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1605-1/LTC1605-2, a printed circuit board is required. Layout for the printed circuit board should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

Figures 12 through 15 show a layout for a suggested evaluation circuit which will help obtain the best performance from the 16-bit ADC. Additional information regarding the evaluation circuit and Gerber files for the PC board layout are available from Linear Technology or your local sales office. Pay particular attention to the design of the analog and digital ground planes. The DGND pin of the LTC1605-1/LTC1605-2 can be tied to the analog ground plane. Placing the bypass capacitor as close as possible to the power supply, the reference and reference buffer output is very important. Low impedance common returns for these bypass capacitors are essential to low noise operation of the ADC, and the PC track width for these lines should be as wide as possible. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. The digital output latches and the onboard sampling clock have been placed on the digital ground plane. The two ground planes are tied together at the power supply ground connection.

APPLICATIONS INFORMATION

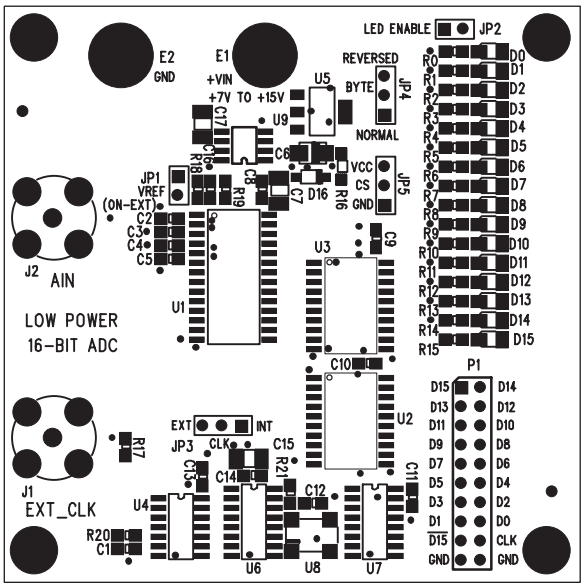


Figure 12. Component Side Silkscreen for the Suggested LTC1605-1/LTC1605-2 Evaluation Circuit

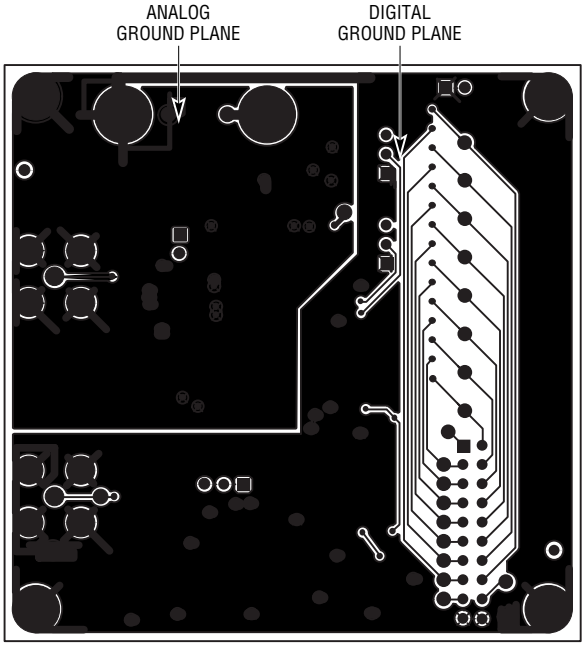


Figure 13. Bottom Side Showing Analog Ground Plane

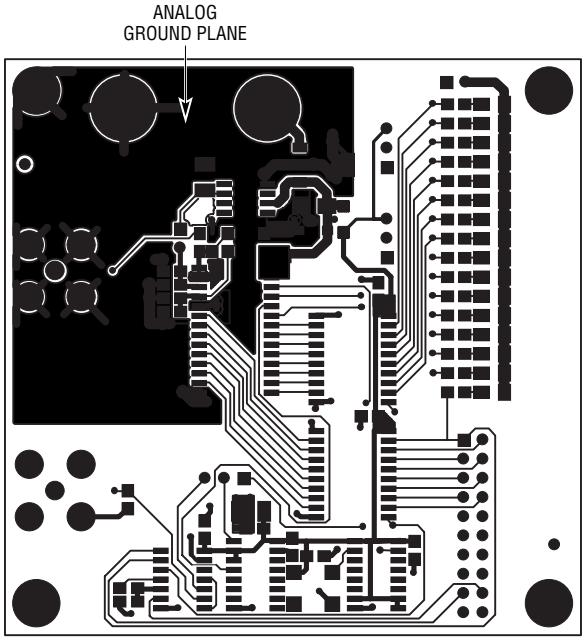


Figure 14. Component Side Showing Separate Analog and Digital Ground Plane

APPLICATIONS INFORMATION

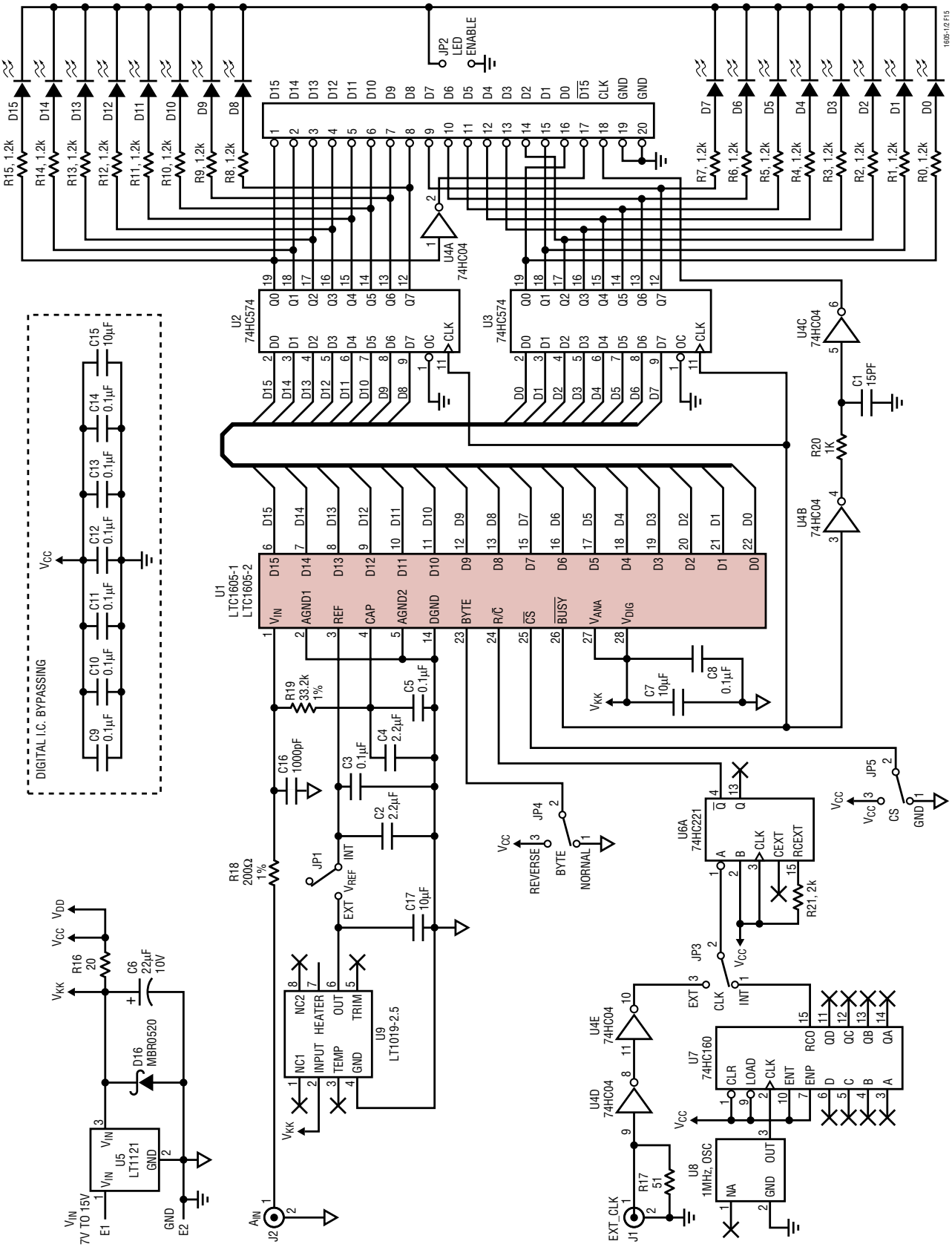


Figure 15. LTC1605-1 Suggested Evaluation Circuit Schematic

TYPICAL APPLICATIONS

The circuit in Figure 16 is an example showing the LTC1605 16-bit A/D converter and LTC1391 8-channel MUX connected to a 68HC11 controller. The LTC1605's 16-bit data output is read in two 8-bit bytes using Pins 6 (MSB, Bit7) through 13 (Bit8, Bit0), connected to the HC11's PORTC. The MUX's 4-bit serial address data is sent using the controller's SPI.

The process to convert a channel's input signal is shown in sample listing A. It begins with shifting in the MUX's channel data while the $\overline{SS}$ signal is a logic high. The MUX channel address is latched on the falling edge of $\overline{SS}$ and the chosen channel's input is applied at the LTC1605's input, Pin 1. Through the processor's PORTA, a low-going pulse is applied to the LTC1605's R/$\overline{C}$ pin, initiating a conversion. The processor then monitors the $\overline{BUSY}$ output. When this signal becomes a logic high, signaling the end of conversion, the processor reads the high byte of the conversion through PORTC. The low byte is read through PORTC when the processor changes the BYTE signal to a logic high. The timing relationship of the control signals and data are shown in Figure 17.

Sample Listing A

```
*************************************************************************
*                                                                       *
* This example program selects the an LTC1391 MUX channel, initiates a*
* conversion, and retrieves conversion data. It stores the 16-bit data*
* in two consecutive memory locations. The program is designed for use*
* with the LTC1605's /CS tied to ground (see timing diagram in        *
* Figure 17).                                                           *
*                                                                       *
*************************************************************************
*
**************************************
* 68HC11 register definitions             *
**************************************
*
PORTA  EQU    $1000  Parallel port A
*                   Use Bit0 as an input for the LTC1605's /BUSY signal
*                   Use Bit3 as an output driving the LTC1605's BYTE
*                   input
PIOC   EQU    $1002  Parallel I/O control register
*                   "STAF,STAI,CWOM,HNDS, OIN, PLS, EGA,INVB"
PORTC  EQU    $1003  Port C data register
*                   "Bit7,Bit6,Bit5,Bit4,Bit3,Bit2,Bit1,Bit0"
DDRC   EQU    $1007  Port D data direction register
*                   "Bit7,Bit6,Bit5,Bit4,Bit3,Bit2,Bit1,Bit0"
*                   1 = output, 0 = input
PORTD  EQU    $1008  Port D data register
*                   " -  , -  , SS* ,CSK ;MOSI,MISO,TxD ,RxD "
DDRD   EQU    $1009  Port D data direction register
SPCR   EQU    $1028  SPI control register
*                   "SPIE,SPE ,DWOM,MSTR;SPOL,CPHA,SPR1,SPR0"
SPSR   EQU    $1029  SPI status register
*                   "SPIF,WCOL, -  ,MODF; -  , -  , -  , -  "
SPDR   EQU    $102A  SPI data register; Read-Buffer; Write-Shifter
*
* RAM variables to hold the LTC1605's 14 conversion result
*
DIN1   EQU    $00    This memory location holds the LTC1605's bits 15 - 08
DIN2   EQU    $01    This memory location holds the LTC1605's bits 07 - 00
MUX    EQU    $02    This memory location holds the MUX address data
*
```

TYPICAL APPLICATIONS

```
****************************************
* Start GETDATA Routine                *
****************************************
*
       ORG    $C000  Program start location
INIT1  LDAA   #$03   0,0,0,0,0,0,1,1
*                   "STAF=0,STAI=0,CWOM=0,HNDS=0, OIN=0, PLS=0, EGA=1,INVB=1"
       STAA   PIOC   Ensures that the PIOC register's status is the same
*                   as after a reset, necessary of simple Port D manipulation
       LDAA   #$00   0,0,0,0,0,0,0,0
*                   "Bits 7 - 0 are used as inputs for the LTC1605's data
       STAA   DDRC   Direction of PortD's bit are now set as inputs
       LDAA   #$2F   -,-,1,0;1,1,1,1
*                   -, -, SS*-Hi, SCK-Lo, MOSI-Hi, MISO-Hi, X, X
       STAA   PORTD  Keeps SS* a logic high when DDRD, Bit5 is set
       LDAA   #$38   -,-,1,1;1,0,0,0
       STAA   DDRD   SS* , SCK, MOSI are configured as Outputs
*                   MISO, TxD, RxD  are configured as Inputs
* DDRD's Bit5 is a 1 so that port D's SS* pin is a general output
       LDAA   #$50
       STAA   SPCR   The SPI is configured as Master, CPHA = 0, CPOL = 0
*                   and the clock rate is E/2
*                   (This assumes an E-Clock frequency of 4MHz. For higher
*                   E-Clock frequencies, change the above value of $50 to a
*                   value that ensures the SCK frequency is 2MHz or less.)
GETDATAPSHX
       PSHY
       PSHA
*
****************************************
* Setup indecies                       *
****************************************
*
       LDX    #$0    The X register is used as a pointer to the memory
*                   locations that hold the conversion data
       LDY    #$1000
*
****************************************
* Ensure that a logic high is applied  *
* to the LTC1391's /CS and the         *
* LTC1605's R/C pins                   *
****************************************
*
       BSET   PORTD,Y %00100000    This sets the SS* output bit to a logic
*                                  high, ensuring that the LTC1391's CS*
*                                  input is a logic high while clocking
*                                  MUX address data into the LTC1391
       BSET   PORTA,Y %00010000    This sets the R/C* output bit to a logic
*                                  high, ensuring that the LTC1605's R/C*
*                                  input is a logic high before initiating
*                                  a conversion

****************************************
```

TYPICAL APPLICATIONS

```
* Retrieve the MUX address from memory    *
* and send it to the LTC1391       *
*************************************
*
       LDAA   MUX    Retrieve the MUX address from memory
       ORAA   #$08   Enable the selected MUX address
       STAA   SPDR   Select the MUX channel
WAIT1  LDAA   SPSR   This loop waits for the SPI to complete a serial
*                    transfer/exchange by reading the SPI Status Register
       BPL    WAIT1  The SPIF (SPI transfer complete flag) bit is the SPSR's
*                    MSB and is set to one at the end of an SPI transfer. The
*                    branch will occur while SPIF is a zero.
       BCLR   PORTD,Y %00100000    This forces a logic low on PORTD's SS*,
*                                  latching the MUXes data
*
*************************************
* Initiate a LTC1605 conversion           *
*************************************
*

       BCLR   PORTA,Y %00010000    Initiate a conversion
       BSET   PORTA,Y %00010000    This sets the LTC1605's R/C* to a logic
*                                  high
*
*************************************
* Set the LTC1605's BYTE input low to     *
* ensure that the high byte is present    *
* during the first read                   *
*************************************
*
       LDAA   PORTA         Get the contents of Port A
       ANDA   #%11110111    Set Bit3 low
       STAA   PORTA         Set the LTC1605's BYTE input low
*
*************************************
* The next short loop ensures that the  *
* LTC1605's conversion is finished *
* before starting the data transfer*
*************************************
*
CONVENDLDAA   PORTA         Retrieve the contents of port A
       ANDA   #%00000001    Look at Bit0
*                           Bit0 = Lo; the LTC1605's conversion is not
*                           complete
*                           Bit0 = Hi; the LTC1605's conversion is complete
       BEQ    CONVEND       Branch to the loop's beginning while Bit7
*                           remains low
*
```

TYPICAL APPLICATIONS

```
*************************************************************************
* This routine retrieves the LTC1605's 16-bit data using two 8-bit    *
* reads. The BYTE input is manipulated through Port A's Bit3. During  *
* the first read when BYTE is low, the upper byte is read and stored in      *
* DIN1.During the second read when BYTE is high, the lower byte is    *
* read and stored in DIN2.                                          *
*************************************************************************
*
       LDAA   PORTC  Retrieve the LTC1605's high byte
       STAA   DIN1   Store the high byte
       LDAA   PORTA  Get the contents of Port A
       ORAA   #%00001000    Set Bit3 high
       STAA   PORTA  Set the LTC1605's BYTE input high
       LDAA   PORTC  Retrieve the LTC1605's low byte
       STAA   DIN2   Store the high byte
       PULA          Restore the A register
       PULY          Restore the Y register
       PULX          Restore the X register
       RTS
```

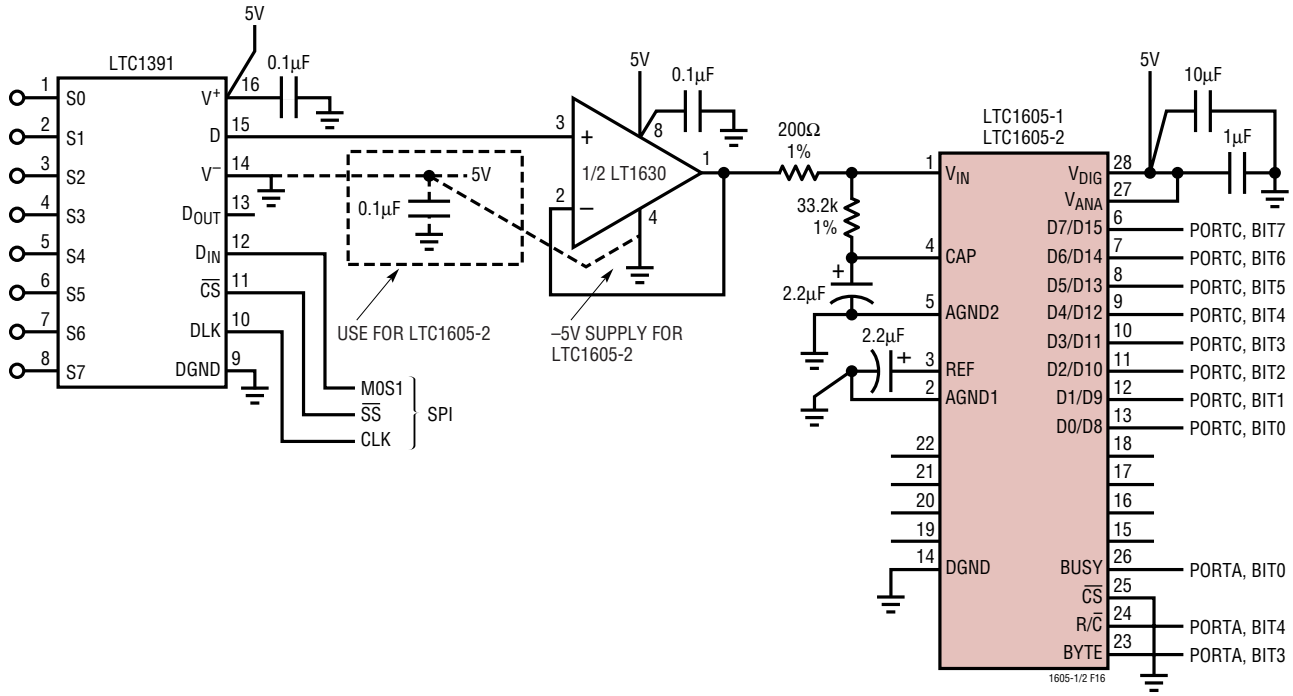
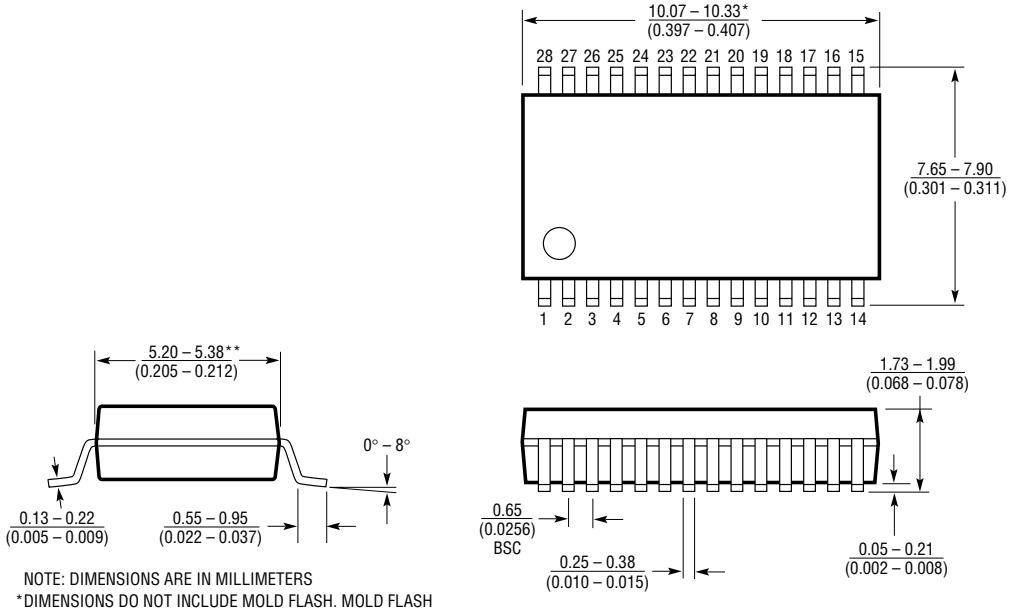


Figure 16. 8-Channel, 16-Bit Data Acquisition System with Interface to the 68HC11

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



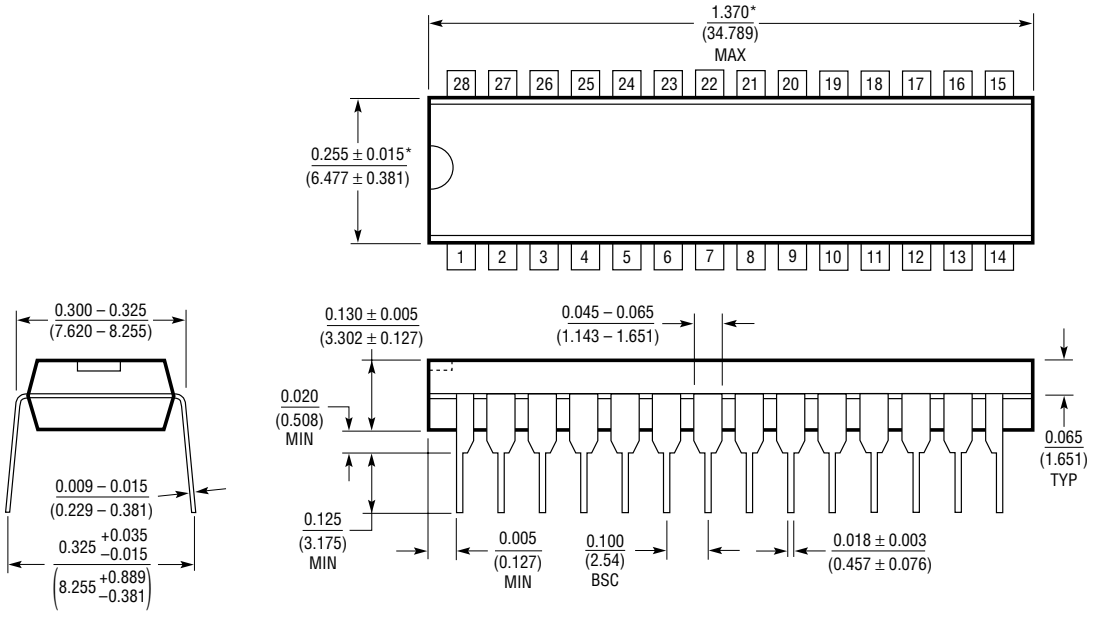
NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

G28 SSOP 1098

N Package
28-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N28 1098

TYPICAL APPLICATION

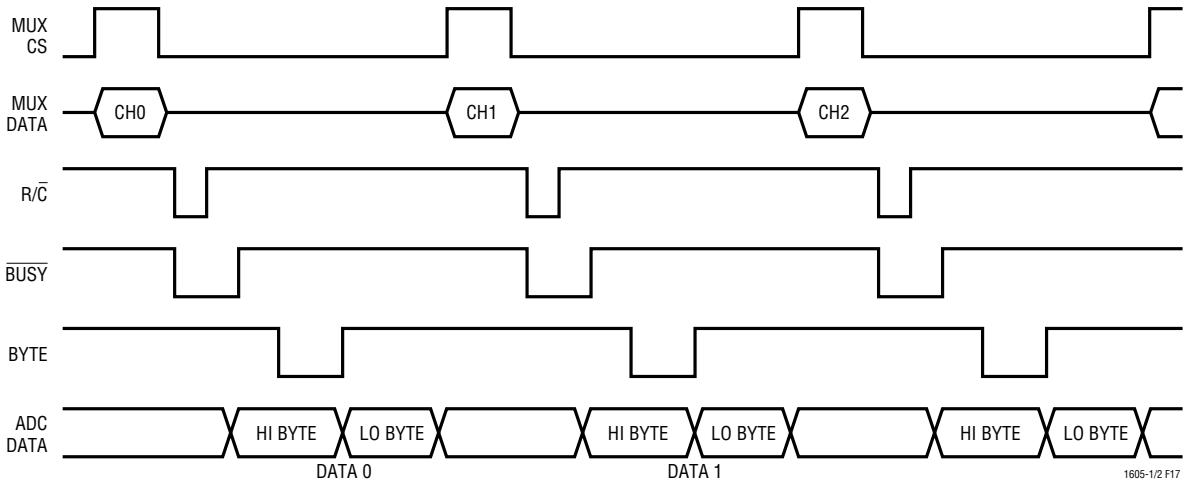


Figure 17. This Is the Timing Relationship Between the Selected MUX Channel, Its Conversion Data and the ADC and MUX Control Signals When Using the Sample Program In Listing 1. The Conversion Process Is Latency Free: the Data Is Always Generated Based On the Currently Selected MUX Input

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1019-2.5	Precision Bandgap Reference	0.05% Max, 5ppm/°C Max
LTC1274/LTC1277	Low Power 12-Bit, 100ksps ADCs	10mW Power Dissipation, Parallel/Byte Interface
LTC1415	Single 5V, 12-Bit, 1.25Msps ADC	55mW Power Dissipation, 72dB SINAD
LTC1419	Low Power 14-Bit, 800ksps ADC	True 14-Bit Linearity, 81.5dB SINAD, 150mW Dissipation
LT1460-2.5	Micropower Precision Series Reference	0.075% Max, 10ppm/°C Max, Only 130µA Supply Current
LTC1594/LTC1598	Micropower 4-/8-Channel 12-Bit ADCs	Serial I/O, 3V and 5V Versions
LTC1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, 90dB SINAD, 100dB THD
LTC1605	Low Power 100ksps 16-Bit ADC	Single 5V, ±10V Inputs

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