



Mosaic Semiconductor Inc.

PUMA 2U16001

PUMA 2U16001-15/17/20

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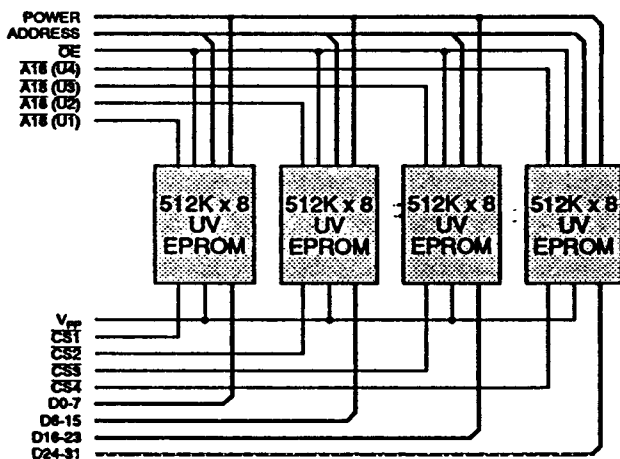
ADVANCE PRODUCT INFORMATION

16,777,216 bit CMOS High Speed Static RAM

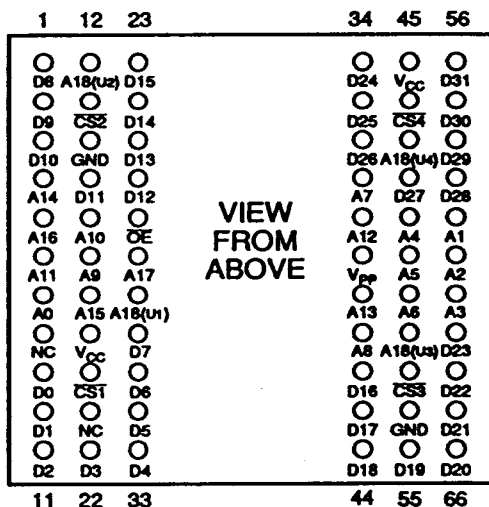
Features

- Fast Access times of 150/170/200 ns
- Pin grid array gives 2:1 improvement over DIL.
- Package Suitable for Thermal Ladder Applications.
- On board decoupling capacitors.
- Configurable as 8 / 16 / 32 bit wide.
- Operating Power 165 / 330 / 660 mW (max)
- Standby Power 2.2mW (max)
- V_{pp} Voltage of 13.0V±0.25V.
- Base components may be screened in accordance with MIL-STD-883.

Block Diagram



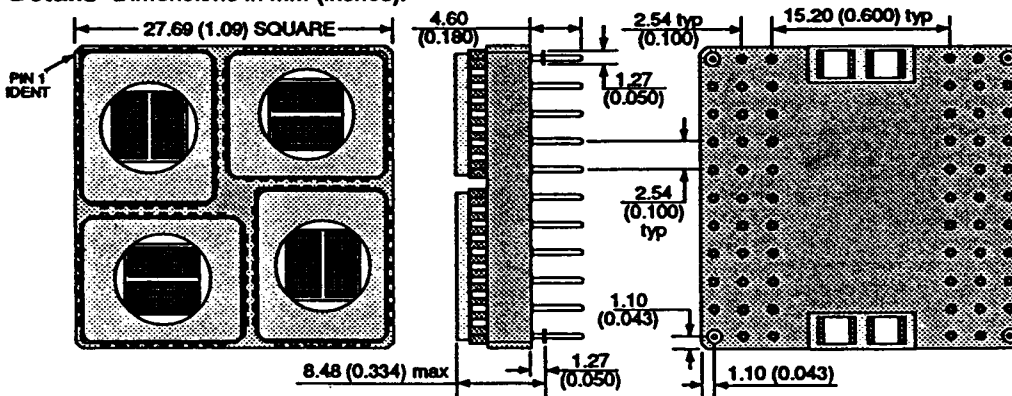
Pin Definition



Pin Functions

- A0 - A16 Address Inputs
- D0 - D31 Data Inputs/Outputs
- CS1-4 Chip Select
- OE Output Enable
- NC No Connect
- V_{pp} Programming Voltage
- V_{CC} Power (+5V)
- GND Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings ⁽¹⁾

Voltage on pins V_{PP} and A_8 ⁽²⁾	V_{TPP}	-2.0V to +14.0 V
Voltage on any other pins ⁽²⁾	V_T	-2.0V to +7.0 V
Storage Temperature	T_{STG}	-65 to +150 °C

Notes : (1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Minimum DC input voltage is -0.6V. During transitions inputs may undershoot to -2.0V for pulses less than 20 ns. Maximum DC voltage on output pins is $V_{CC}+0.75V$, which may overshoot to +7.0V for pulses less than 20 ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	$V_{CC}+0.75$	V
Input Low Voltage	V_{IL}	-0.6	-	0.8	V
Operating Temperature	T_A	0	-	70	°C (2U16001)
	T_{AI}	-40	-	85	°C (2U16001I)
	T_{AM}	-55	-	125	°C (2U16001M, MB)

Capacitance ($V_{CC}=5V\pm 10\%$, $f=1$ MHz, $T_A=25^\circ C$)

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance	Address, \overline{OE}	C_{NI} $V_N=0V$	16	32	pF
	$\overline{CS1-4}$	C_{N2} $V_N=0V$	4	8	pF
I/O Capacitance	32 Bit Mode	C_{IO} $V_{IO}=0V$	8	12	pF

Note: These parameters are calculated and not measured.

AC Test Conditions

- *Input pulse levels: 0.45V to 2.4V
- *Input rise and fall times: 20 ns
- *Input and Output timing reference levels: 0.8V to 2.0V
- *Output load: 1 TTL gate + 100pF
- * $V_{CC}=5V\pm 10\%$

Operating Modes

This table shows the inputs required to control the operating modes of the EPROMs on the PUMA 2U16001.

MODE	\overline{CS}	\overline{OE}	A_0	A_9	V_{PP}	OUTPUTS	
Read	V_L	V_L	X	X	X	D_{OUT}	
Output Disable	X	V_H	X	X	X	High Z	
Standby	V_H	X	X	X	X	High Z	
Program	V_L	V_H	X	X	V_{PP}	D_{IN}	
Program Verify	X	V_L	X	X	V_{PP}	D_{OUT}	
Program Inhibit	V_H	V_H	X	X	V_{PP}	High Z	
Identifier (NOTE 1)	Manufacturer	V_L	V_L	V_L	V_H	X	$1E_H$
	Device Code	V_L	V_L	V_H	V_H	X	$0B_H$

$V_H=12.0V\pm 0.5V$
 $X=V_H$ or V_L

- Notes: (1) $A1 - A8 = A10 - A16 = V_L$
 (2) \overline{CS} is accessed through $\overline{CS1-4}$. For correct operation, $\overline{CS1-4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation.
 (3) The PUMA 2U16001 module is based on ATMEL AT27C040 devices.

DC Electrical Characteristics for Read Operation ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

Parameter	Symbol	Test Condition	min	max	Unit
Input Leakage Current Address, $\overline{\text{OE}}$	I_{L1}	$V_{IN} = -0.1\text{V}$ to $V_{CC} + 1\text{V}$	-	20	μA
	Other Pins	$V_{IN} = -0.1\text{V}$ to $V_{CC} + 1\text{V}$	-	5	μA
Output Leakage Current	I_{LO}	$V_{OUT} = -0.1\text{V}$ to $V_{CC} + 0.1\text{V}$, 8 bit	-	40	μA
V_{PP} Read Current ^(1,2)	I_{PP1}	$V_{PP} = 3.8\text{V}$ to $V_{CC} + 0.3\text{V}$	-	40	μA
V_{CC} Operating Supply Current ⁽⁴⁾	32 bit ⁽⁴⁾	$\overline{\text{CS}} = V_{IL}$, $I_{OUT} = 0\text{mA}$, $f = 5\text{MHz}$	-	120	mA
	16 bit	As above	-	60	mA
	8 bit	As above	-	30	mA
Standby Supply Current TTL levels ⁽¹⁾	I_{SB1}	$\overline{\text{CS}} = 2.0\text{V}$ to $V_{CC} + 1.0\text{V}$	-	4	mA
	CMOS levels ⁽¹⁾	$\overline{\text{CS}} = V_{CC} - 0.3\text{V}$ to $V_{CC} + 1.0\text{V}$	-	400	μA
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	V

- Notes: (1) V_{CC} must be applied simultaneously or before V_{PP} , and removed simultaneously or after V_{PP} .
 (2) V_{PP} may be connected directly to V_{CC} , except during programming. The supply current is the sum of I_{CC} and I_{PP} .
 (3) **CAUTION:** the PUMA 2U16001 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.
 (4) $\overline{\text{CS}}$ above are accessed through $\overline{\text{CS}}1-4$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

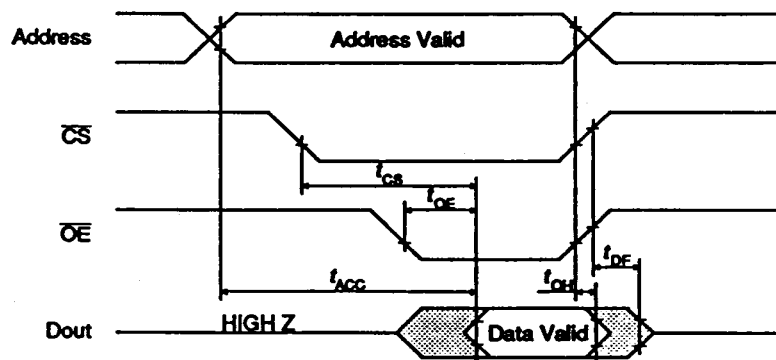
Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-15		-17		-20		Unit	Notes
		min	max	min	max	min	max		
Address to Output Delay	t_{ACC}	-	150	-	170	-	200	ns	3
Chip Select Access Time	t_{CS}	-	150	-	170	-	200	ns	2
Output Enable to Output Valid	t_{OE}	-	40	-	65	-	75	ns	2,3
Chip Deselect to O/P high Z	t_{DF}	-	40	-	50	-	55	ns	4,5
Output Hold from Address Change	t_{OH}	-	0	-	0	-	0	ns	

Notes: See AC Characteristics Notes.

Read Cycle Timing Waveform (1)



Notes: See AC Characteristics Notes.

DC Programming Characteristics ($V_{CC}=6.5V\pm 0.25V, V_{PP}=13.0V\pm 0.25V, T_A=25^\circ C\pm 5^\circ C$)

Parameter	Symbol	Test Condition	min	max	Unit
Input Leakage Current	Address, \overline{OE}	I_{L1} $V_{IN}=V_{IL}, V_{IH}$	-	40	μA
	Other Pins	I_{L2} $V_{IN}=V_{IL}, V_{IH}$	-	10	μA
V_{PP} Program Current	32 bit	I_{PP32} Program, $\overline{CS}=V_{IL}$	-	80	mA
	16 bit	I_{PP16} As above	-	40	mA
	8 bit	I_{PP8} As above	-	20	mA
V_{CC} Operating Supply Current	32 bit	I_{CC32} Program and Verify	-	160	mA
	16 bit	I_{CC16} As above	-	80	mA
	8 bit	I_{CC8} As above	-	40	mA
Identifier Select Voltage	V_H		11.5	12.5	V
Input Low Level	V_{IL}	(All inputs)	-0.6	0.8	V
Input High Level	V_{IH}		2.0	$V_{CC}+0.7$	V
Output Low Voltage	V_{OL}	$I_{OL}=2.1mA$	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH}=-400\mu A$	2.4	-	V

- Notes: (1) \overline{CS} above are accessed through $\overline{CS1-4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.
 (2) Programming characteristics are sampled but not 100% tested at worst case conditions.

AC Programming Characteristics (1)

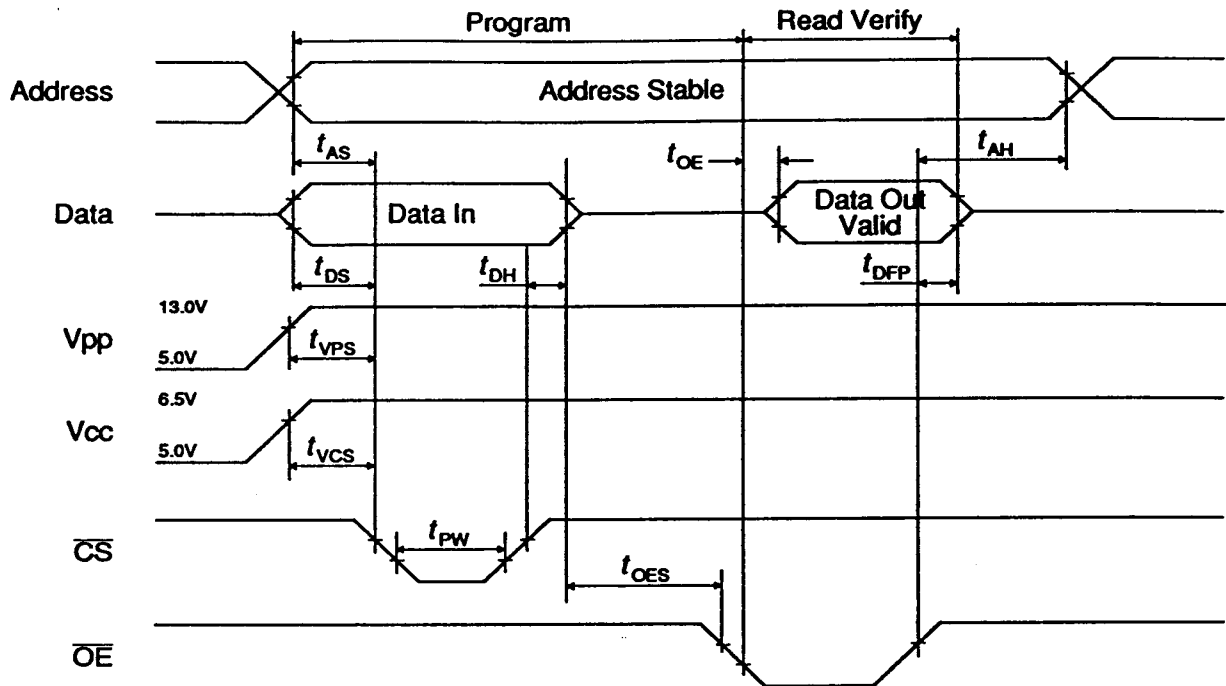
Parameter	Symbol	min	typ	max	Unit	Notes
Address Setup Time	t_{AS}	2	-	-	μs	
Output Enable Setup Time	t_{OES}	2	-	-	μs	
Data Setup Time	t_{DS}	2	-	-	μs	
Address Hold Time	t_{AH}	0	-	-	μs	
Data Hold Time	t_{DH}	2	-	-	μs	
Output Enable High to Output Float Delay	t_{DFP}	0	-	130	ns	2
V_{PP} Setup Time	t_{VPS}	2	-	-	μs	
Initial Program Pulse Width	t_{PW}	95	-	105	μs	3
V_{CC} Setup Time	t_{VCS}	2	-	-	μs	
Chip Select Setup Time	t_{CES}	2	-	-	μs	
Data Valid from Output Enable	t_{OE}	-	-	150	ns	2

- Notes: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 (2) This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven - see timing diagram.
 (3) Program Pulse width tolerance is $100\mu s \pm 5\%$.

AC Characteristics Notes

- (1) Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
- (2) \overline{OE} may be delayed up to $t_{CS}-t_{OE}$ after the falling edge of \overline{CS} without impact on t_{CS} .
- (3) \overline{OE} may be delayed up to $t_{ACC}-t_{OE}$ after the address is valid without impact on t_{ACC} .
- (4) This parameter is only sampled and is not 100% tested.
- (5) Output float is defined as the point when data is no longer driven.

Programming Cycle Timing Waveform (1)



- Notes:
- (1) The Input Timing Reference is 0.8V for V_L and 2.0V for V_{HT} .
 - (2) t_{OE} and t_{DFF} are characteristics of the device but must be accommodated by the programmer.
 - (3) When programming the PUMA2U16001 a 0.1 μ F capacitor is required across V_{PP} and ground to suppress spurious voltage transients.
-

High Performance Programming Algorithm

The PUMA2U16001 can be programmed using the algorithm shown here. This allows faster programming times without stressing the device or causing deterioration in Data Retention Time. Each of the four devices used on this module is an ATMEL AT27C040; this information, together with the device identifier code, should allow the correct programming algorithm to be selected automatically.

Although the flow chart specifically refers to a single EPROM, all four devices on the PUMA tile can be programmed simultaneously in 32 bit mode, in pairs in 16 bit mode or singly in 8 bit mode. Obviously 32 bit mode is potentially the fastest programming time, but this makes greater demands on the V_{PP} Supply Current as shown on the Programming Operation DC Characteristics on page 4.

Programming

Upon delivery, or after each erasure, the PUMA 2U16001 has all 16,777,216 bits in the ONE or HIGH state. ZEROS are loaded into the devices through the procedure of programming.

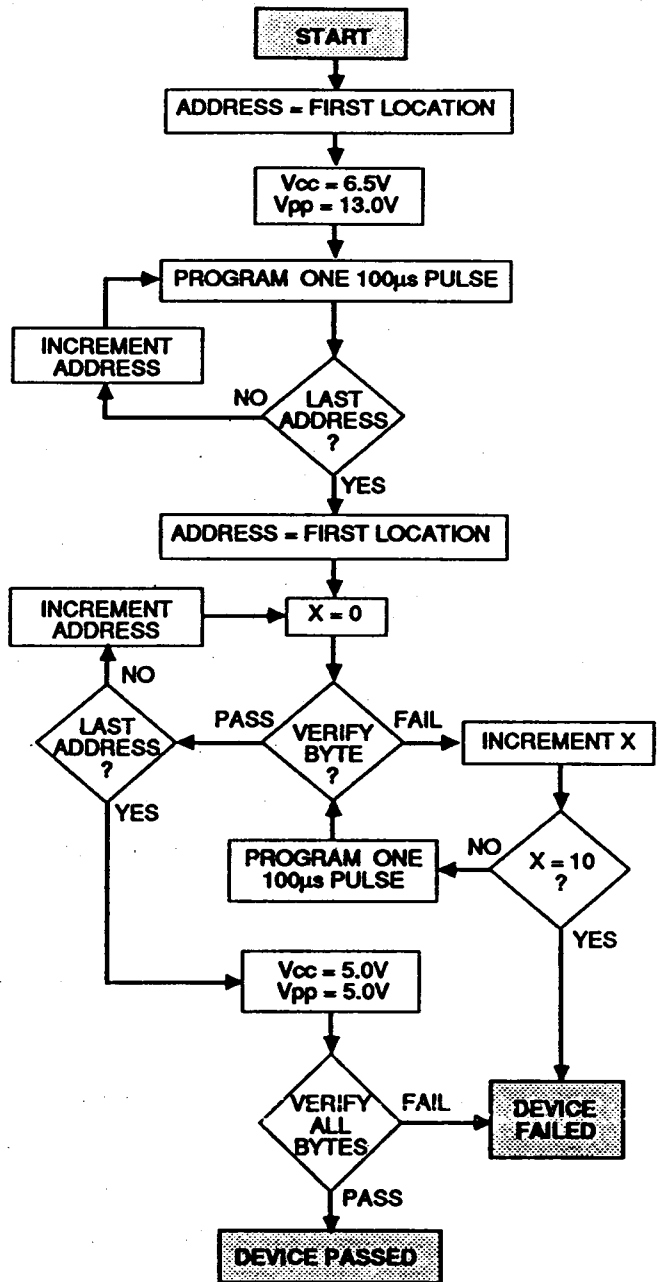
This mode is entered when 13.0V is applied to the V_{PP} pin, V_{CC} is raised to 6.5V, \overline{CS} is at V_L and \overline{OE} is at V_{HI} , as shown on the Table on page 2. Data may be applied in 8, 16 or 32 bits in parallel depending on how $\overline{CS}1-4$.

The algorithm reduces programming time by initially programming all locations with 100µs pulses without verification. Subsequently a verification/reprogramming loop is executed for each address. If the data does not verify, up to 10 such loops can be used, after which, if verification fails, programming stops. This process is repeated for each memory location within the PUMA 2U16001.

This algorithm programs at $V_{CC}=6.5V$ in order to ensure that each EPROM bit is programmed to a sufficiently high threshold voltage. After programming is complete, all bytes are compared with the original data with $V_{CC}=5.0V \pm 10\%$.

In order to overcome the voltage drop caused by the inductive effects of the printed circuit board on which the PUMA 2U16001 module is used, it is recommended that a 4.7µF electrolytic capacitor is used between V_{CC} and GND for every two PUMA modules. This capacitor should be placed close to the point where the power supply is routed to the UV EPROM array.

PROGRAMMING ALGORITHM



NOTE: THE ALGORITHM SHOWN HERE MUST BE USED TO ENSURE CORRECT PROGRAMMING OF THE PUMA 2U16001. THIS MAXIMIZES THE DATA RETENTION TIME OF THE UV EPROMS AND DOES NOT STRESS THE MEMORY CELL.

DEVICE IDENTIFIER MODE

The device identifier mode allows the reading out of a binary code from an EPROM which identify its manufacturer and specific type. It is intended to be used to automatically match the device to be programmed with the correct algorithm. This mode operates over the $25^{\circ}\text{C}\pm 5^{\circ}\text{C}$ temperature range.

In order to activate this mode $12.0\text{V}\pm 0.5\text{V}$ must be placed onto address line A9, after which two identifier bytes may be read by toggling A0 from V_L to V_H . All other address lines are held at V_L during this sequence.

The manufacturer code is accessed with $A0=V_L$ and the device code with $A0=V_H$; the values for these codes are given in the Operating Mode Table on page 2. Note that all identifiers for manufacturer and device codes will possess odd parity, with D7 defined as the parity bit.

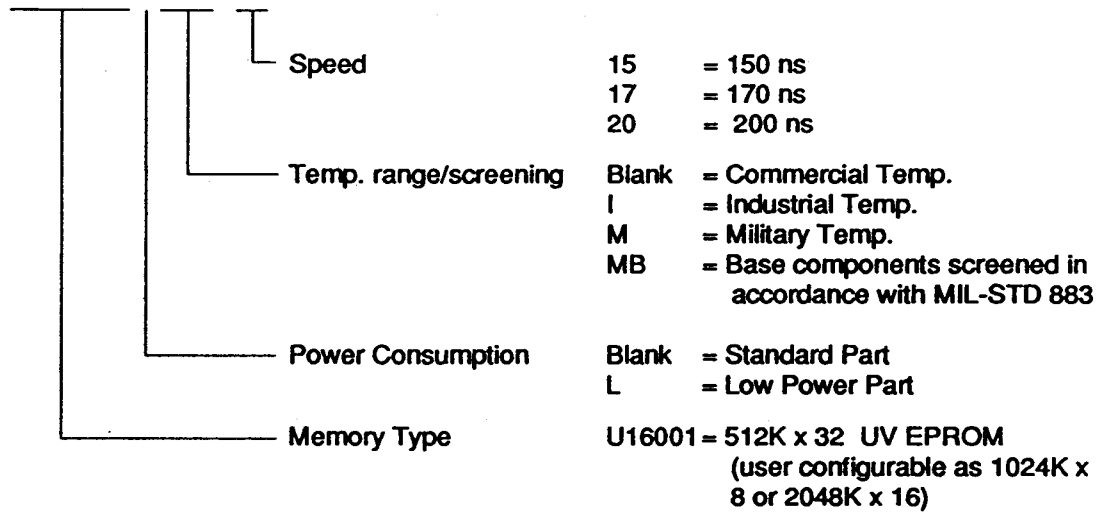
ERASE

Complete erasure of the devices used on the PUMA 2U16001 is performed by exposure to an ultraviolet light source giving a dosage of $15\text{WS}/\text{cm}^2$. This dosage can be obtained by using an ultraviolet lamp with a wavelength of 2537 \AA at a minimum intensity of $12,000\mu\text{W}/\text{cm}^2$, for approximately 15 - 20 minutes. The PUMA 2U16001 should be directly under and about 1 inch from the light source.

Note that sunlight and fluorescent light may contain sufficient ultraviolet light to erase the programmed information. Although erasure times will be much longer at these levels, the transparent lids on this module should be covered with an opaque label to provide maximum system reliability.

Ordering Information

PUMA 2U16001LMB-15



The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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