TEMIC´s TSC87C51 is high performance CMOS EPROM version of the 80C51 CMOS single chip 8 bit microcontroller.

The fully static design of the TSC87C51 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The TSC87C51 retains all the features of the 80C51 with some enhancement: 4 K bytes of internal code memory (EPROM); 128 bytes of internal data memory (RAM); 32 I/O lines; two 16 bit timers; a 5-source, 2-level interrupt structure; a full duplex serial port with framing

error detection; a power off flag; and an on-chip oscillator.

The TSC87C51 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the RAM, the timers, the serial port and the interrupt system continue to function. In the power down mode the RAM is saved and all other functions are inoperative.

The TSC87C51 is manufactured using non volatile SCMOS process which allows it to run up to:

- 25 MHz with VCC = 5 V ± 10%.

Features

- 4 Kbytes of EPROM
  - Improved Quick Pulse programming algorithm
  - Secret ROM by encryption
- 128 bytes of RAM
- 64 Kbytes program memory space
- 64 Kbytes data memory space
- 32 programmable I/O lines
- Two 16 bit timer/counters
- Programmable serial port with framing error detection
- Power control modes

- Two–level interrupt priority
- Fully static design
- 0.8μ SCMOS non volatile process
- ONCE Mode
- Enhanced Hooks system for emulation purpose
- Military temperature ranges (–55ºC to + 125ºC)
- Available packages:
  - CDIL40 (OTP)
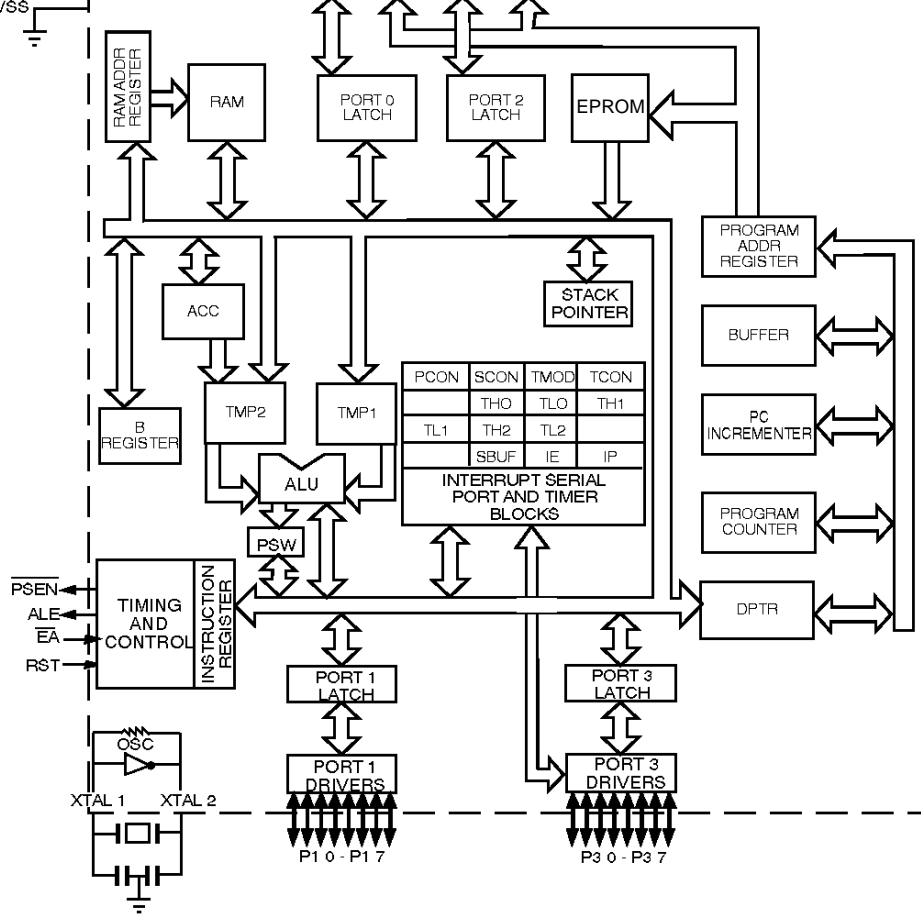 - CDIL40 (UV erasable)
  - CQPJ44 (OTP)
  - CQPJ44 (UV erasable)

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Figure 1 TSC87C51 Block diagram

CDIL

Left	Pin	Pin	Right
P1.2	3	38	P0.1
P1.3	4	37	P0.2
P1.4	5	36	P0.3
P1.5	6	35	P0.4
P1.6	7	34	P0.5
P1.7	8	33	P0.6
RST	9	32	P0.7
P3.0/RxD	10	31	$\overline{EA}$/VPP
P3.1/TxD	11	30	ALE/$\overline{PROG}$
P3.2/$\overline{INT0}$	12	29	$\overline{PSEN}$
P3.3/$\overline{INT1}$	13	28	P2.7
P3.4/T0	14	27	P2.6
P3.5/T1	15	26	P2.5
P3.6/$\overline{WR}$	16	25	P2.4
P3.7/RD	17	24	P2.3
XTAL2	18	23	P2.2
XTAL1	19	22	P2.1
VSS	20	21	P2.0

CQPJ

Left	Pin	Pin	Right
P1.5	7	39	P0.4/AD4
P1.6	8	38	P0.5/AD5
P1.7	9	37	P0.6/AD6
RST	10	36	P0.7/AD7
P3.0/RxD	11	35	$\overline{EA}$/VPP
Reserved	12	34	Reserved
P3.1/TxD	13	33	ALE/$\overline{PROG}$
P3.2/$\overline{INT0}$	14	32	$\overline{PSEN}$
P3.3/$\overline{INT1}$	15	31	P2.7/A15
P3.4/T0	16	30	P2.6/A14
P3.5/T1	17	29	P2.5/A13

18 19 20 21 22 23 24 25 26 27 28

P3.6/$\overline{WR}$ | P3.7/$\overline{RD}$ | XTAL2 | XTAL1 | VSS | Reserved | P2.0/A8 | P2.1/A9 | P2.2/A10 | P2.3/A11 | P2.4/A12
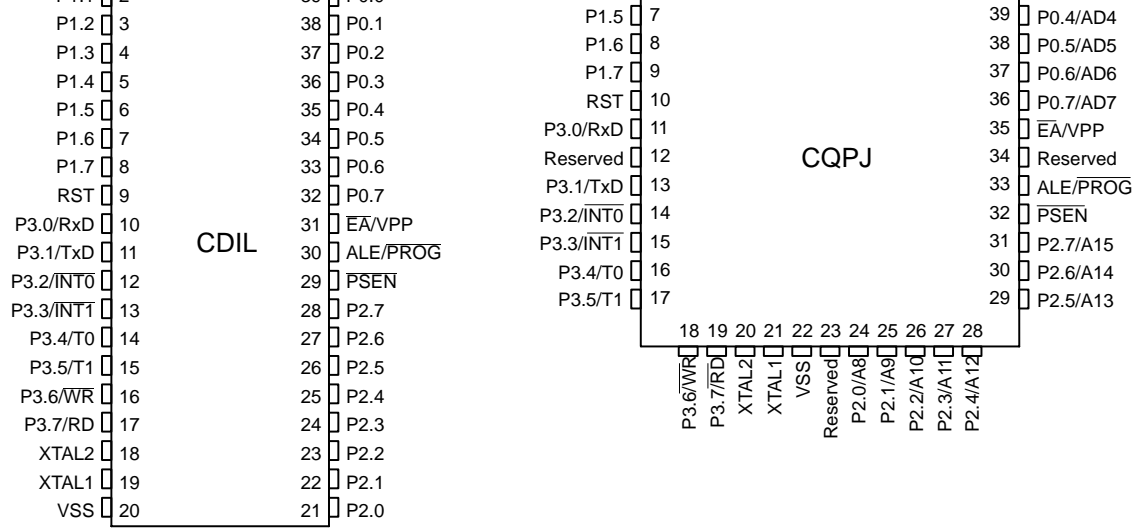
Figure 2 TSC87C51 pin configuration

Do not connect Reserved pins.

VSS1

Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by–passing.
Note: This pin is not a substitute for the VSS pin. Connection is not necessary for proper operation.

VCC

Supply voltage during normal, Idle, and Power Down operation.

Port 0

Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's.

Port 0 can sink eight LS TTL inputs.

Port 0 is used as data bus during EPROM programming and program verification.

Port 1

Port 1 is an 8 bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, in the DC parameters section) because of the internal pullups.

Port 1 can sink/ source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 1 receives the low–order address byte during EPROM programming and program verification.

Port 2

Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL, in the DC parameters section) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16 bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Some Port 2 pins receive the high–order address bits and control signals during EPROM programming and program verification.

Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL, in the DC parameters section) because of the pullups.

P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	$\overline{RD}$ (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Some Port 3 pins receive control signals during EPROM programming and program verification.

RST

A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{CC}. The port pins will be driven to their reset condition when a minimum VIH1 voltage is applied whether the oscillator is started or not (asynchronous reset).

ALE/$\overline{PROG}$

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped.

ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without external pullup.

If desired, to reduce EMI, ALE operation can be disabled by setting bit 0 of SFR location 8Eh (MSCON). With this bit set, the pin is weakly pulled high. However, ALE remains active during MOVX, MOVC instructions and external fetches. Setting the ALE disable bit has no effect if the microcontroller is in external execution mode ($\overline{EA}=0$).

Throughout the remainder of this datasheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$

Program Store Enable output is the read strobe to external Program Memory. $\overline{PSEN}$ is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of $\overline{PSEN}$ are skipped during each access to external Data Memory). $\overline{PSEN}$ is not activated during fetches from internal Program Memory. $\overline{PSEN}$ can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{EA}$/VPP

External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000h to FFFFh. Note however, that if any of the Security bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to VCC for internal program execution.

This pin also receives the programming supply voltage (VPP) during EPROM programming.

XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2

Output from the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

The Power Off Flag allows the user to distinguish between a 'cold start' reset and a 'warm start' reset.

A cold start reset is one that is coincident with VCC being turned on to the device after it was turned off. A warm start reset occurs while VCC is still applied to the device and could be generated for example by an exit from Power Down.

The Power Off Flag (POF) is located in PCON at bit location 4 (see Table 1). POF is set by hardware when VCC rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

Table 1 PCON – Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL

Symbol	Description
SMOD1	**Serial Port Mode bit 1**, **new name of SMOD bit** Set to select double baud rate in mode 1,2 or 3.
SMOD0	**Serial Port Mode bit 0** Set to to select FE bit in SCON. Clear to select SM0 bit in SCON.
–	**Reserved** Do not write 1 in this bit.
POF	**Power Off Flag** Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software. Clear by software to recognize next reset type.
GF1	**General purpose Flag** Set by software for general purpose usage. Clear by software for general purpose usage.
GF0	**General purpose Flag** Set by software for general purpose usage. Clear by software for general purpose usage.
PD	**Power Down mode bit** Set to enter power down mode. Clear by hardware when reset occurs.
IDL	**Idle mode bit** Set to enter idle mode. Clear by hardware when interrupt or reset occur.

The reset value of PCON is 00XX 0000b.

ONCE Mode

The ONCE mode facilitates testing and debugging of systems using TSC87C51 without the TSC87C51 having to be removed from the circuit. The ONCE mode is invoked by driving certain pins of the TSC87C51, the following sequence must be exercised.

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.

- Hold ALE low as RST is deactivated.

While the TSC87C51 is in ONCE mode, an emulator or test CPU can be used to drive the circuit. Table 2 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

ALE Disabling

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal should be disabled by setting AO bit.

The AO bit is located in MSCON at bit location 0 (see Table 3). As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 3 MSCON – Miscellaneous Control Register (8Eh)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	AO

Symbol	Description
–	**Reserved** Do not write 1 in these bits.
AO	**ALE Output bit** Set to disable ALE operation during internal fetches. Clear to restore ALE operation during internal fetches.

The reset value of MSCON is XXXX XXX0b.

UART

The UART in the TSC87C51 operates identically to the UART in the 80C51 but includes the following enhancement. For a complete understanding of the TSC87C51 UART please refer to the description in the 80C51 Hardware Description Guide.

Framing Error Detection

Framing error detection allows the serial port to check for missing stop bits in the communication in mode 1, 2 or 3. A missing stop bit can be caused for example by noise on the serial lines or transmission by two CPUs simultaneously.

If a stop bit is missing a Framing Error bit (FE) is set. The FE bit can be checked in software after each reception to detect communication errors. Once set, the FE bit must be cleared in software. A valid stop bit will not clear FE.

The FE bit is located in SCON at bit location 7. It shares the same bit location as SM0 (see Table 4). The new control bit SMOD0 in PCON (see Table 1) determines whether the SM0 or FE bit is accessed (see Figure 3), so whether the framing error detection is enabled or not. If SMOD0 is set then SCON.7 functions as FE, if SMOD0 is cleared then SCON.7 functions as SM0. Once set, the FE bit must be cleared by software. A valid stop bit will not clear FE. When UART is in mode 1 (8–bit mode), RI flag is set during stop bit whether or not framing error is enabled (see Figure 4). When in mode 2 and 3 (9–bit mode), RI flag is set during stop bit if framing error is enabled or during ninth bit if not (see Figure 5).

To UART framing error control

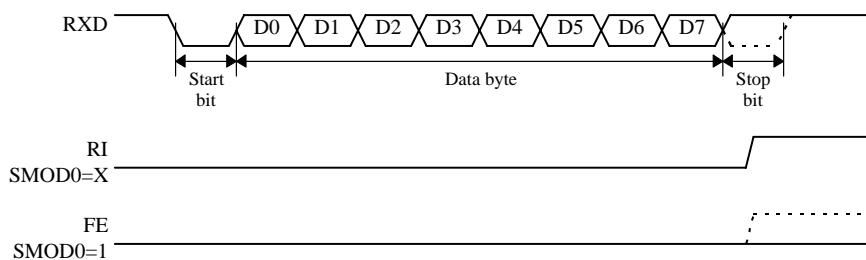**Figure 3 Framing error block diagram**

RXD

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |

Start bit   Data byte   Stop bit

RI
SMOD0=X

FE
SMOD0=1

Figure 4 Enhanced UART timing diagram in mode 1

RXD

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 |

Start bit   Data byte   Ninth bit   Stop bit

RI
SMOD0=0

RI
SMOD0=1

FE
SMOD0=1
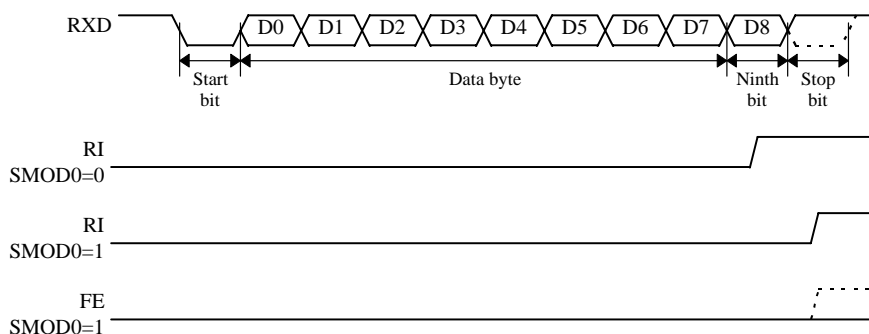
Figure 5 Enhanced UART timing diagram in mode 2 and 3

Table 4 SCON – Serial Control Register (98h)

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Symbol	Description
FE	**Framing Error bit (SMOD0 bit set)** Set by hardware when an invalid stop bit is detected. Clear to reset the error state, not cleared by a valid stop bit.
SM0	**Serial Mode bit 0 (SMOD0 bit cleared)** Used with SM1 to select serial mode.
SM1	**Serial Mode bit 1** Used with SM0 to select serial mode.
SM2	**Multiprocessor Communication Enable bit** Set to enable multiprocessor communication feature in mode 2 and 3. Clear to disable multiprocessor communication feature.
REN	**Serial Reception Enable bit** Set to enable serial reception. Clear to disable serial reception.

TI	**Transmit Interrupt Flag** Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes. Clear to acknowledge interrupt.	
RI	**Receive Interrupt Flag** Set by hardware at the end of the 8th bit time in mode 0, see Figure 4 and Figure 5 in the other modes. Clear to acknowledge interrupt.	

The reset value of SCON is 0000 0000b.

- the code array: 4 Kbytes.
- the encryption array: 64 bytes.

In addition a third non programmable array is implemented:

- the signature array: 4 bytes.

EPROM Lock System

The program Lock system, when programmed, protects the on–chip program against software piracy.

Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all 1's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive–NOR'ed (XNOR) with the code byte, creating an encryption verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

EPROM Programming

Set–up modes

In order to program and verify the EPROM or to read the signature bytes, the TSC87C51 is placed in specific set–up modes (see Figure 6).

Control and program signals must be held at the levels indicated in Table 5.

Definition of terms

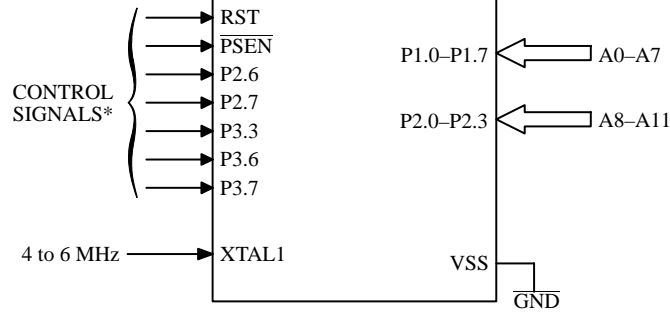**Address Lines:**   P1.0–P1.7, P2.0–P2.3 respectively for A0–A11

Data Lines: P0.0–P0.7 for D0–D7

Control Signals: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7.

Program Signals: ALE/$\overline{PROG}$, $\overline{EA}$/VPP.

Table 5 EPROM Set–up Modes

Mode	RST	$\overline{PSEN}$	ALE/ $\overline{PROG}$	$\overline{EA}$/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0	⊓⊔⊓	12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0	⊔⊓	0	1	1
Program Encryption Array Address 0–3Fh	1	0	⊓⊔⊓	12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0	⊔⊓	0	0	0

CONTROL SIGNALS*	RST
	$\overline{PSEN}$
	P2.6
	P2.7
	P3.3
	P3.6
	P3.7

4 to 6 MHz → XTAL1

P1.0–P1.7 ⇐ A0–A7

P2.0–P2.3 ⇐ A8–A11

VSS → $\overline{GND}$

* See Table 5 for proper value on these inputs

Figure 6 Set–up modes configuration

Programming algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 5.

To program the TSC87C51 the following sequence must be exercised:

● Step 1: Input the valid address on the address lines.

● Step 2: Input the appropriate data on the data lines.

● Step 3: Activate the combination of control signals.

● Step 4: Raise $\overline{EA}$/VPP from VCC to VPP (typical 12.75V).

● Step 5: Pulse ALE/$\overline{PROG}$ 5 times.

Repeat step 1 through 5 changing the address and data for the entire array or until the end of the object file is reached (see Figure 7).

Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TSC87C51.

To verify the TSC87C51 code the following sequence must be exercised :

● Step 1: Activate the combination of program signals.

● Step 2: Input the valid address on the address lines.

● Step 3: Input the appropriate data on the data lines.

● Step 4: Activate the combination of control signals.

Repeat step 2 through 4 changing the address and data for the entire array (see Figure 7).

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.
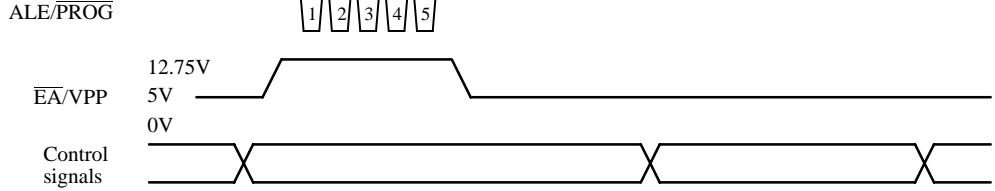
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Figure 7 Programming and verification signal's waveform

Signature bytes

The TSC87C51 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 5 for Read Signature Bytes. Table 6 shows the content of the signature byte for the TSC87C51.

Table 6 Signature bytes content

Location	Contents	Comment
30h	58h	Customer selection byte: TEMIC
31h	58h	Family selection byte: C51
60h	9Eh	TSC87C51
61h	XXh	Product revision number

EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array and also the encryption array returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state.

Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W–sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 25 mm, should be sufficient.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room–level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

Voltage on VCC to VSS . . . . –0.5 V to + 6.5 V
Voltage on VPP to VSS . . . . –0.5 V to + 13 V
Voltage on Any Pin to VSS . . . –0.5 V to VCC + 0.5 V
Power Dissipation . . . . 1 W[2]

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Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
VIL	Input Low Voltage	−0.5		0.2 VCC − 0.1	V	
VIH	Input High Voltage except XTAL1, RST	0.2 VCC + 1.2 (military)		VCC + 0.5	V	
VIH1	Input High Voltage, XTAL1, RST	0.7 VCC		VCC + 0.5	V	
VOL	Output Low Voltage, ports 1, 2, 3 [6]			0.3	V	IOL = 100μA[4]
				0.45	V	IOL = 1.6mA[4]
				1.0	V	IOL = 3.5mA[4]
VOL1	Output Low Voltage, port 0, ALE, $\overline{PSEN}$ [6]			0.3	V	IOL = 200μA[4]
				0.45	V	IOL = 3.2mA[4]
				1.0	V	IOL = 7.0mA[4]
VOH	Output High Voltage, ports 1, 2, 3	VCC − 0.3			V	IOH = −10μA
		VCC − 0.7			V	IOH = −30μA
		VCC − 1.5			V	IOH = −60μA
						VCC = 5V ± 10%
VOH1	Output High Voltage, port 0, ALE, $\overline{PSEN}$	VCC − 0.3			V	IOH = −200μA
		VCC − 0.7			V	IOH = −3.2mA
		VCC − 1.5			V	IOH = −7.0mA
						VCC = 5V ± 10%
RRST	RST Pulldown Resistor	50	90 [5]	200	kΩ	
IIL	Logical 0 Input Current ports 1, 2 and 3			−50	μA	Vin = 0.45V
ILI	Input Leakage Current			±10	μA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current, ports 1, 2, 3			−650	μA	Vin = 2.0V
CIO	Capacitance of I/O Buffer			10	pF	fc = 1MHz, TA = 25°C
IPD	Power Down Current		10 [5]	50	μA	VCC = 2.0V to 5.5V[3]
ICC	Power Supply Current [7]					
	Freq = 1 MHz Icc op			1.8	mA	VCC = 5.5V[1]
	Icc idle			1	mA	
	Freq = 6 MHz Icc op			10	mA	VCC = 5.5V[2]
	Icc idle			4	mA	
	Freq ≥ 12 MHz		[5]			
	Icc op = 1.25 Freq (MHz) + 5 mA		20@12MHz 40@25MHz		mA	
	Icc idle = 0.36 Freq (MHz) + 2.7 mA		8@12MHz 13@25MHz		mA	
	Icc idle = 0.4 Freq (MHz) + 2.7 mA (military)					

Notes for DC Electrical Characteristics

1. Operating ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns (see Figure 11), VIL = VSS + 0.5V, VIH = VCC − 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = VCC. ICC would be slightly higher if a crystal oscillator used (see NO TAG).

2. Idle ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5ns, VIL = VSS + 0.5V, VIH = VCC–0.5V; XTAL2 N.C; Port 0 = VCC; $\overline{EA}$ = RST = VSS (see Figure 9).

3. Power Down ICC is measured with all output pins disconnected; $\overline{EA}$ = VSS, PORT 0 = VCC; XTAL2 NC.; RST = VSS (see NO TAG).

4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst

14

Maximum total IOL for all output pins: 71 mA

If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

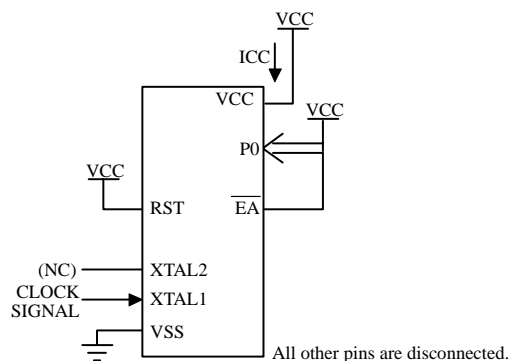7. For other values, please contact your sales office.
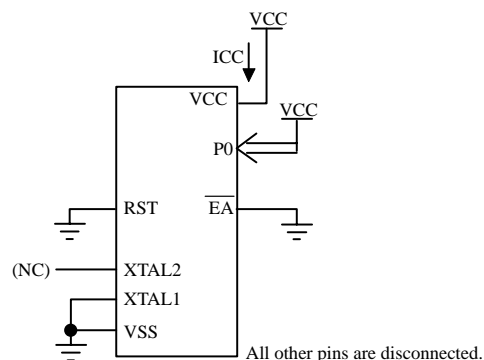
Figure 8 ICC Test Condition, Active Mode

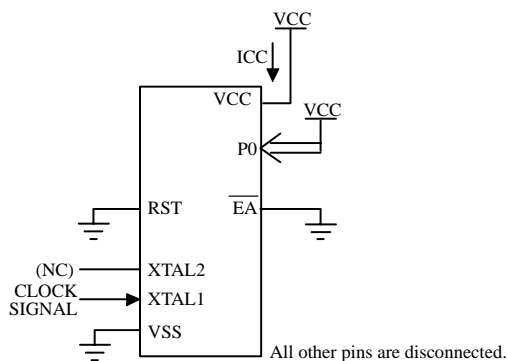**Figure 10 ICC Test Condition, Power Down Mode**
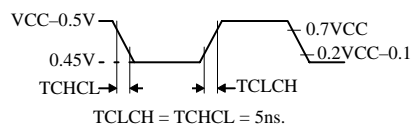
Figure 9 ICC Test Condition, Idle Mode

$TCLCH = TCHCL = 5ns.$

Figure 11 Clock Signal Waveform for ICC Tests in Active and Idle Modes

Example: TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{\text{PSEN}}$ Low.

T_A = –55°C to +125°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 12MHz.
(Load Capacitance for PORT 0, ALE and PSEN = 100pf; Load Capacitance for all other outputs = 80 pF.)

External Program Memory Characteristics

Symbol	Parameter	0 to 12 MHz		25 MHz		Units
		Min	Max	Min	Max	
TLHLL	ALE pulse width	2TCLCL – 40		70		ns
TAVLL	Address Valid to ALE	TCLCL – 40		20		ns
TLLAX	Address Hold After ALE	TCLCL – 30		28		ns
TLLIV	ALE to Valid Instruction In		4TCLCL – 100		120	ns
TLLPL	ALE to $\overline{\text{PSEN}}$	TCLCL – 30		30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	3TCLCL – 45		100		ns
TPLIV	$\overline{\text{PSEN}}$ to Valid Instruction In		3TCLCL – 105		80	ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instruction FloatAfter $\overline{\text{PSEN}}$		TCLCL – 25		35	ns
TPXAV	$\overline{\text{PSEN}}$ to Address Valid	TCLCL – 8		40		ns
TAVIV	Address to Valid Instruction In		5TCLCL – 105		140	ns
TPXAV	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns

External Program Memory Read Cycle
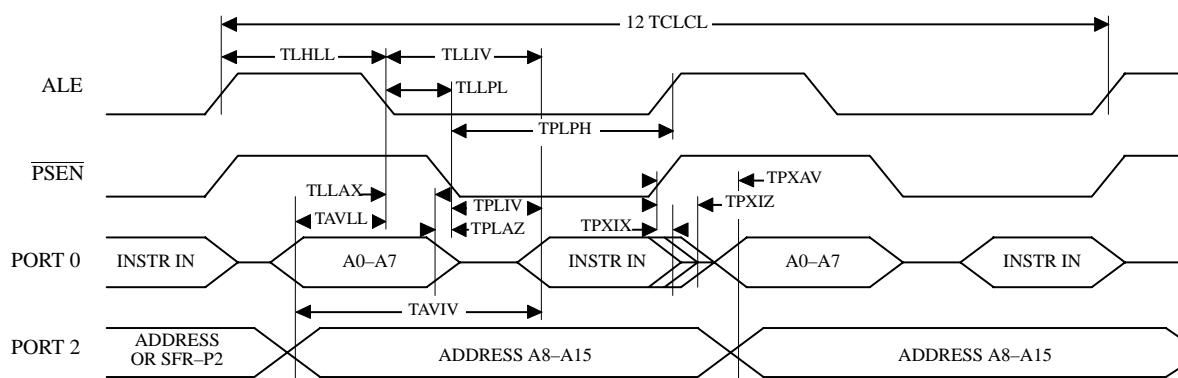
Symbol	Parameter	Min	Max	Min	Max	Units
TWLWH	$\overline{WR}$ Pulse Width	6TCLCL–100		210		ns
TRLDV	$\overline{RD}$ to Valid Data In		5TCLCL–165		170	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		2TCLCL–60		70	ns
TLLDV	ALE to Valid Data In		8TCLCL–150		290	ns
TAVDV	Address to Valid Data In		9TCLCL–165		320	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	3TCLCL–50	3TCLCL+50	130	170	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	4TCLCL–130		140		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	TCLCL–50		15		ns
TQVWH	Data set–up to $\overline{WR}$ High	7TCLCL–150		250		ns
TWHQX	Data Hold After $\overline{WR}$	TCLCL–50		30		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE high	TCLCL–40	TCLCL+40	25	50	ns

External Data Memory Write Cycle
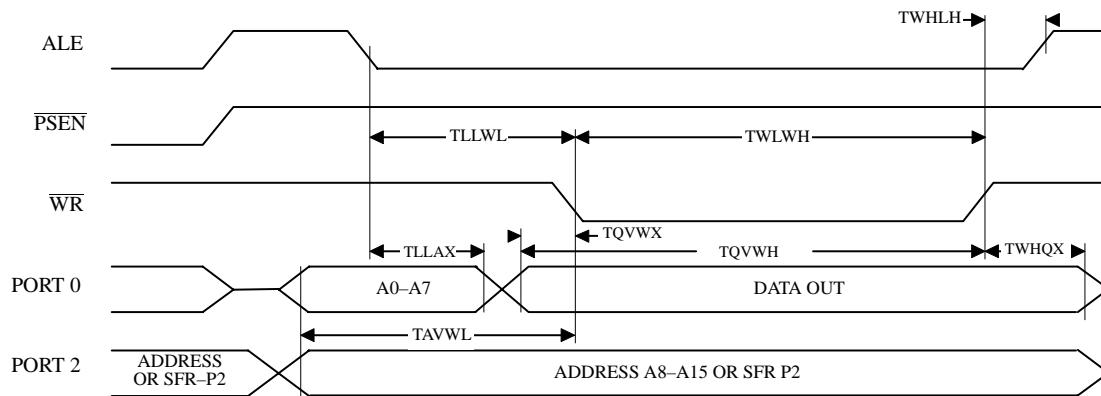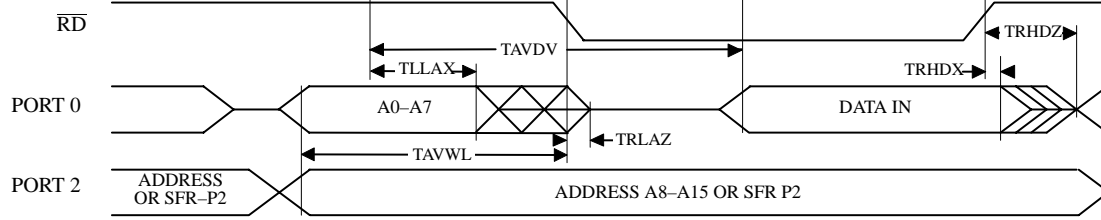
## Serial Port Timing – Shift Register Mode

Symbol	Parameter	0 to 12MHz		25 MHz		Units
		Min	Max	Min	Max	
TXLXL	Serial port clock cycle time	12TCLCL		480		ns
TQVHX	Output data set–up to clock rising edge	10TCLCL–133		380		ns
TXHQX	Output data hold after clock rising edge	2TCLCL–117		65		ns
TXHDX	Input data hold after clock rising edge	0		0		ns
TXHDV	Clock rising edge to input data valid		10TCLCL–133		350	ns

Shift Register Timing Waveforms
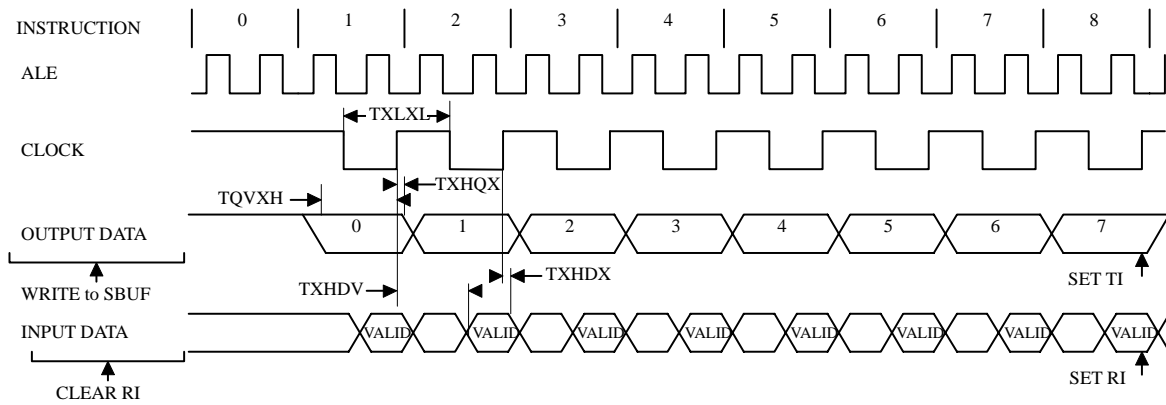
IPP	Programming Supply Current			75	mA
1/TCLCL	Oscillator Frquency	4	6		MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48 TCLCL			
TGHAX	Adress Hold after $\overline{PROG}$	48 TCLCL			
TDVGL	Data Setup to $\overline{PROG}$ Low	48 TCLCL			
TGHDX	Data Hold after $\overline{PROG}$	48 TCLCL			
TEHSH	(Enable) High to VPP	48 TCLCL			
TSHGL	VPP Setup to $\overline{PROG}$ Low	10			μs
TGHSL	VPP Hold after $\overline{PROG}$	10			μs
TGLGH	$\overline{PROG}$ Width	90	110		μs
TAVQV	Address to Valid Data		48 TCLCL		
TELQV	ENABLE Low to Data Valid		48 TCLCL		
TEHQZ	Data Float after ENABLE	0	48 TCLCL		
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10			μs

EPROM Programming and Verification Waveforms

Rev. E － July 03, 2000
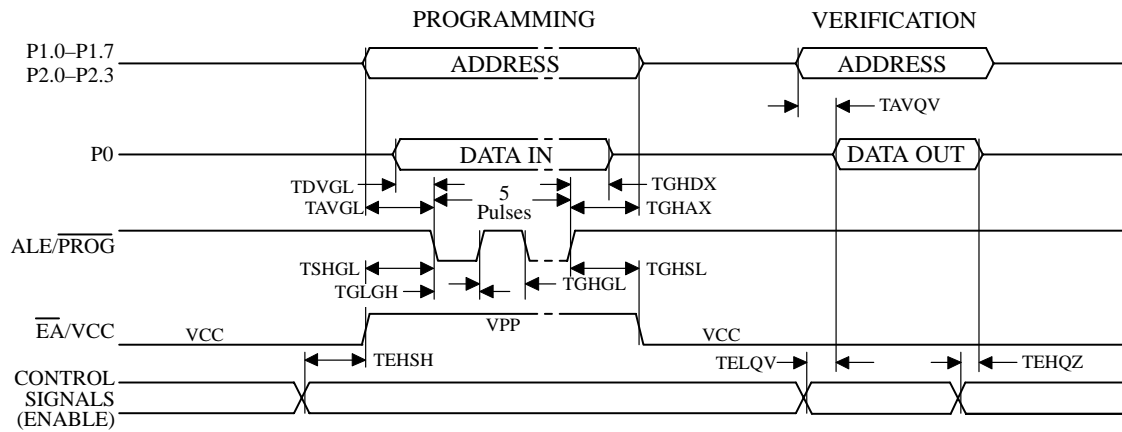
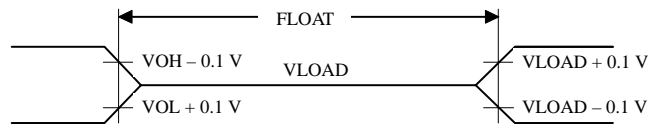|			5		ns
TCLCX	Low Time		5		ns
TCLCH	Rise Time			5	ns
TCHCL	Fall Time			5	ns

External Clock Drive Waveforms
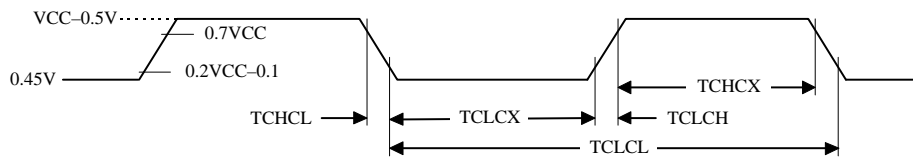
AC Testing Input/Output Waveforms
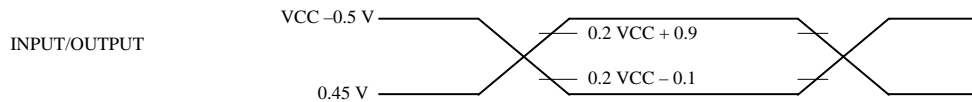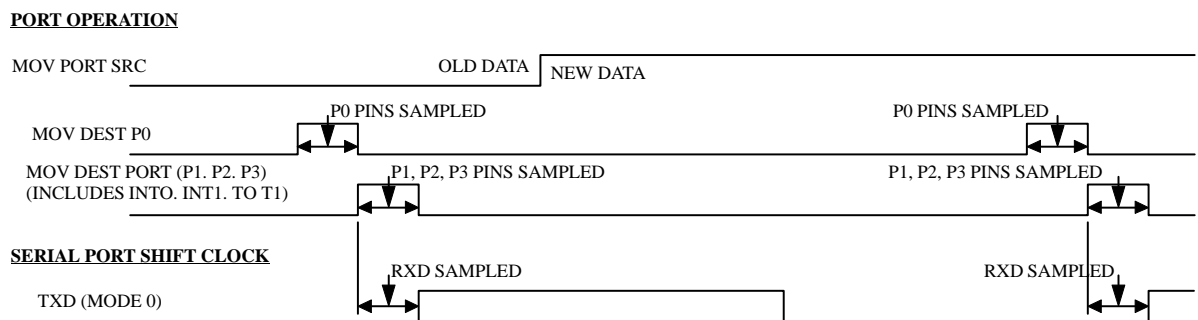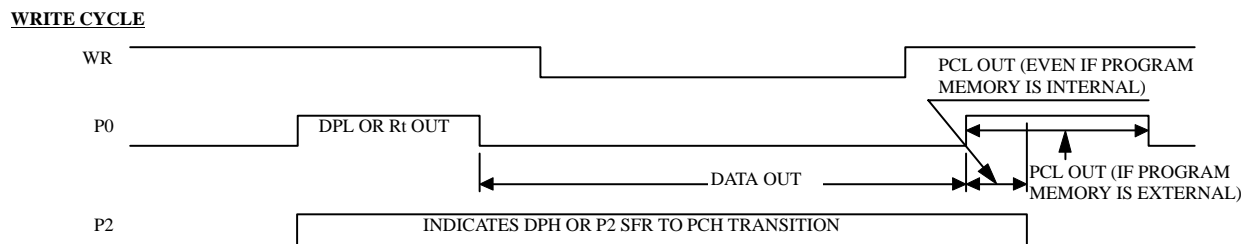
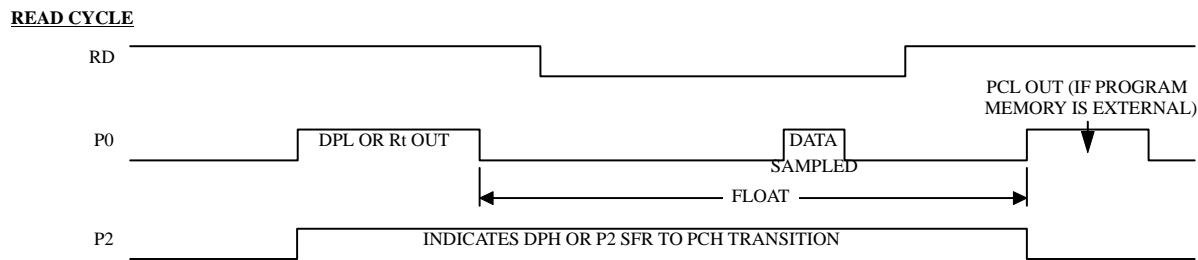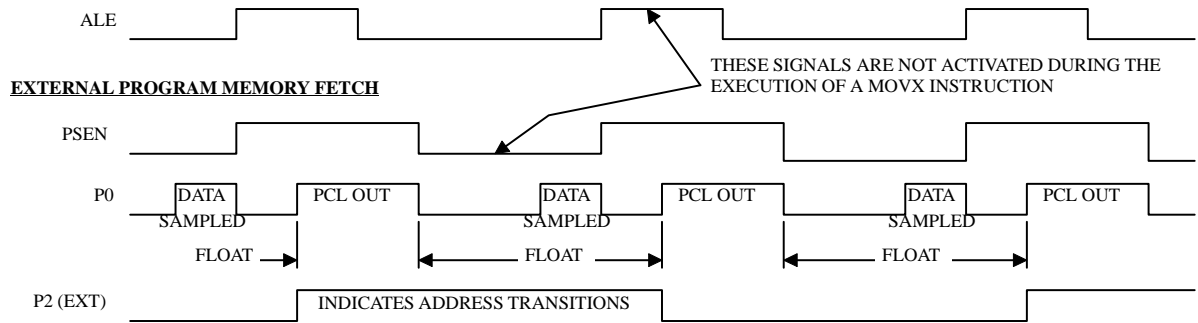

AC inputs during testing are driven at VCC – 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at VIH min for a logic "1" and VIL max for a logic "0".

Float Waveforms

For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. IOL/IOH ≥ ± 20mA.

ALE

THESE SIGNALS ARE NOT ACTIVATED DURING THE
EXECUTION OF A MOVX INSTRUCTION

EXTERNAL PROGRAM MEMORY FETCH

PSEN

P0   DATA SAMPLED   PCL OUT   DATA SAMPLED   PCL OUT   DATA SAMPLED   PCL OUT

FLOAT   FLOAT   FLOAT

P2 (EXT)   INDICATES ADDRESS TRANSITIONS

READ CYCLE

RD

PCL OUT (IF PROGRAM MEMORY IS EXTERNAL)

P0   DPL OR Rt OUT   DATA SAMPLED

FLOAT

P2   INDICATES DPH OR P2 SFR TO PCH TRANSITION

WRITE CYCLE

WR

PCL OUT (EVEN IF PROGRAM MEMORY IS INTERNAL)

P0   DPL OR Rt OUT

DATA OUT

PCL OUT (IF PROGRAM MEMORY IS EXTERNAL)

P2   INDICATES DPH OR P2 SFR TO PCH TRANSITION

PORT OPERATION

MOV PORT SRC   OLD DATA   NEW DATA

MOV DEST P0   P0 PINS SAMPLED   P0 PINS SAMPLED

MOV DEST PORT (P1. P2. P3) (INCLUDES INTO. INT1. TO T1)   P1, P2, P3 PINS SAMPLED   P1, P2, P3 PINS SAMPLED

SERIAL PORT SHIFT CLOCK

TXD (MODE 0)   RXD SAMPLED   RXD SAMPLED

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A=25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85ns. Propagation delays are incorporated in the AC specifications.

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–25: 25 MHz version

OTP Packaging
    G: CDIL 40 (.6)
    I: CQPJ 44

EPROM–UV Erasable
    J: Window CDIL 40
    K: Window CQPJ 44

Part Number
87C51: Programmable ROM

Quality Flow
Blank : Military temperature
MQ : QML.Q*
/883 : M.I–STD 883 CLASS B

TEMIC Semiconductors
Microcontroller Product Line

Temperature Range
M:Military –55° to 125°C

* The Standart Microcircuit Drawing 5962–87684 must be used as the reference for QML–Q procurement.