



128Kx32 SRAM MODULE, SMD 5962-93187 & 5962-95595

FEATURES

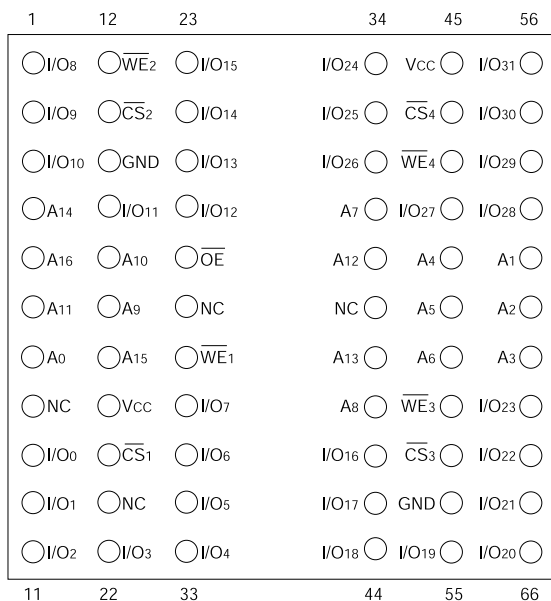
- Access Times of 15, 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 Compliant Devices Available
- Packaging
 - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400)
 - 68 lead, 40mm CQFP (G4T)¹, 3.56mm (0.140") (Package 502).
 - 68 lead, 22.4mm CQFP (G2T)¹, 4.57mm (0.180"), (Package 509)
 - 68 lead, 23.9mm Low Profile CQFP (G1U), 3.57mm (0.140"), (Package 519)
 - 68 lead, 23.9mm Low Profile CQFP (G1T), 4.06 mm (0.160"), (Package 524)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8

- Low Power Data Retention - only available in G2T package type
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight:
 - WS128K32-XG1UX - 5 grams typical
 - WS128K32-XG1TX - 5 grams typical
 - WS128K32-XG2TX¹ - 8 grams typical
 - WS128K32-XH1X - 13 grams typical
 - WS128K32-XG4TX¹ - 20 grams typical
- All devices are upgradeable to 512Kx32

Note 1: Package Not Recommended For New Design

FIG. 1 PIN CONFIGURATION FOR WS128K32N-XH1X

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

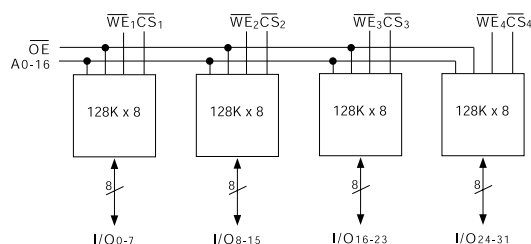
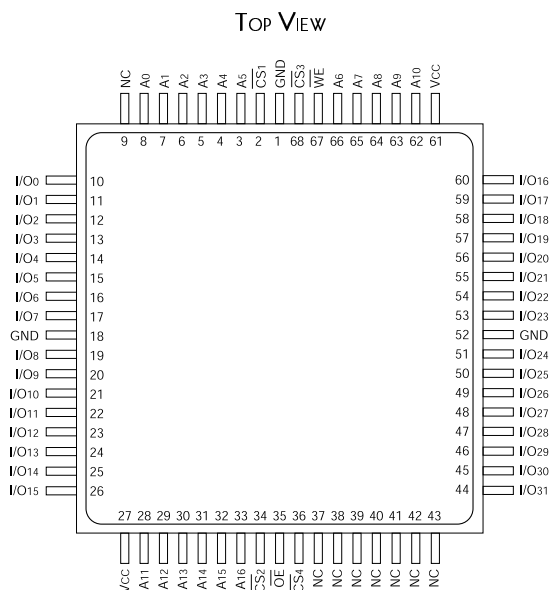




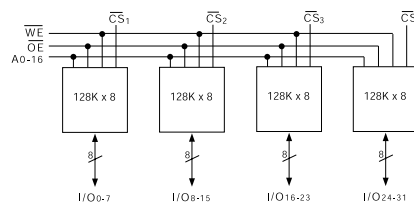
FIG. 2 PIN CONFIGURATION FOR WS128K32-XG4TX¹



PIN DESCRIPTION

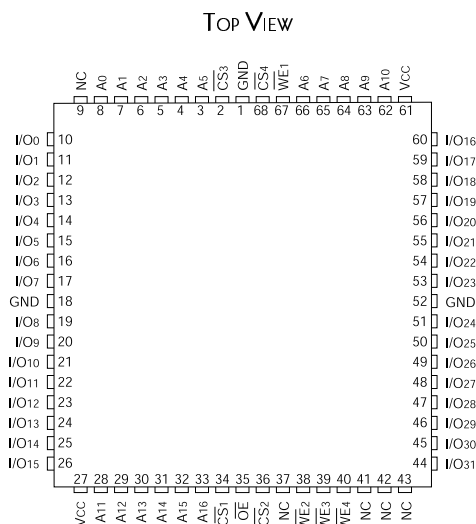
I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



Note 1: Package Not Recommended For New Design

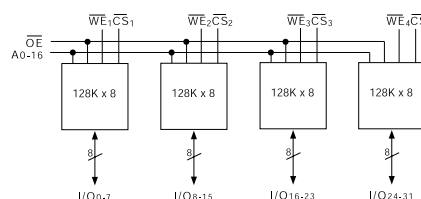
FIG. 3 PIN CONFIGURATION FOR WS128K32-XG2TX¹, WS128K32-XG1TX AND WS128K32-XG1UX



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



Note 1: Package Not Recommended For New Design



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} + 0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE (T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance HIP (PGA) H1 CQFP G4 CQFP G2T CQFP G1U/G1T	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20 50 20 20	pF
$\overline{CS}$ 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{IO}	V _{IO} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C TO +125°C)

Parameter	Sym	Conditions	-15		-17		-20		-25		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{II}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10		10		10		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10		10		10		10	μA
Operating Supply Current	I _{CC}	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5 MHz, V _{CC} = 5.5		600		600		600		600	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5 MHz, V _{CC} = 5.5		80		80		80		60	mA
Output Low Voltage	V _{OL}	I _{OL} = 8 mA, V _{CC} = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA, V _{CC} = 4.5	2.4		2.4		2.4		2.4		V

Parameter	Sym	Conditions	-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{II}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10		10		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10		10		10	μA
Operating Supply Current	I _{CC}	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5 MHz, V _{CC} = 5.5		600		600		600	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5 MHz, V _{CC} = 5.5		60		60		60	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1 mA, V _{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA, V _{CC} = 4.5	2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS*

(T_A = -55°C TO +125°C), (T_A = -40°C TO +85°C)

Characteristic	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V _{CC}	V _{CC} = 2.0V	2	-	-	V
Data Retention Quiescent Current	I _{CCDR}	CS • V _{CC} - 0.2V	-	1	2	mA
Chip Disable to Data Retention Time (1)	T _{CDR}	V _{IN} • V _{CC} - 0.2V	0	-	-	ns
Operation Recovery Time (1)	T _{IR}	or V _{IN} - 0.2V	T _{RC}	-	-	ns

NOTE: Parameter guaranteed, but not tested.

*Low Power Data Retention available only in G2T Package Type.



AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t _{AA}		15		17		20		25		35		45		55	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	t _{OE}		10		10		12		15		20		25		30	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		3		3		3		3		3		3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		12		12		12		12		20		20		20	ns
Output Disable to Output in High Z	t _{OHZ} ¹		12		12		12		12		20		20		20	ns

1. This parameter is guaranteed by design but not tested.

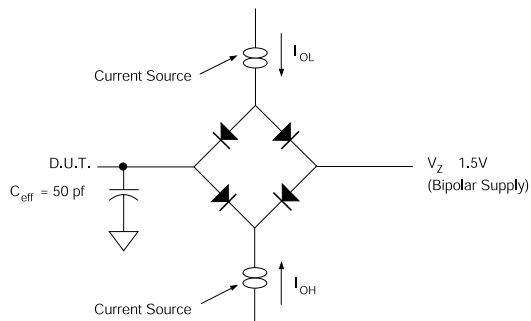
AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	15		17		20		25		35		45		55		ns
Chip Select to End of Write	t _{CW}	14		14		15		20		25		30		45		ns
Address Valid to End of Write	t _{AW}	14		15		15		20		25		30		45		ns
Data Valid to End of Write	t _{DW}	10		10		12		15		20		25		25		ns
Write Pulse Width	t _{WP}	14		14		15		20		25		30		45		ns
Address Setup Time	t _{AS}	0		0		0		0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		0		0		0		ns
Output Active from End of Write	t _{OW} ¹	3		3		3		3		4		4		4		ns
Write Enable to Output in High Z	t _{WHZ} ¹		10		10		12		15		20		25		25	ns
Data Hold Time	t _{DH}	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 4 AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

V_Z is programmable from -2V to +7V.

I_{OL} & I_{OH} programmable from 0 to 16mA.

Tester Impedance: Z₀ = 75 Ω.

V_Z is typically the midpoint of V_{OH} and V_{OL}.

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit. ATE tester includes jig capacitance.



FIG. 5 TIMING WAVEFORM - READ CYCLE

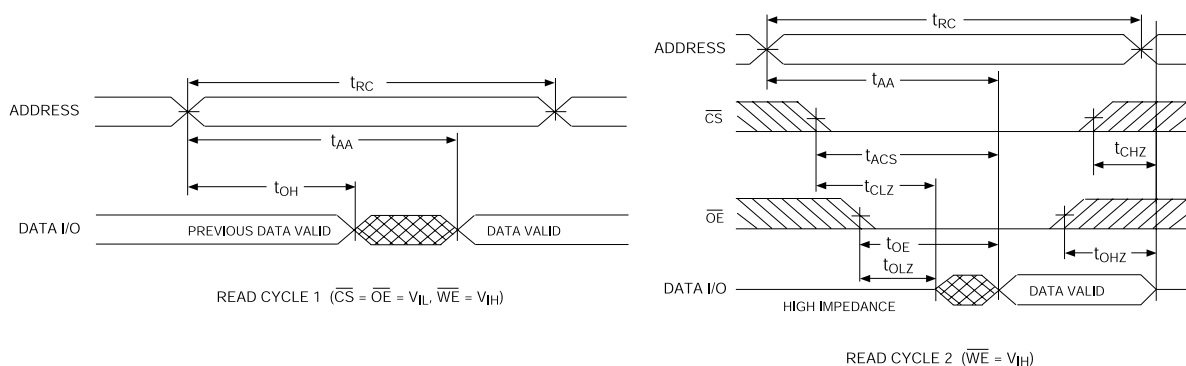


FIG. 6 WRITE CYCLE - $\overline{WE}$ CONTROLLED

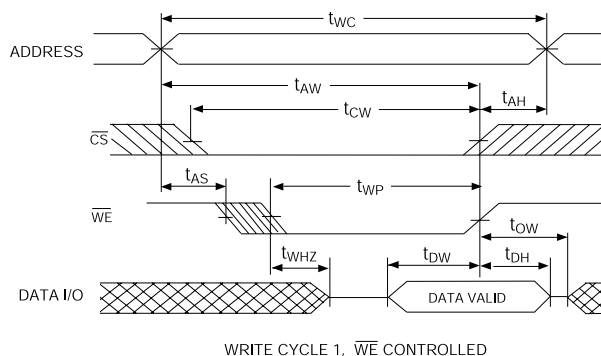
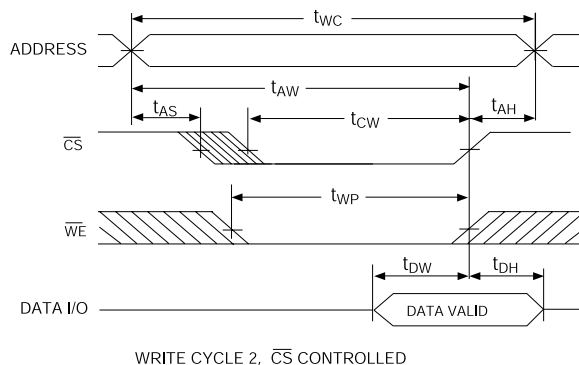
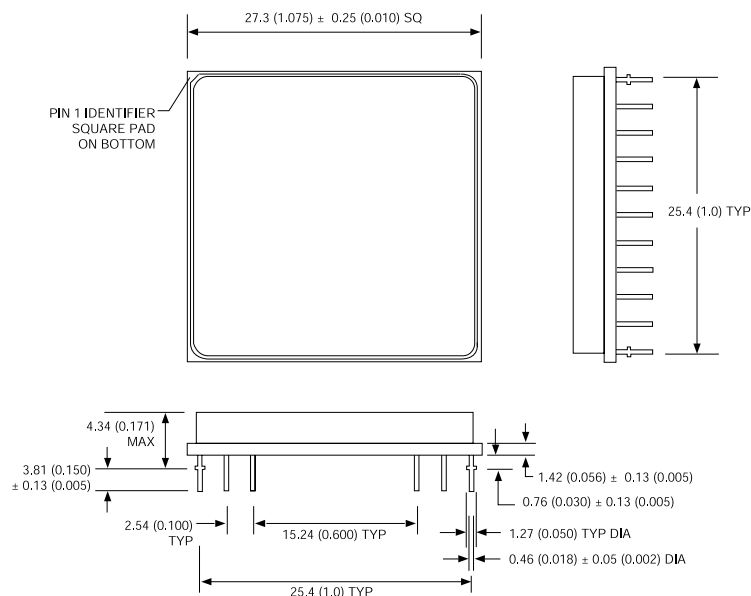


FIG. 7 WRITE CYCLE - $\overline{CS}$ CONTROLLED



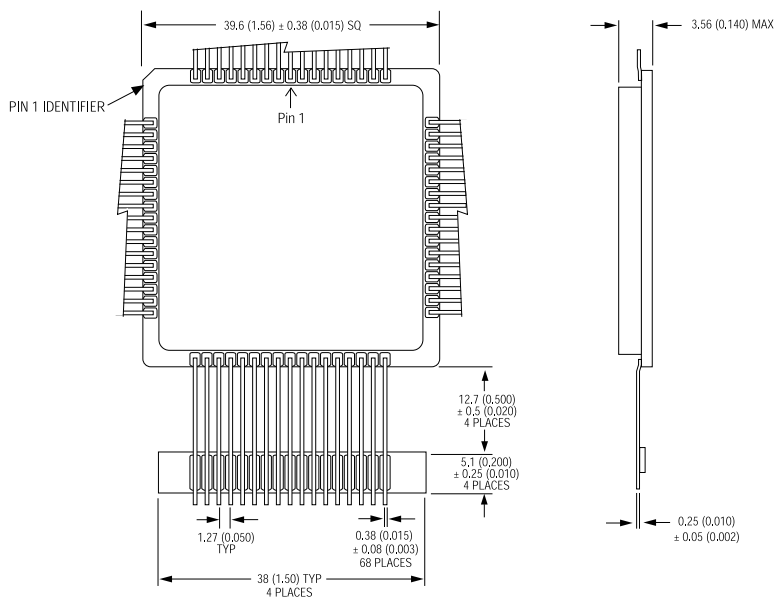


PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)¹

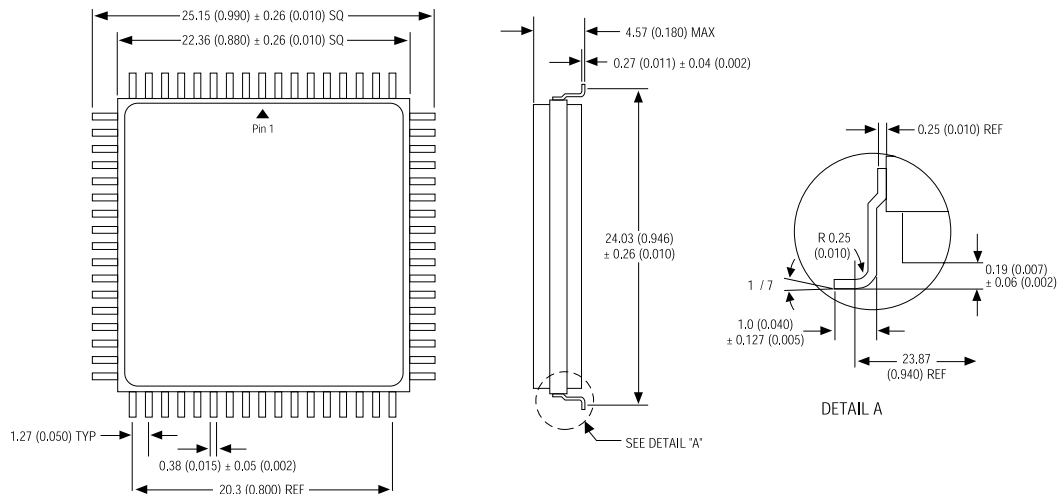


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

Note 1: Package Not Recommended For New Design



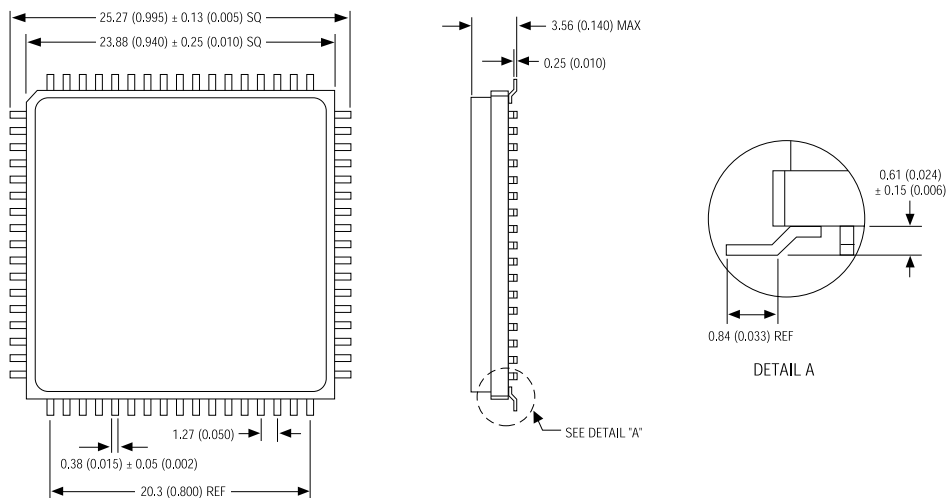
PACKAGE 509: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2T)¹



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

Note 1: Package Not Recommended For New Design

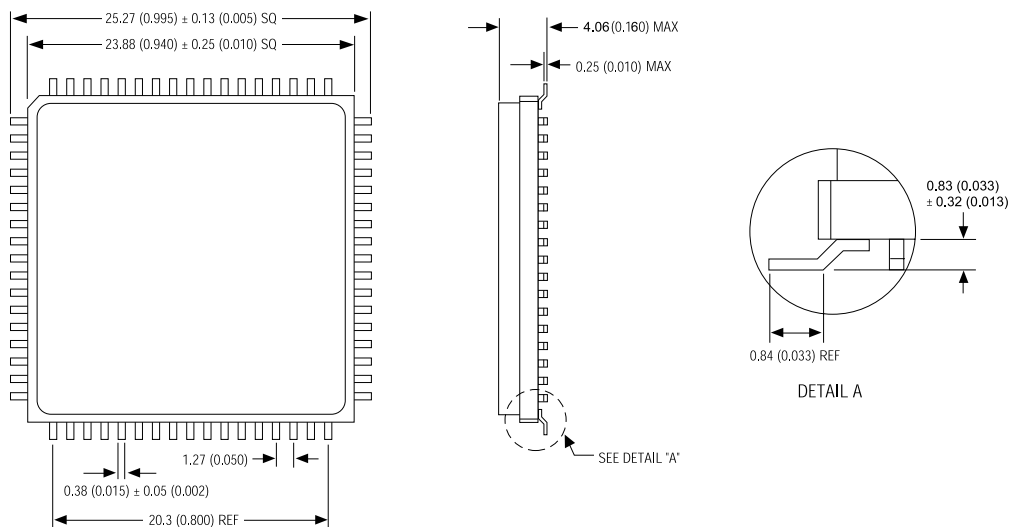
PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 524: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W S 128K 32 X - XXX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

H1 = 1.075" sq. Ceramic Hex-In-line Package, HIP (Package 400)

G2T¹ = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 509)

G1U = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 519)

G1T = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 524)

G4T¹ = 40 mm Low Profile CQFP (Package 502)

ACCESS TIME (ns)

IMPROVEMENT MARK:

N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades

L = Low Power*

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE ELECTRONIC DESIGNS CORPORATION

* Low Power Data Retention only available in G2T Package Type

Note 1: Package Not Recommended For New Design



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-93187 05H4X
128K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-93187 06H4X
128K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-93187 07H4X
128K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-93187 08H4X
128K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-93187 09H4X
128K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-93187 10H4X
128K x 32 SRAM Module	15ns	66 pin HIP (H1)	5962-93187 11H4X
128K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T) ¹	5962-95595 05HYX ¹
128K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T) ¹	5962-95595 06HYX ¹
128K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T) ¹	5962-95595 07HYX ¹
128K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T) ¹	5962-95595 08HYX ¹
128K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T) ¹	5962-95595 09HYX ¹
128K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T) ¹	5962-95595 10HYX ¹
128K x 32 SRAM Module	15ns	68 lead CQFP Low Profile (G4T) ¹	5962-95595 11HYX ¹
128K x 32 SRAM Module	55ns	68 lead CQFP/J (G2T) ¹	5962-95595 05HMX ¹
128K x 32 SRAM Module	45ns	68 lead CQFP/J (G2T) ¹	5962-95595 06HMX ¹
128K x 32 SRAM Module	35ns	68 lead CQFP/J (G2T) ¹	5962-95595 07HMX ¹
128K x 32 SRAM Module	25ns	68 lead CQFP/J (G2T) ¹	5962-95595 08HMX ¹
128K x 32 SRAM Module	20ns	68 lead CQFP/J (G2T) ¹	5962-95595 09HMX ¹
128K x 32 SRAM Module	17ns	68 lead CQFP/J (G2T) ¹	5962-95595 10HMX ¹
128K x 32 SRAM Module	15ns	68 lead CQFP/J (G2T) ¹	5962-95595 11HMX ¹
128K x 32 SRAM Module	55ns	68 lead CQFP/J (G1U)	5962-95595 05H9X
128K x 32 SRAM Module	45ns	68 lead CQFP/J (G1U)	5962-95595 06H9X
128K x 32 SRAM Module	35ns	68 lead CQFP/J (G1U)	5962-95595 07H9X
128K x 32 SRAM Module	25ns	68 lead CQFP/J (G1U)	5962-95595 08H9X
128K x 32 SRAM Module	20ns	68 lead CQFP/J (G1U)	5962-95595 09H9X
128K x 32 SRAM Module	17ns	68 lead CQFP/J (G1U)	5962-95595 10H9X
128K x 32 SRAM Module	15ns	68 lead CQFP/J (G1U)	5962-95595 11H9X

Note 1: Package Not Recommended For New Design