32Kx32 SRAM MODULE

FEATURES

- Access Times of 25, 35, 45, 55, 70, 85, 100, 120ns
- Packaging
  - 66 pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
- Organized as 32Kx32; User Configurable as 64Kx16 or 128Kx8
- Battery Back-Up Operation
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

FIG. 1 PIN CONFIGURATION FOR WS32K32N-XH1X

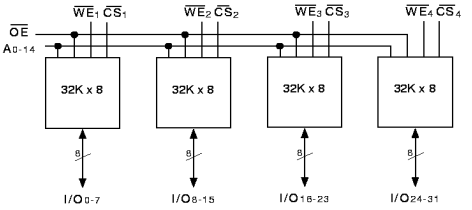
TOP VIEW

1	12	23		34	45	56
I/O8	$\overline{WE}_2$	I/O15		I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14		I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13		I/O26	$\overline{WE}_4$	I/O29
A13	I/O11	I/O12		A6	I/O27	I/O28
A14	A10	$\overline{OE}$		A7	A3	A0
NC	A11	NC		NC	A4	A1
NC	A12	$\overline{WE}_1$		A8	A5	A2
NC	VCC	I/O7		A9	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6		I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-14	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = 25°C)

Test	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
$\overline{CS}$ 1-4 capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

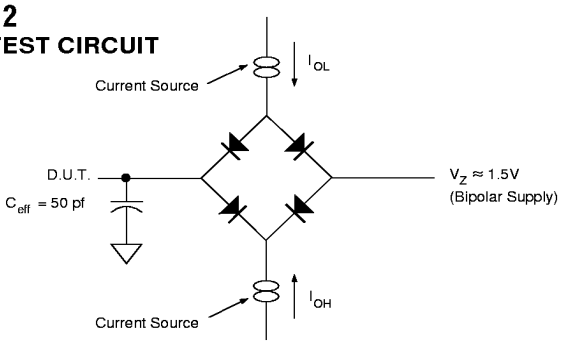
(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-25		-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		15		15		15		15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		15		15		15		15	µA
Operating Supply Current x 32 Mode	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		450		450		450		450	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz		60		60		55		50	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, Vcc = 4.5		0.4		0.4					V
		I_{OL} = 2.1mA, Vcc = 4.5						0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, Vcc = 4.5	2.4		2.4						V
		I_{OH} = -1.0mA, Vcc = 4.5					2.4		2.4		V

Parameter	Symbol	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		15		15		15		15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		15		15		15		15	µA
Operating Supply Current x 32 Mode	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz	450		450		170		170		mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz	45		4		2.0		2.0		mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, Vcc = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, Vcc = 4.5	2.4		2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

FIG. 2
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-25			-35			-45			-55			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		.5	8.0		.5	8.0		.5	8.0		.03	3.2	mA
	I_{CCDR2}	V_{CC} = 2V		.25	4.0		.25	4.0		.25	4.0		.02	2.1	mA

Parameter	Symbol	Conditions	-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		30	1200		10	1600		10	750		10	750	µA
	I_{CCDR2}	V_{CC} = 2V		20	900		7	1200		7	500		7	500	µA

AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		55		ns
Address Access Time	t_{AA}		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	5		5		5		5		ns
Chip Select Access	t_{ACS}		25		35		45		55	ns
Output Enable to Output Valid	t_{OE}		15		20		25		30	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		12		15		20		25	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12		15		20		25	ns

1. This parameter is guaranteed by design but not tested.

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Output Hold from Address Change	t_{OH}	5		5		5		5		ns
Chip Select Access	t_{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t_{OE}		35		40		45		50	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		30		35		40		50	ns
Output Disable to Output in High Z	t_{OHZ}[1]		30		35		40		50	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-25		-35		-45		-55		Units
Write Cycle		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Cycle Time	t_{WC}	25		35		45		55		ns
Chip Select to End of Write	t_{CW}	20		30		40		45		ns
Address Valid to End of Write	t_{AW}	20		30		40		45		ns
Data Valid to End of Write	t_{DW}	15		18		20		25		ns
Write Pulse Width	t_{WP}	20		25		35		40		ns
Address Setup Time	t_{AS}	5		5		5		5		ns
Address Hold Time	t_{AH}	0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		10		15		15		20	ns
Data Hold Time	t_{DH}	3		3		3		5		ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		-85		-100		-120		Units
Write Cycle		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	65		80		90		110		ns
Address Valid to End of Write	t_{AW}	65		80		90		110		ns
Data Valid to End of Write	t_{DW}	30		35		40		55		ns
Write Pulse Width	t_{WP}	45		50		55		65		ns
Address Setup Time	t_{AS}	5		5		5		5		ns
Address Hold Time	t_{AH}	0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		30		35		40		50	ns
Data Hold Time	t_{DH}	5		5		5		5		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3
TIMING WAVEFORM - READ CYCLE

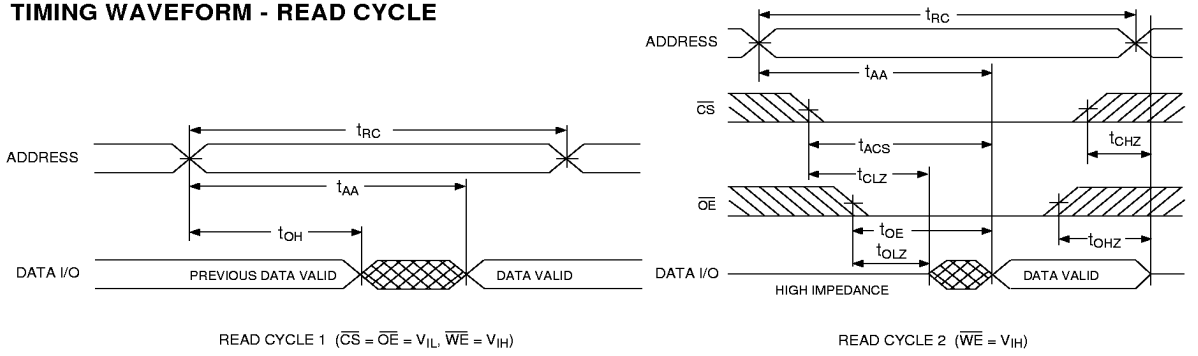


FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED

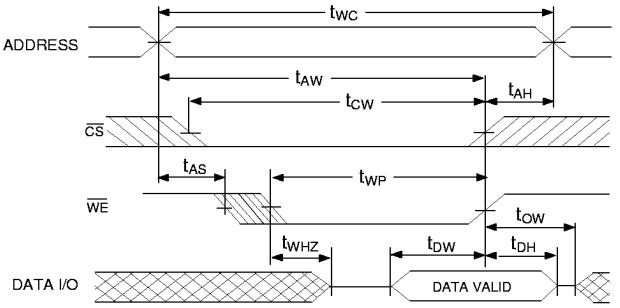
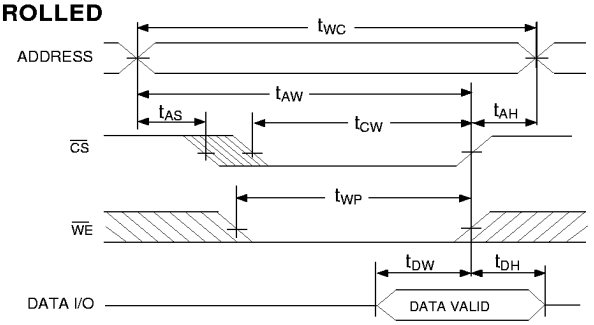
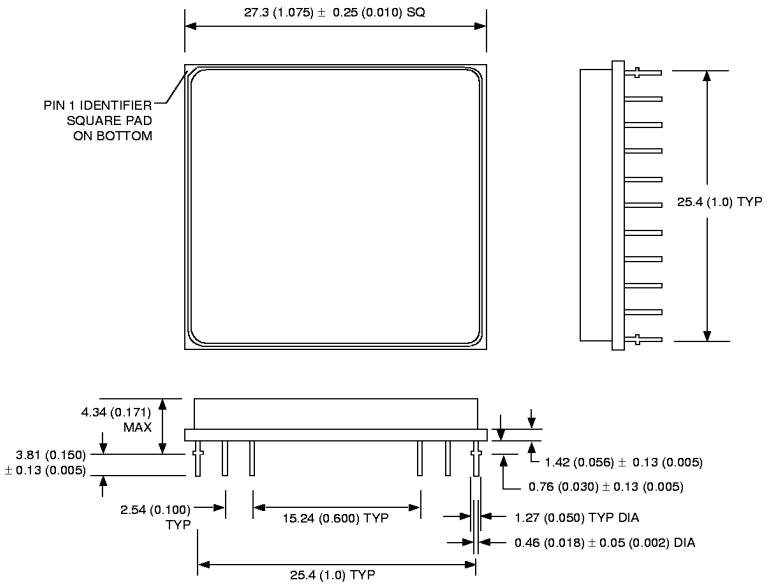


FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED



PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION