CYPRESS SEMICONDUCTOR

CY7C420, CY7C421
CY7C424, CY7C425
CY7C428, CY7C429

CYPRESS SEMICONDUCTOR

T-46-35

Cascadeable 512 x 9 FIFO
Cascadeable 1K x 9 FIFO
Cascadeable 2K x 9 FIFO

Features

- 512 x 9, 1,024 x 9, 2,048 x 9 FIFO buffer memory
- Dual-port RAM cell
- Asynchronous read/write
- High-speed 33.3-MHz read/write independent of depth/width
- Low operating power
  - I_{CC} (max.) = 142 mA (commercial)
  - I_{CC} (max.) = 147 mA (military)
- Half Full flag in standalone
- Empty and Full flags
- Retransmit in standalone
- Expandable in width and depth
- Parallel cascade minimizes bubble-through
- 5V ± 10% supply
- 300-mil DIP packaging
- 300-mil SOJ packaging
- TTL compatible
- Three-state outputs
- Pin compatible and functional equivalent to IDT7201, IDT7202, and IDT7203

Functional Description

The CY7C420/CY7C421, CY7C424/CY7C425, and CY7C428/CY7C429 are first-in first-out (FIFO) memories offered in 600-mil wide and 300-mil wide packages. They are, respectively, 512, 1,024, and 2,048 words by 9-bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

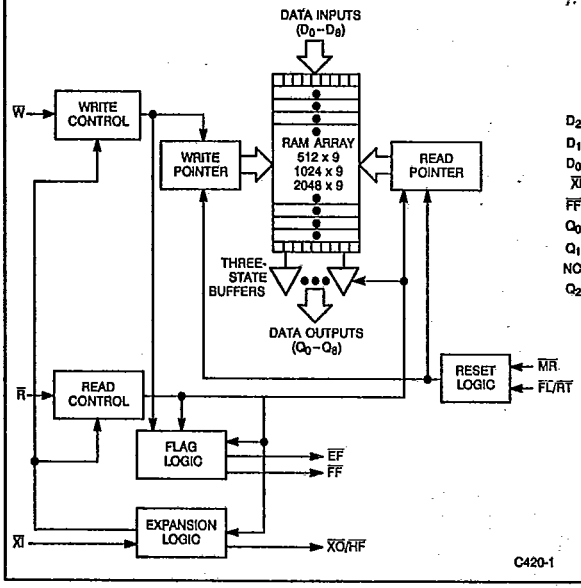
The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during retransmit, and then $\overline{R}$ is used to access the data.

The CY7C420, CY7C421, CY7C424, CY7C425, CY7C428, and CY7C429 are fabricated using an advanced 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout, guard rings, and a substrate bias generator.

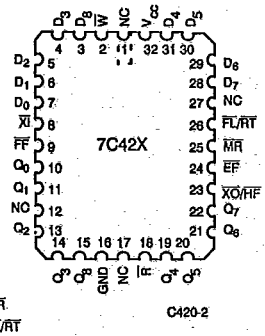
Logic Block Diagram



C420-1

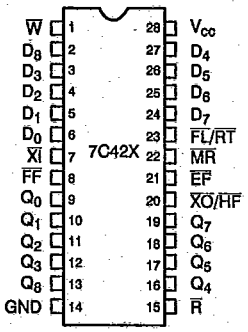
Pin Configurations

PLCC/LCC
Top View



C420-2

DIP
Top View



C420-3

Selection Guide

		7C420-20 7C421-20 7C424-20 7C425-20 7C428-20 7C429-20	7C420-25 7C421-25 7C424-25 7C425-25 7C428-25 7C429-25	7C420-30 7C421-30 7C424-30 7C425-30 7C428-30 7C429-30	7C420-40 7C421-40 7C424-40 7C425-40 7C428-40 7C429-40	7C420-65 7C421-65 7C424-65 7C425-65 7C428-65 7C429-65
Frequency (MHz)		33.3	28.5	25	20	12.5
Maximum Access Time (ns)		20	25	30	40	65
Maximum Operating Current (mA)	Commercial	142	132	125	115	100
	Military/Industrial		147	140	130	115

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	− 40°C to +85°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C420-20 7C421-20 7C424-20 7C425-20 7C428-20 7C429-20		7C420-25 7C421-25 7C424-25 7C425-25 7C428-25 7C429-25		7C420-30 7C421-30 7C424-30 7C425-30 7C428-30 7C429-30		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
			Mil/Ind			2.2	V_{CC}	2.2	V_{CC}	
V_{IL}	Input LOW Voltage			− 3.0	0.8	− 3.0	0.8	− 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		142		132		125	mA
			Mil/Ind[4]				147		140	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		30		25		25	mA
			Mil/Ind				30		30	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		25		20		20	mA
			Mil/Ind				25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			− 90		− 90		− 90	mA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 100 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
4. I_{CC} (military) = 115 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz.
   where $\bar{f}$ = the larger of the write or read operating frequency.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[2] (continued)

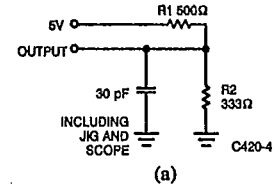
Parameter	Description	Test Conditions		7C420-40 7C421-40 7C424-40 7C425-40 7C428-40 7C429-40 Min.	Max.	7C420-65 7C421-65 7C424-65 7C425-65 7C428-65 7C429-65 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	V
			Mil/Ind	2.2	V_{CC}	2.2	V_{CC}	
V_{IL}	Input LOW Voltage			− 3.0	0.8	− 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		− 10	+10	− 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		115		100	mA
			Mil/Ind[4]		130		115	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25		25	mA
			Mil		30		30	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		20		20	mA
			Mil		25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			− 90		− 90	mA

Capacitance[6]

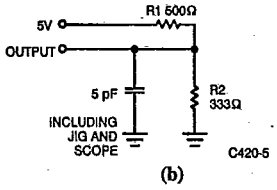
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
6. Tested initially and after any design or process changes that may affect these parameters.

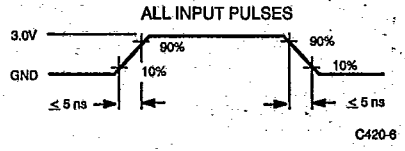
AC Test Loads and Waveforms



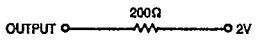
(a)



(b)



Equivalent to: THÉVENIN EQUIVALENT



T-46-35

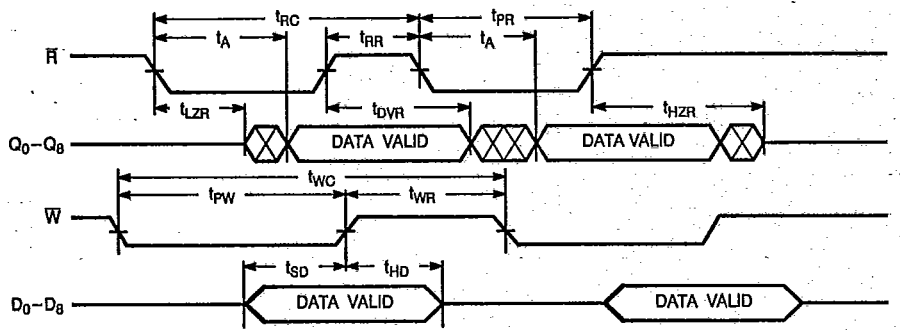
Switching Characteristics Over the Operating Range[7,8]

Parameters	Description	7C420-20 7C421-20 7C424-20 7C425-20 7C428-20 7C429-20		7C420-25 7C421-25 7C424-25 7C425-25 7C428-25 7C429-25		7C420-30 7C421-30 7C424-30 7C425-30 7C428-30 7C429-30		7C420-40 7C421-40 7C424-40 7C425-40 7C428-40 7C429-40		7C420-65 7C421-65 7C424-65 7C425-65 7C428-65 7C429-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	30		35		40		50		80		ns
t_A	Access Time		20		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		10		15		ns
t_{PR}	Read Pulse Width	20		25		30		40		65		ns
t_{LZR}[9]	Read LOW to Low Z	3		3		3		3		3		ns
t_{DVR}[9,10]	Read HIGH to Data Valid	3		3		3		3		3		ns
t_{HZR}[9,10]	Read HIGH to High Z		15		18		20		25		30	ns
t_{WC}	Write Cycle Time	30		35		40		50		80		ns
t_{PW}	Write Pulse Width	20		25		30		40		65		ns
t_{HWZ}[9]	Write HIGH to Low Z	10		10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		10		15		ns
t_{SD}	Data Set-Up Time	12		15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	30		35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	20		25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	20		25		30		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	20		25		30		40		65		ns
t_{RTC}	Retransmit Cycle Time	30		35		40		50		80		ns
t_{PRT}	Retransmit Pulse Width	20		25		30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		30		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		30		35		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		30		35		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		25		25		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		25		25		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		25		25		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		25		25		30		35		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		30		35		40		50		80	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		30		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		20		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	20		25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		20		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	20		25		30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		20		25		30		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		20		25		30		40		65	ns

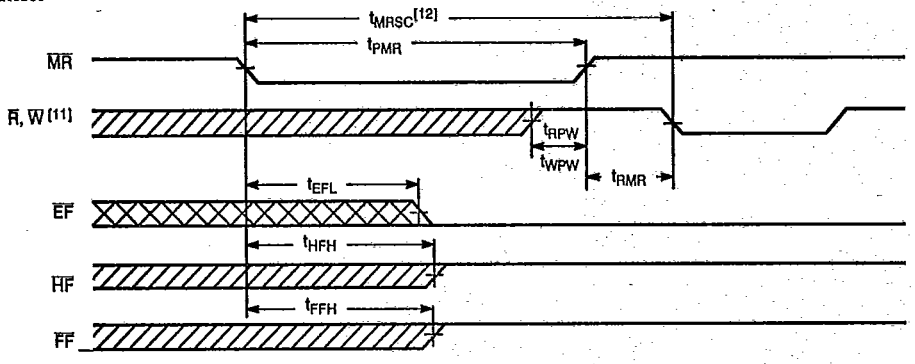
Switching Waveforms

T-46-35

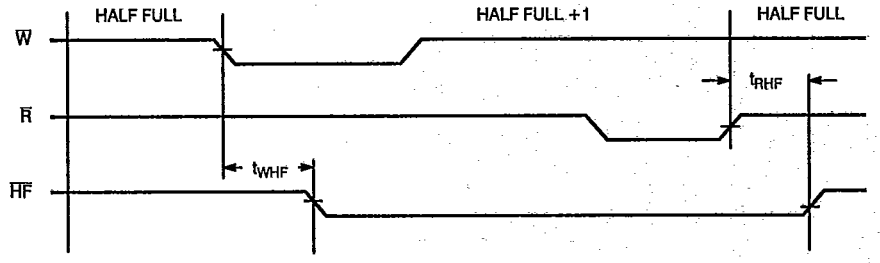
Asynchronous Read and Write



Master Reset



Half-Full Flag



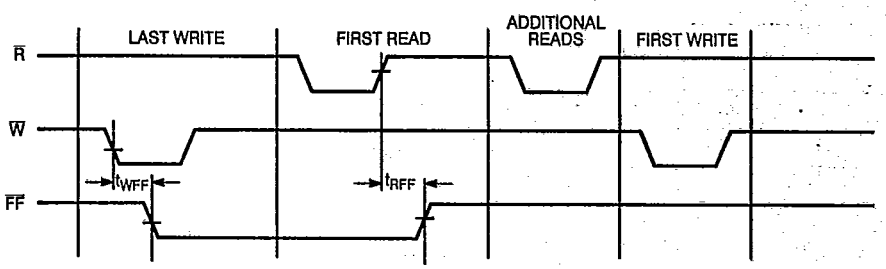
Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
8. See the last page of this specification for Group A subgroup testing information.
9. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
10. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Load and Waveforms.
11. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$.
12. $t_{MRSC} = t_{PMR} + t_{RMR}$.

Switching Waveforms (continued)

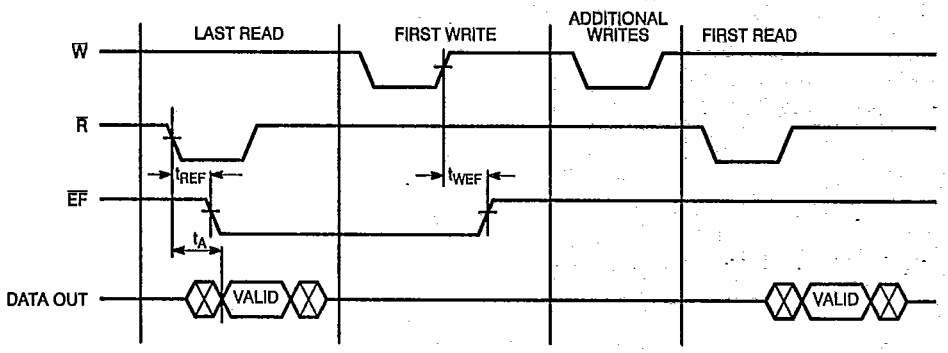
T-46-35

Last Write to First Read Full Flag



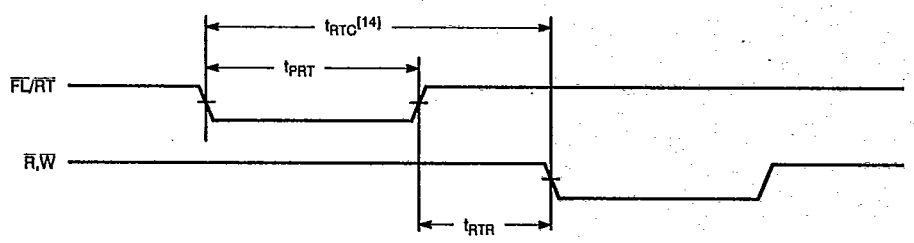
C420-10

Last Read to First Write Empty Flag



C420-11

Retransmit[13]



C420-12

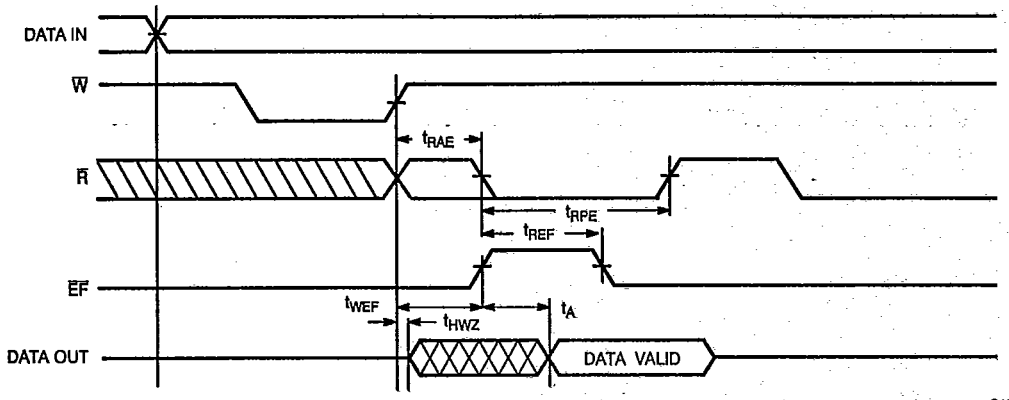
Notes:
13. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
14. $t_{RTC} = t_{PRT} + t_{RTR}$.

5 FIFOs

Switching Waveforms (continued)

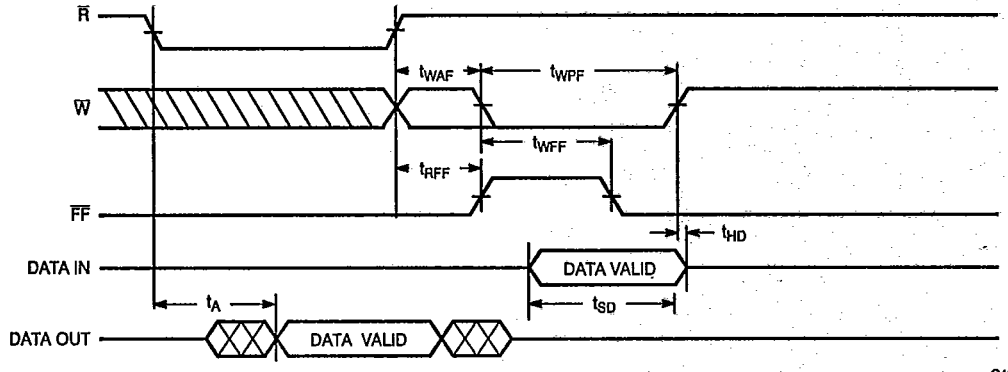
Empty Flag and Empty Boundary Timing Diagram

T-46-35



C420-13

Full Flag and Full Boundary Timing Diagram

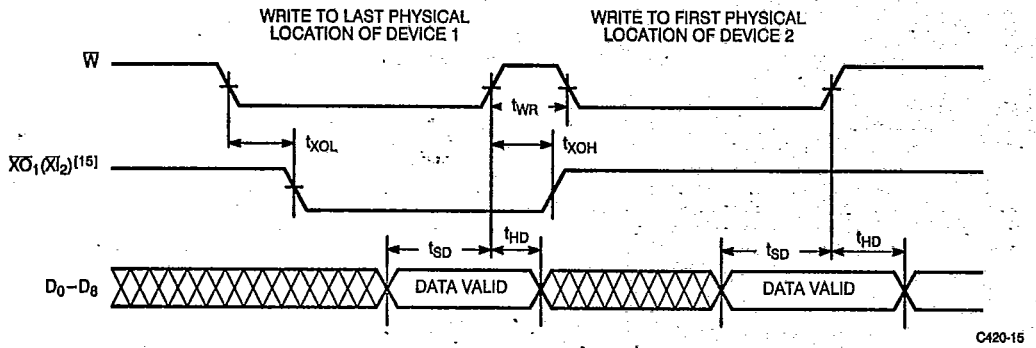


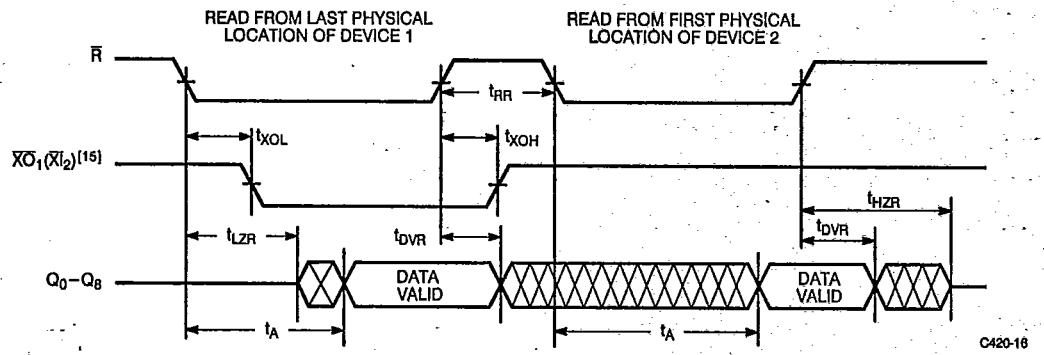
C420-14

Switching Waveforms (continued)

T-46-35

Expansion Timing Diagrams





Notes:
15. Expansion Out of device 1 ($\overline{XO_1}$) is connected to Expansion In of device 2 ($\overline{XI_2}$).

5 FIFOs

Architecture

The CY7C420/421/424/425/428/429 FIFOs consist of an array of 512/1024/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data propagation through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0 - D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being Half Full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{REF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs (Q_0 - Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH) when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly transmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In ($\overline{XI}$) and tying First Load ($\overline{FL}$) to V_{CC}. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

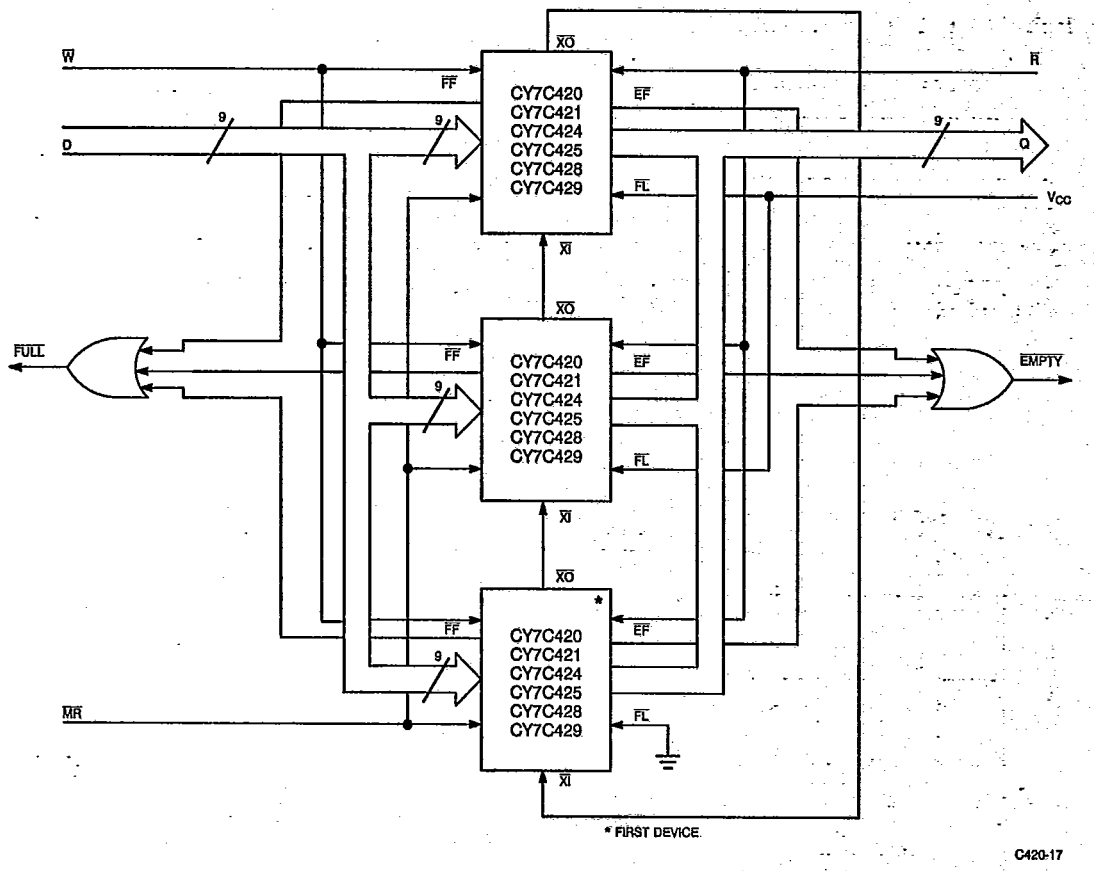
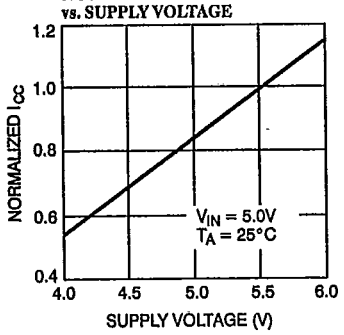


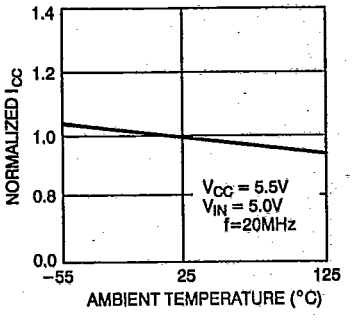
Figure 1. Depth Expansion

Typical DC and AC Characteristics

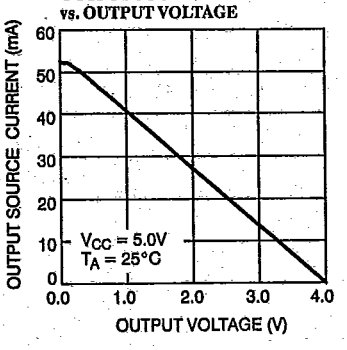
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



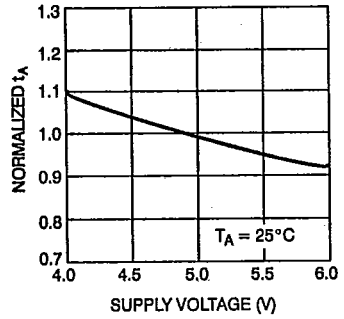
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



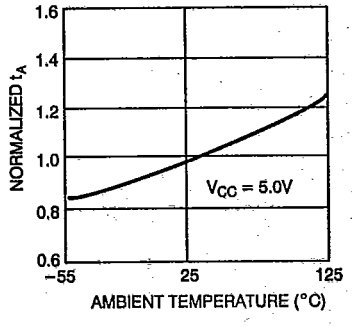
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



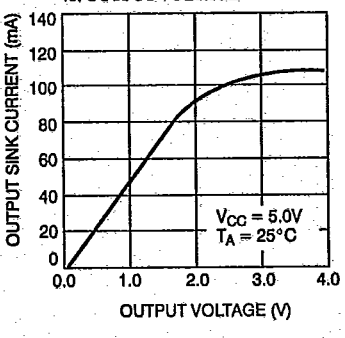
NORMALIZED t_A vs. SUPPLY VOLTAGE



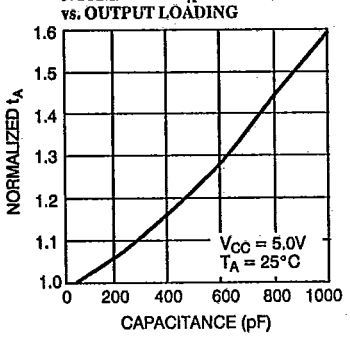
NORMALIZED t_A vs. AMBIENT TEMPERATURE



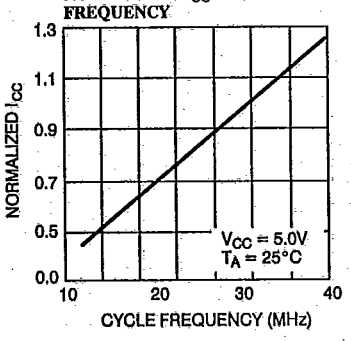
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED t_A CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE FREQUENCY



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C420-20DC	D16	Commercial
	CY7C420-20PC	P15	
25	CY7C420-25DC	D16	Commercial
	CY7C420-25PC	P15	
	CY7C420-25DI	D16	Industrial
	CY7C420-25PI	P15	
	CY7C420-25DMB	D16	Military
30	CY7C420-30DC	D16	Commercial
	CY7C420-30PC	P15	
	CY7C420-30DI	D16	Industrial
	CY7C420-30PI	P15	
	CY7C420-30DMB	D16	Military
40	CY7C420-40DC	D16	Commercial
	CY7C420-40PC	P15	
	CY7C420-40DI	D16	Industrial
	CY7C420-40PI	P15	
	CY7C420-40DMB	D16	Military
65	CY7C420-65DC	D16	Commercial
	CY7C420-65PC	P15	
	CY7C420-65DI	D16	Industrial
	CY7C420-65PI	P15	
	CY7C420-65DMB	D16	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C421-20DC	D22	Commercial
	CY7C421-20JC	J65	
	CY7C421-20LC	L55	
	CY7C421-20PC	P21	
	CY7C421-20VC	V21	
25	CY7C421-25DC	D22	Commercial
	CY7C421-25JC	J65	
	CY7C421-25LC	L55	
	CY7C421-25PC	P21	
	CY7C421-25VC	V21	
	CY7C421-25DI	D22	Industrial
	CY7C421-25JI	J65	
	CY7C421-25PI	P21	
	CY7C421-25DMB	D22	Military
	CY7C421-25KMB	K74	
	CY7C421-25LMB	L55	
30	CY7C421-30DC	D22	Commercial
	CY7C421-30JC	J65	
	CY7C421-30LC	L55	
	CY7C421-30PC	P21	
	CY7C421-30VC	V21	
	CY7C421-30DI	D22	Industrial
	CY7C421-30JI	J65	
	CY7C421-30PI	P21	
	CY7C421-30DMB	D22	Military
	CY7C421-30KMB	K74	
	CY7C421-30LMB	L55	
40	CY7C421-40DC	D22	Commercial
	CY7C421-40JC	J65	
	CY7C421-40LC	L55	
	CY7C421-40PC	P21	
	CY7C421-40VC	V21	
	CY7C421-40DI	D22	Industrial
	CY7C421-40JI	J65	
	CY7C421-40PI	P21	
	CY7C421-40DMB	D22	Military
	CY7C421-40KMB	K74	
	CY7C421-40LMB	L55	
65	CY7C421-65DC	D22	Commercial
	CY7C421-65JC	J65	
	CY7C421-65LC	L55	
	CY7C421-65PC	P21	
	CY7C421-65VC	V21	
	CY7C421-65DI	D22	Industrial
	CY7C421-65JI	J65	
	CY7C421-65PI	P21	
	CY7C421-65DMB	D22	Military
	CY7C421-65KMB	K74	
	CY7C421-65LMB	L55	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C424–20DC	D16	Commercial
	CY7C424–20PC	P15	
25	CY7C424–25DC	D16	Commercial
	CY7C424–25PC	P15	
	CY7C424–25DI	D16	Industrial
	CY7C424–25PI	P15	
	CY7C424–25DMB	D16	Military
30	CY7C424–30DC	D16	Commercial
	CY7C424–30PC	P15	
	CY7C424–30DI	D16	Industrial
	CY7C424–30PI	P15	
	CY7C424–30DMB	D16	Military
40	CY7C424–40DC	D16	Commercial
	CY7C424–40PC	P15	
	CY7C424–40DI	D16	Industrial
	CY7C424–40PI	P15	
	CY7C424–40DMB	D16	Military
65	CY7C424–65DC	D16	Commercial
	CY7C424–65PC	P15	
	CY7C424–65DI	D16	Industrial
	CY7C424–65PI	P15	
	CY7C424–65DMB	D16	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C425–20DC	D22	Commercial
	CY7C425–20JC	J65	
	CY7C425–20LC	L55	
	CY7C425–20PC	P21	
	CY7C425–20VC	V21	
25	C77C425–25DC	D22	Commercial
	CY7C425–25JC	J65	
	CY7C425–25LC	L55	
	CY7C425–25PC	P21	
	CY7C425–25VC	V21	
	CY7C425–25DI	D22	Industrial
	CY7C425–25JI	J65	
	CY7C425–25PI	P21	
	CY7C425–25DMB	D22	Military
	CY7C425–25KMB	K74	
	CY7C425–25LMB	L55	
30	C77C425–30DC	D22	Commercial
	CY7C425–30JC	J65	
	CY7C425–30LC	L55	
	CY7C425–30PC	P21	
	CY7C425–30VC	V21	
	CY7C425–30DI	D22	Industrial
	CY7C425–30JI	J65	
	CY7C425–30PI	P21	
	CY7C425–30DMB	D22	Military
	CY7C425–30KMB	K74	
	CY7C425–30LMB	L55	
40	C77C425–40DC	D22	Commercial
	CY7C425–40JC	J65	
	CY7C425–40LC	L55	
	CY7C425–40PC	P21	
	CY7C425–40VC	V21	
	CY7C425–40DI	D22	Industrial
	CY7C425–40JI	J65	
	CY7C425–40PI	P21	
	CY7C425–40DMB	D22	Military
	CY7C425–40KMB	K74	
	CY7C425–40LMB	L55	
65	C77C425–65DC	D22	Commercial
	CY7C425–65JC	J65	
	CY7C425–65LC	L55	
	CY7C425–65PC	P21	
	CY7C425–65VC	V21	
	CY7C425–65DI	D22	Industrial
	CY7C425–65JI	J65	
	CY7C425–65PI	P21	
	CY7C425–65DMB	D22	Military
	CY7C425–65KMB	K74	
	CY7C425–65LMB	L55	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C428–20DC	D16	Commercial
	CY7C428–20PC	P15	
25	CY7C428–25DC	D16	Commercial
	CY7C428–25PC	P15	
	CY7C428–25DI	D16	Industrial
	CY7C428–25PI	P15	
	CY7C428–25DMB	D16	Military
30	CY7C428–30DC	D16	Commercial
	CY7C428–30PC	P15	
	CY7C428–30DI	D16	Industrial
	CY7C428–30PI	P15	
	CY7C428–30DMB	D16	Military
40	CY7C428–40DC	D16	Commercial
	CY7C428–40PC	P15	
	CY7C428–40DI	D16	Industrial
	CY7C428–40PI	P15	
	CY7C428–40DMB	D16	Military
65	CY7C428–65DC	D16	Commercial
	CY7C428–65PC	P15	
	CY7C428–65DI	D16	Industrial
	CY7C428–65PI	P15	
	CY7C428–65DMB	D16	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C429–20DC	D22	Commercial
	CY7C429–20JC	J65	
	CY7C429–20LC	L55	
	CY7C429–20PC	P21	
	CY7C429–20VC	V21	
25	CY7C429–25DC	D22	Commercial
	CY7C429–25JC	J65	
	CY7C429–25LC	L55	
	CY7C429–25PC	P21	
	CY7C429–25VC	V21	
	CY7C429–25DI	D22	Industrial
	CY7C429–25JI	J65	
	CY7C429–25PI	P21	
	CY7C429–25DMB	D22	Military
	CY7C429–25KMB	K74	
	CY7C429–25LMB	L55	
30	CY7C429–30DC	D22	Commercial
	CY7C429–30JC	J65	
	CY7C429–30LC	L55	
	CY7C429–30PC	P21	
	CY7C429–30VC	V21	
	CY7C429–30DI	D22	Industrial
	CY7C429–30JI	J65	
	CY7C429–30PI	P21	
	CY7C429–30DMB	D22	Military
	CY7C429–30KMB	K74	
	CY7C429–30LMB	L55	
40	CY7C429–40DC	D22	Commercial
	CY7C429–40JC	J65	
	CY7C429–40LC	L55	
	CY7C429–40PC	P21	
	CY7C429–40VC	V21	
	CY7C429–40DI	D22	Industrial
	CY7C429–40JI	J65	
	CY7C429–40PI	P21	
	CY7C429–40DMB	D22	Military
	CY7C429–40KMB	K74	
	CY7C429–40LMB	L55	
65	CY7C429–65DC	D22	Commercial
	CY7C429–65JC	J65	
	CY7C429–65LC	L55	
	CY7C429–65PC	P21	
	CY7C429–65VC	V21	
	CY7C429–65DI	D22	Industrial
	CY7C429–65JI	J65	
	CY7C429–65PI	P21	
	CY7C429–65DMB	D22	Military
	CY7C429–65KMB	K74	
	CY7C429–65LMB	L55	

T-46-35

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPB}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

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