

Description

The μPD424268 is a 262,144 by 4-bit dynamic RAM designed with a write-per-bit option to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of RAS. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by switching the column address inputs.

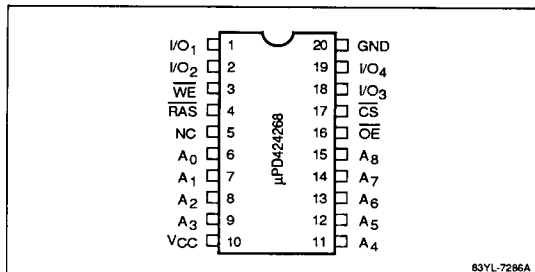
Refreshing may be accomplished by means of a $\overline{CS}$ before RAS cycle that internally generates the refresh address. Refreshing may also be accomplished by means of RAS-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period.

Features

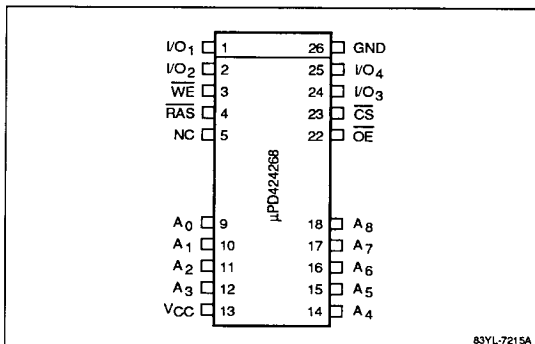
- 262,144 by 4-bit organization
- Single +5-volt power supply
- Write-per-bit option
- Static-column option
- Low power dissipation
- $\overline{CS}$ before RAS internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 512 refresh cycles every 8 ms
- High-density 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

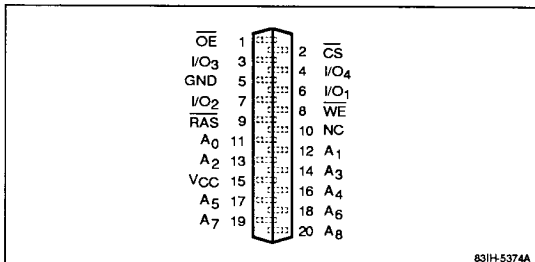
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



Pin Identification

Name	Function
A ₀ - A ₈	Address inputs
I/O ₁ - I/O ₄	Data inputs and outputs
CS	Chip select
OE	Output enable
RAS	Row address strobe
WE	Write enable
GND	Ground
V _{CC}	+5-volt power supply
NC	No connection

CapacitanceT_A = 25 °C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C _{I1}	5	pF	Addresses
	C _{I2}	7	pF	RAS, CS, WE, OE
Input/output capacitance	C _D	7	pF	I/O ₁ - I/O ₄

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V _{IH}	2.4		V _{CC} + 1.0	V
Input voltage, low	V _{IL}	-1.0		0.8	V
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Ambient temperature	T _A	0		70	°C

Absolute Maximum Ratings

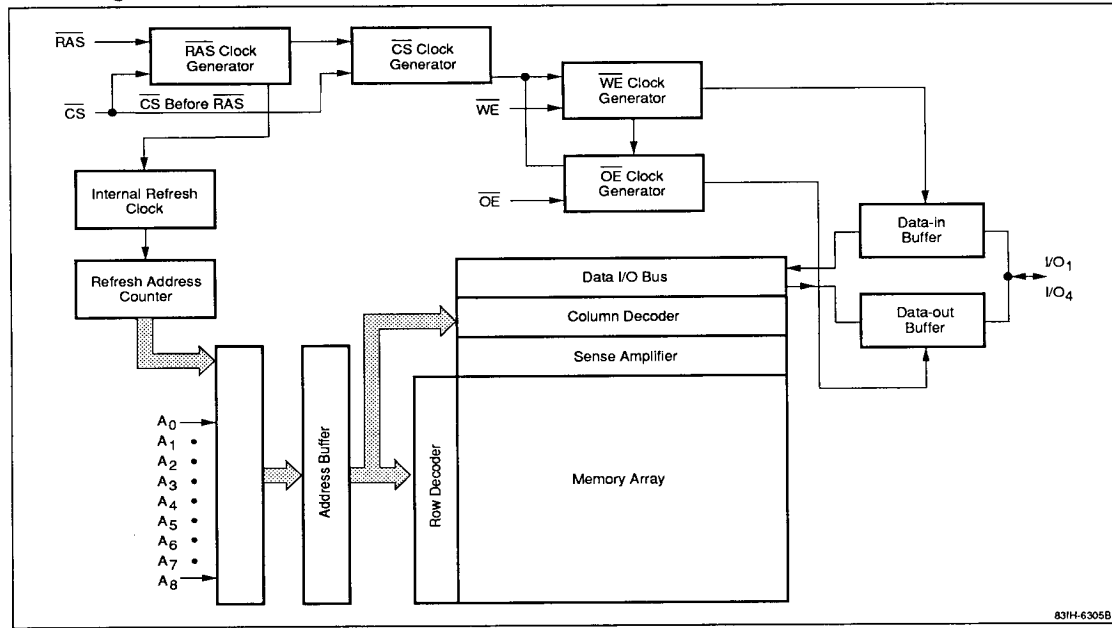
Voltage on any pin relative to GND, V _T	-1.0 to +7.0 V
Operating temperature, T _{OPR}	0 to +70 °C
Storage temperature, T _{STG}	-55 to +125 °C
Short-circuit output current, I _{OS}	50 mA
Power dissipation, P _D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Package
μPD424268C-60	60 ns	120 ns	35 ns	20-pin plastic DIP
C-70	70 ns	130 ns	40 ns	
C-80	80 ns	160 ns	45 ns	
C-10	100 ns	190 ns	55 ns	
μPD424268LA-60	60 ns	120 ns	35 ns	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	40 ns	
LA-80	80 ns	160 ns	45 ns	
LA-10	100 ns	190 ns	55 ns	
μPD424268V-60	60 ns	120 ns	35 ns	20-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	160 ns	45 ns	
V-10	100 ns	190 ns	55 ns	

Block Diagram



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DC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = +5.0 \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} \geq V_{IH} \text{ (min)}; I_O = 0 \text{ mA}$
				1.0	mA	$\overline{RAS} = \overline{CS} \geq V_{CC} - 0.2 \text{ V}; I_O = 0 \text{ mA}$
Input leakage current	$I_{I(L)}$	-10		10	μA	$V_{IN} = 0 \text{ V to } V_{CC}$; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	-10		10	μA	D_{OUT} disabled; $V_{OUT} = 0 \text{ V to } V_{CC}$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 4.2 \text{ mA}$
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -5 \text{ mA}$

AC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	-60		-70		-80		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}, \overline{CS}$ cycling; $t_{RC} = t_{RC} \text{ min (Note 5)}$
Operating current, RAS-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CS} = V_{IH}$; $t_{RC} = t_{RC} \text{ min (Note 5)}$
Operating current, static-column cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS} = \overline{CS} = V_{IL}$; $t_{RSC} = t_{RSC} \text{ min or } t_{WSC} = t_{WSC} \text{ min (Note 5)}$

AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Operating current, CS before RAS refresh cycle, average	I _{CC5}		90		80		70		60	mA	RAS cycling; t _{RC} = t _{RC} min (Note 5)
Access time from column address	t _{AA}		30		35		40		50	ns	(Notes 7, 10)
Column address hold time referenced to RAS (rising edge)	t _{AH}	15		15		15		15		ns	
Column address setup time	t _{ASC}	0		0		0		0		ns	
Row address setup time	t _{ASR}	0		0		0		0		ns	
Column address to WE delay time	t _{AWD}	50		55		65		80		ns	(Note 17)
Access time from CS (falling edge)	t _{CAC}		20		20		20		25	ns	(Notes 7, 9, 10)
Column address hold time	t _{CAH}	15		17		20		20		ns	
CS hold time for CS before RAS refresh cycle	t _{CHR}	15		15		15		20		ns	
CS precharge time	t _{CP}	10		10		10		10		ns	
CS to RAS precharge time	t _{CRP}	10		10		10		10		ns	(Note 13)
CS pulse width	t _{CS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
CS hold time	t _{CSH}	60		70		80		100		ns	
CS setup time for CS before RAS refresh cycle	t _{CSR}	10		10		10		10		ns	
CS to WE delay	t _{CWD}	40		40		45		55		ns	(Note 17)
Write command to CS lead time	t _{CWL}	15		15		20		20		ns	
Data-in hold time	t _{DH}	15		15		20		20		ns	(Note 16)
Data-in setup time	t _{DS}	0		0		0		0		ns	(Note 16)
Access time from OE	t _{OEA}		20		20		20		25	ns	(Note 7)
OE data delay time	t _{OED}	15		15		20		25		ns	
OE command hold time	t _{OEH}	0		0		0		0		ns	
OE to RAS inactive setup time	t _{OES}	0		0		0		0		ns	
Output turnoff delay from OE	t _{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output buffer turnoff delay	t _{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output hold time from address	t _{OH}	5		5		5		5		ns	
Output enable time from WE	t _{OW}		25		25		25		25	ns	(Note 7)
Access time from WE	t _{PWA}		60		70		80		100	ns	(Notes 7, 18)

AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{WE}$	t _{PWH}	60		70		80		100		ns	
Access time from $\overline{RAS}$	t _{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t _{RAD}	15	30	15	35	17	40	17	50	ns	(Note 10)
Row address hold time	t _{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t _{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t _{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t _{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t _{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CS}$	t _{RCH}	0		0		0		0		ns	(Note 14)
Read command setup time	t _{RCS}	0		0		0		0		ns	
Refresh period	t _{REF}		8		8		8		8	ms	Addresses A ₀ - A ₈
$\overline{RAS}$ precharge time	t _{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t _{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t _{RRH}	10		10		10		10		ns	(Note 14)
Static-column read cycle time	t _{RSC}	35		40		45		55		ns	(Note 6)
$\overline{RAS}$ hold time	t _{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t _{RSW}	75		85		95		115		ns	
Read-write cycle time	t _{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t _{RWD}	80		90		105		130		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t _{RWL}	20		20		25		30		ns	
Static-column read-modify-write cycle time	t _{RWSC}	85		95		110		135		ns	(Note 6)
Rise and fall transition time	t _T	3	50	3	50	3	50	3	50	ns	(Note 4)
$\overline{WE}$ to column address delay time	t _{WAD}	20	30	22	35	25	40	25	50	ns	(Note 18)
Write-per-bit hold time	t _{WBH}	10		10		10		10		ns	
Write-per-bit setup time	t _{WBS}	0		0		0		0		ns	
Write command hold time	t _{WCH}	15		15		15		20		ns	
Write command setup time	t _{WCS}	0		0		0		0		ns	(Note 17)

AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Write-per-bit mask data hold time	t_{WH}	10		10		10		10		ns	
Write-per-bit mask data setup time	t_{WS}	0		0		0		0		ns	
Write invalid time	t_{WI}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 15)
Static-column write cycle time	t_{WSC}	35		40		45		55		ns	(Note 6)

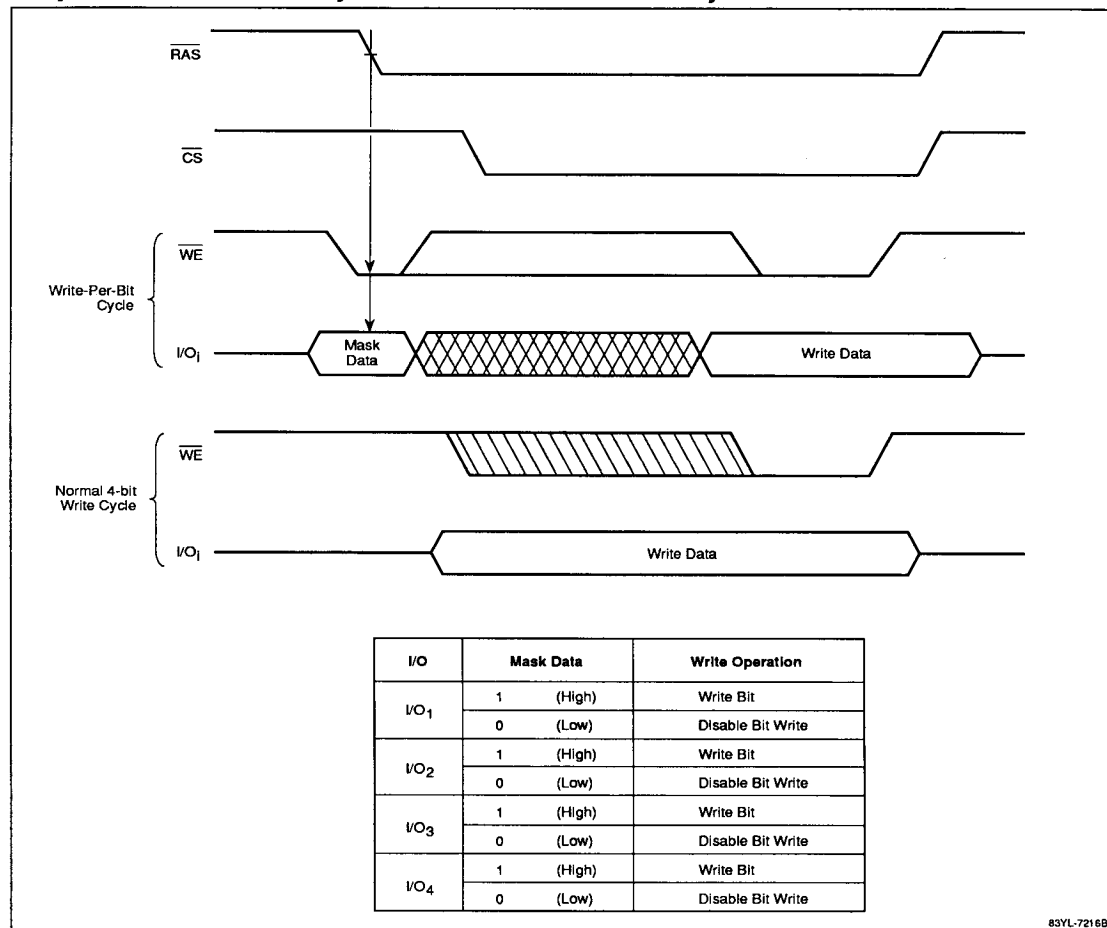
Notes:

- (1) All voltages are referenced to GND.
- (2) An initial pause of 100 μs is required after power-up, followed by any eight RAS cycles, before proper device operation is achieved.
- (3) AC measurements assume $t_T = 5$ ns.
- (4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- (5) I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$ -only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each static-column cycle.
- (6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70^\circ\text{C}$) is assured.
- (7) Load = 2 TTL (-1 mA, $+4$ mA) loads and 100 pF ($V_{OH} = 2.4$ V, $V_{OL} = 0.4$ V).
- (8) Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.
- (9) Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
- (10) If $t_{RAD} \geq t_{RAD}(\text{max})$, then the access time is defined by t_{AA} .
- (11) $t_{OFF}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL} .
- (12) Operation within the $t_{RCD}(\text{max})$ limit assures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than $t_{RCD}(\text{max})$, then access time is controlled exclusively by t_{CAC} , t_{AA} , or t_{OEA} .
- (13) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles preceded by any cycle.
- (14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- (15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.
- (16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.
- (17) t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$, and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.
- (18) If $t_{WAD} \leq t_{WAD}(\text{max})$, then the access time is defined by t_{PWA} .

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 4-bit word. The mask is loaded from the four I/O lines at the falling edge of RAS if $\overline{WE} = V_{IL}$. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If an I/O line is low, the corresponding bit does not change. A mask loaded during static-column operation will remain set and active for each write cycle that executes while RAS remains low. The mask may be changed at the falling edge of $\overline{RAS}$ only.

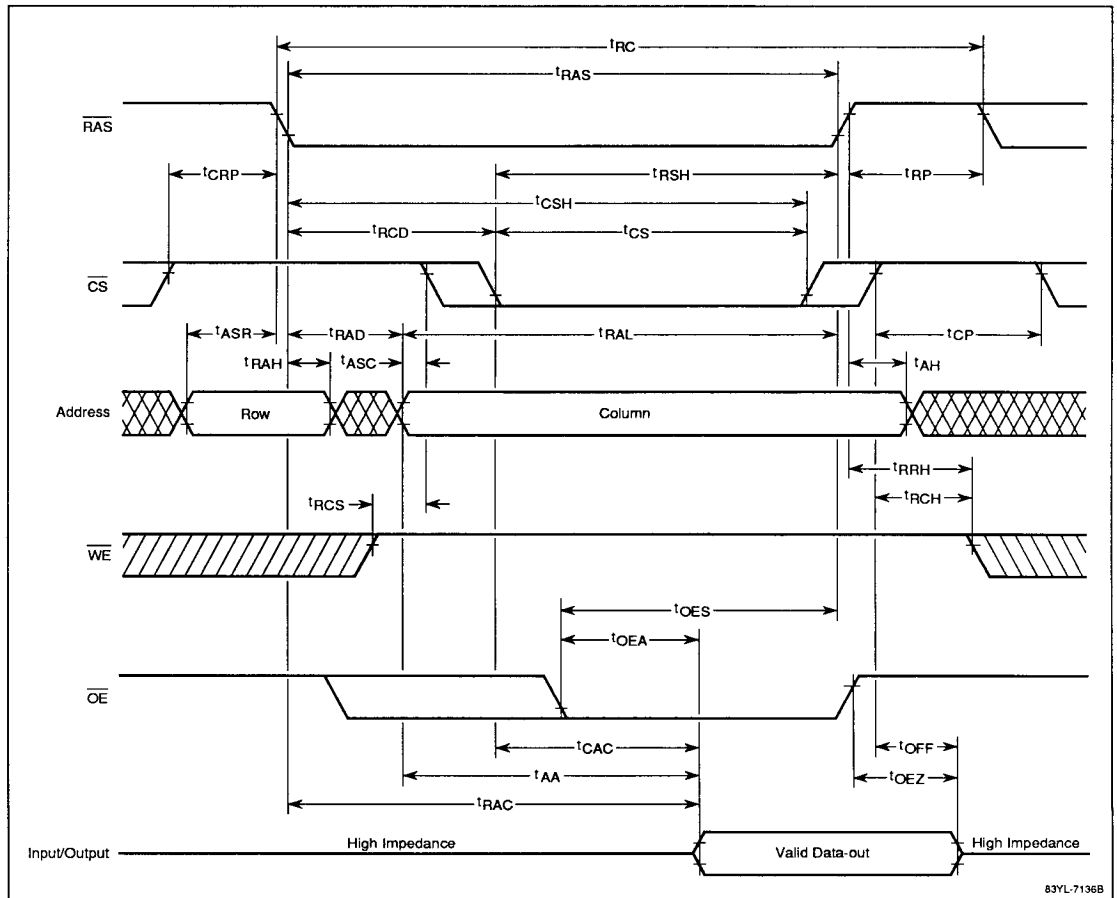
Comparison of Write-Per-Bit Cycle Versus Standard 4-Bit Write Cycle



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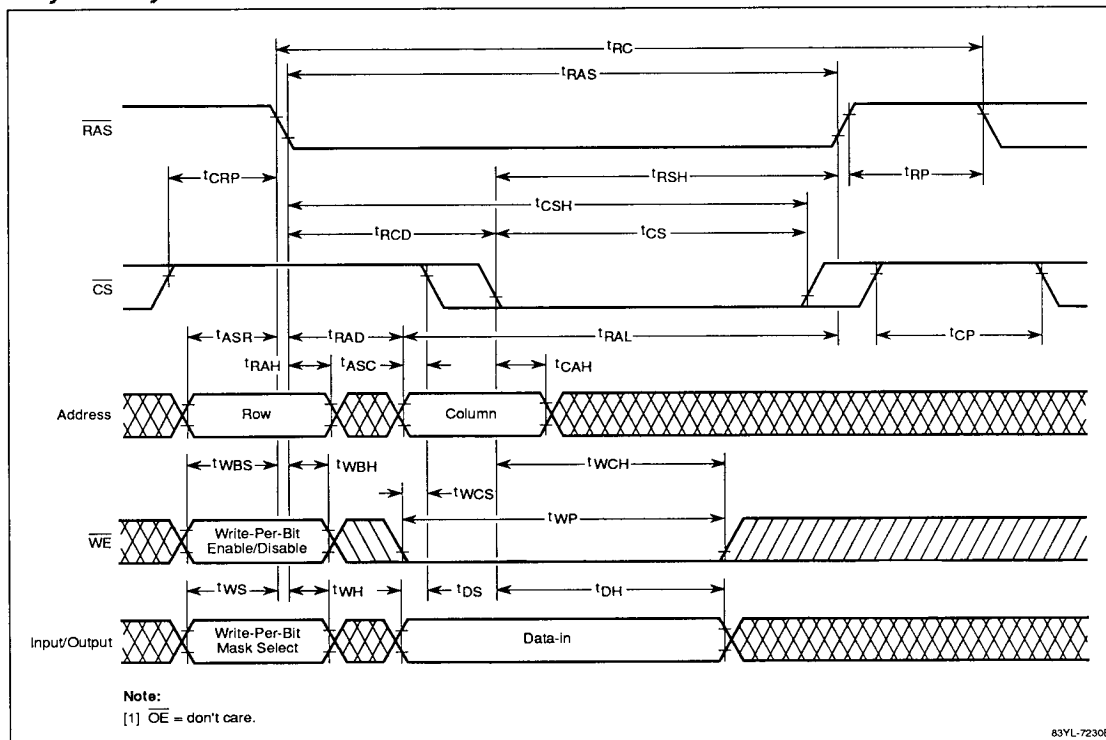
Timing Waveforms

Read Cycle



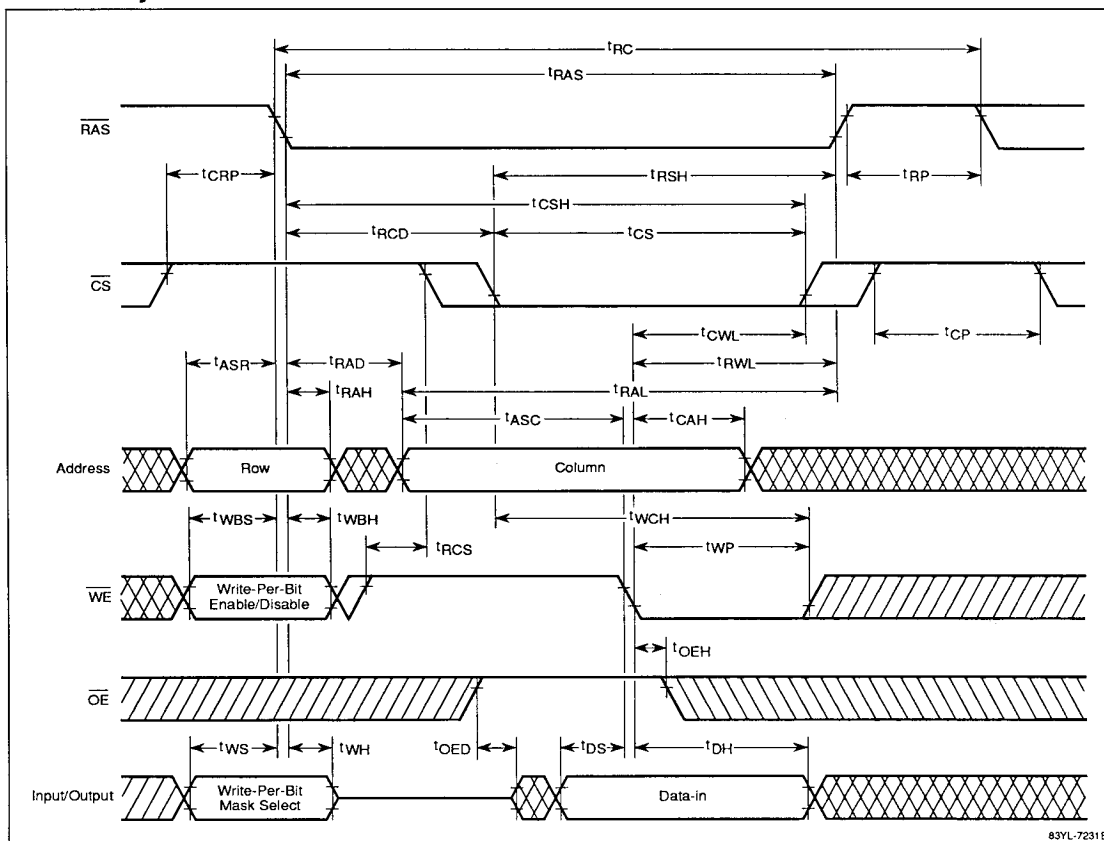
Timing Waveforms (cont)

Early Write Cycle



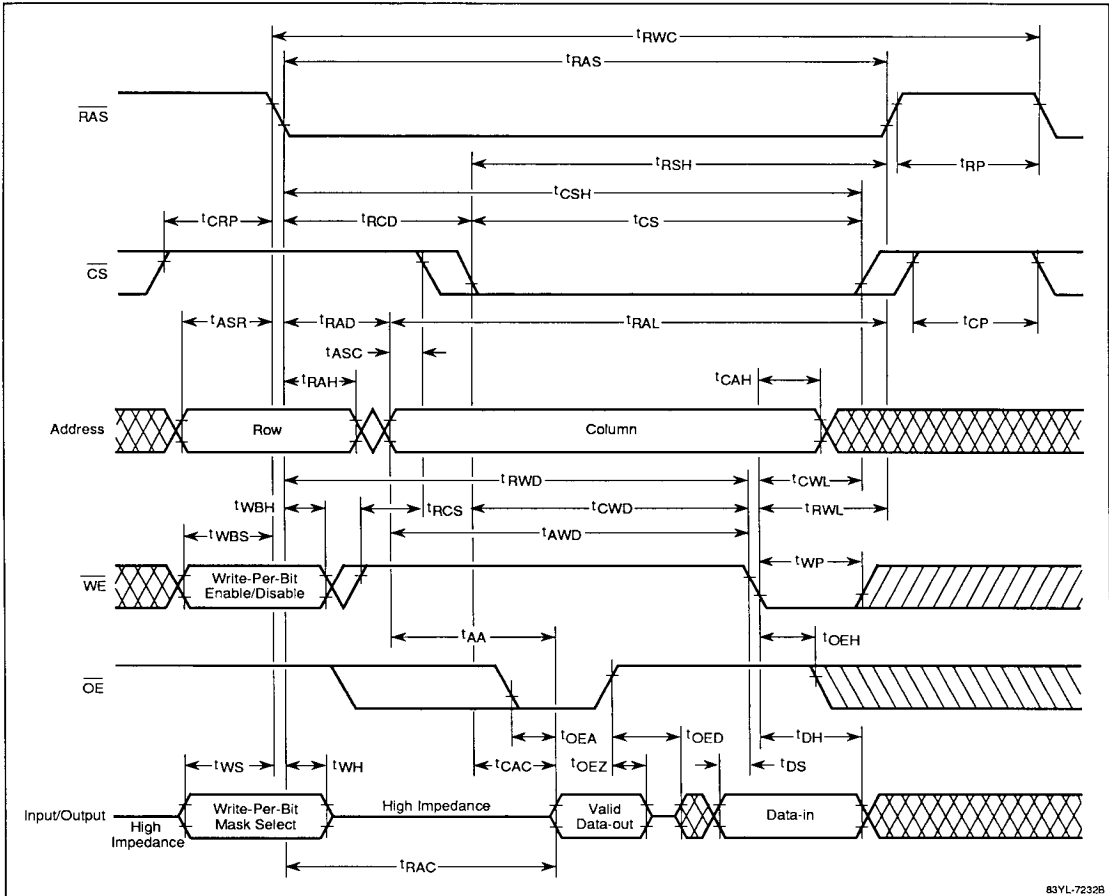
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

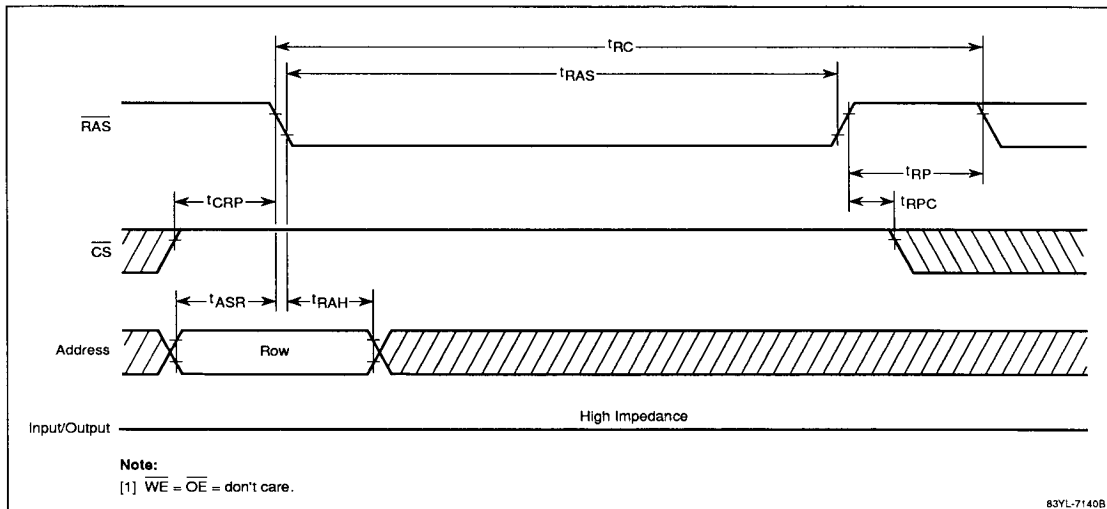
Read-Write/Read-Modify-Write Cycle



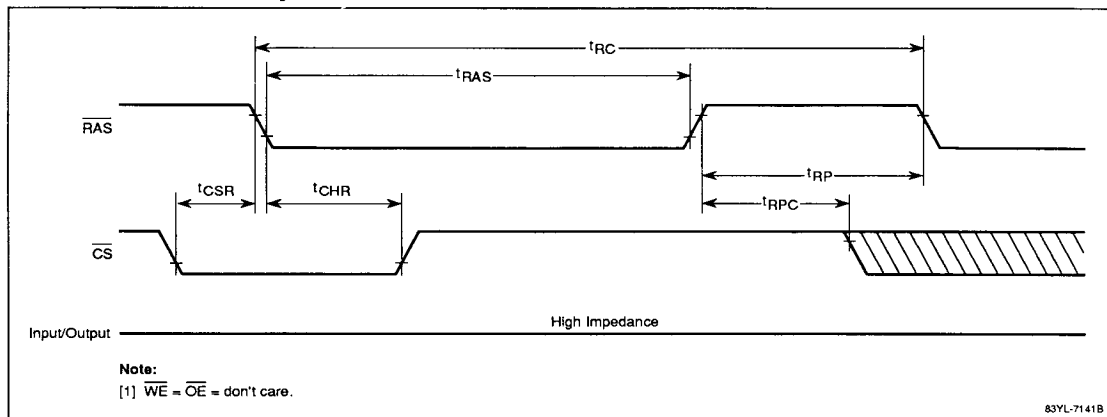
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Timing Waveforms (cont)

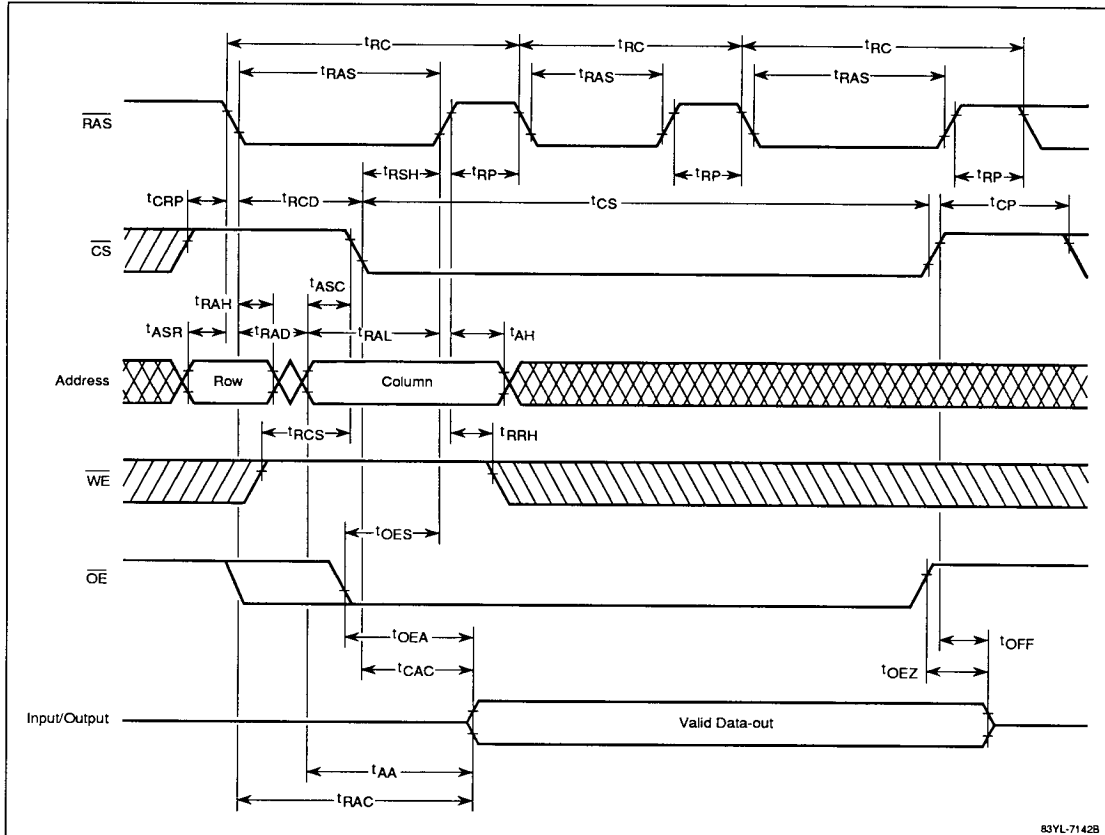
RAS-Only Refresh Cycle



$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

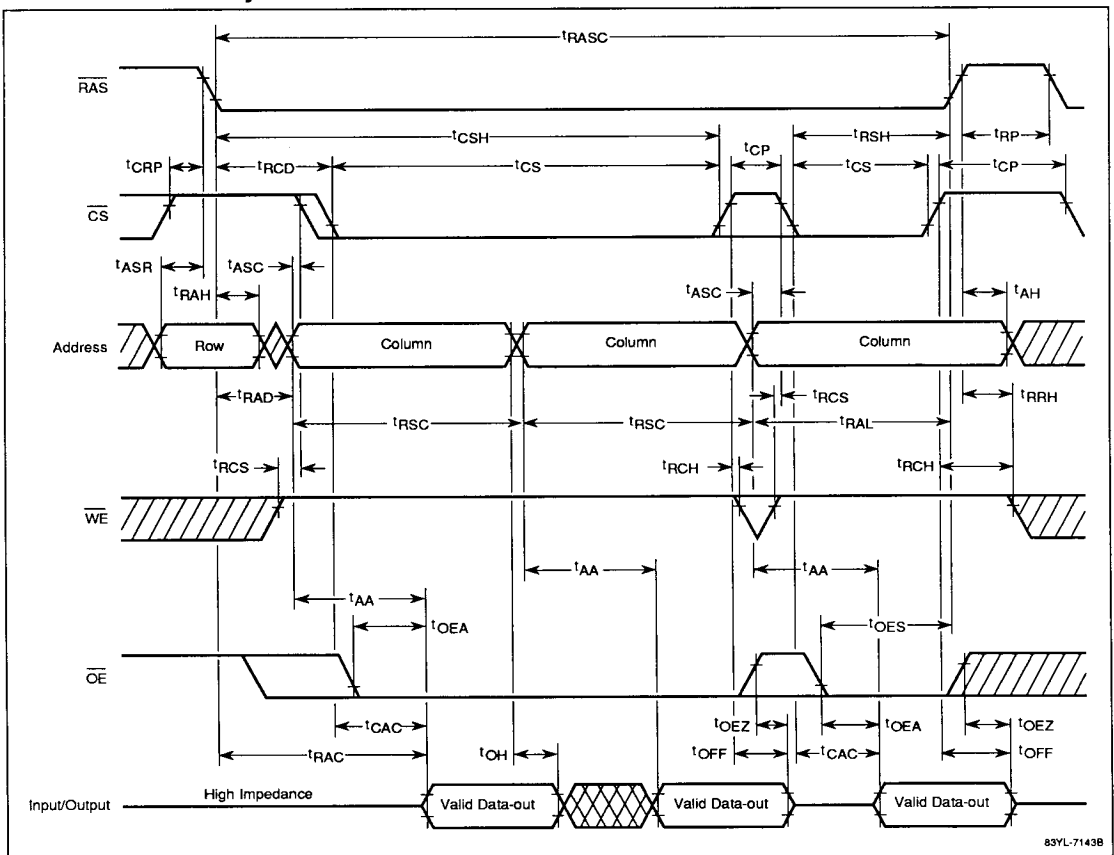


Hidden Refresh Cycle

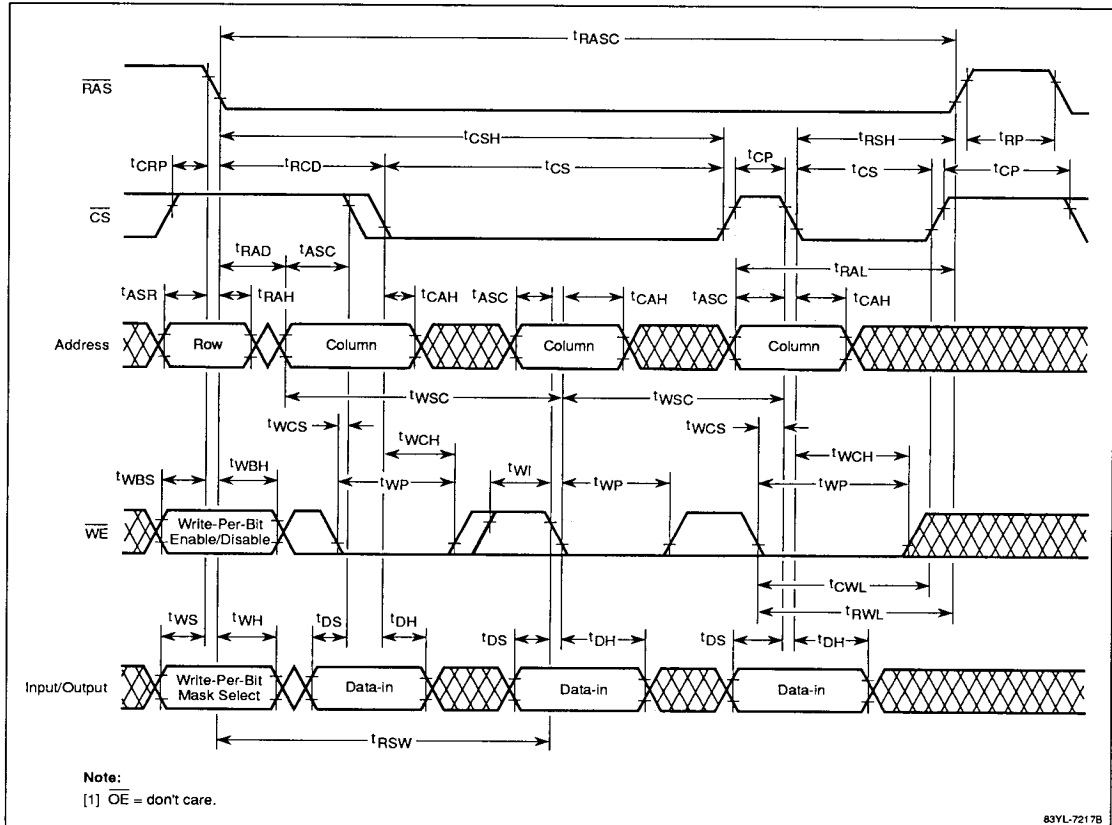


Timing Waveforms (cont)

Static-Column Read Cycle



Static-Column Early Write Cycle



Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle

