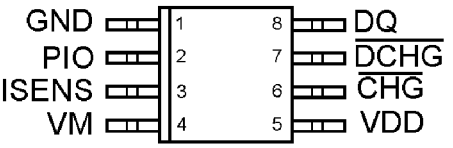
DALLAS SEMICONDUCTOR

DS2442
2-Cell Li-Ion Battery Manager

FEATURES

- Provides all identification, information, instrumentation and protection functions needed in a lithium-ion battery pack
- Supports two-cell battery packs
- Protects cells from:
  - overvoltage (overcharge)
  - undervoltage (overdischarge)
  - overcurrent (charging and discharging)
  - high temperatures (thermal runaway)
- Built-in cell-balancing support circuitry
- Current accumulator tracks remaining battery capacity in 0.5% increments
- Voltage measurement with 10 mV accuracy
- Temperature measurement with ±2°C accuracy eliminates need for thermistor
- 32-byte user memory stores battery data
- 64-bit ROM ID uniquely identifies each battery pack
- 1-Wire™ interface carries all commands and data via a single wire
- Programmable alarm warns when cells are nearly discharged
- Programmable I/O pin supports LEDs, vibration motors and other features
- Operating temperature range: -40°C to +85°C
- 10kV ESD rating

PIN ASSIGNMENT



150 MIL 8-PIN SOIC

PIN DESCRIPTION

GND	Ground
PIO	Programmable I/O Pin
ISENS	Current Sense Input
VM	Voltage Monitor Input
V_{DD}	Power Supply Input (2.4V to 10V)
$\overline{CHG}$	Charge Control Output
$\overline{DCHG}$	Discharge Control Output
DQ	Data I/O (1-Wire Interface)

DESCRIPTION

The DS2442 2-Cell Li-Ion Battery Manager provides all essential functions for monitoring, protecting and managing two-cell lithium-ion battery packs. The DS2442 constantly measures cell voltages, current, and temperature, and automatically takes action to disable charging and/or discharging of the cells to protect them when undesirable conditions arise.

Via its 1-Wire interface, the DS2442 provides the host system access to identification information, status data, configuration and control settings, instrumentation registers, and general purpose data storage. Each DS2442 has a factory-programmed 64-bit ROM ID which allows the host system to verify the authenticity of the battery pack as well as a factory-programmed 16-bit manufacturing ID which can be used to encode assembly location, cell chemistry and other information. A full set of status information in the DS2442 keeps the host informed about protection conditions, remaining capacity and other matters. Configuration and control fields in the device allow the host to disable charging and/or discharging, put

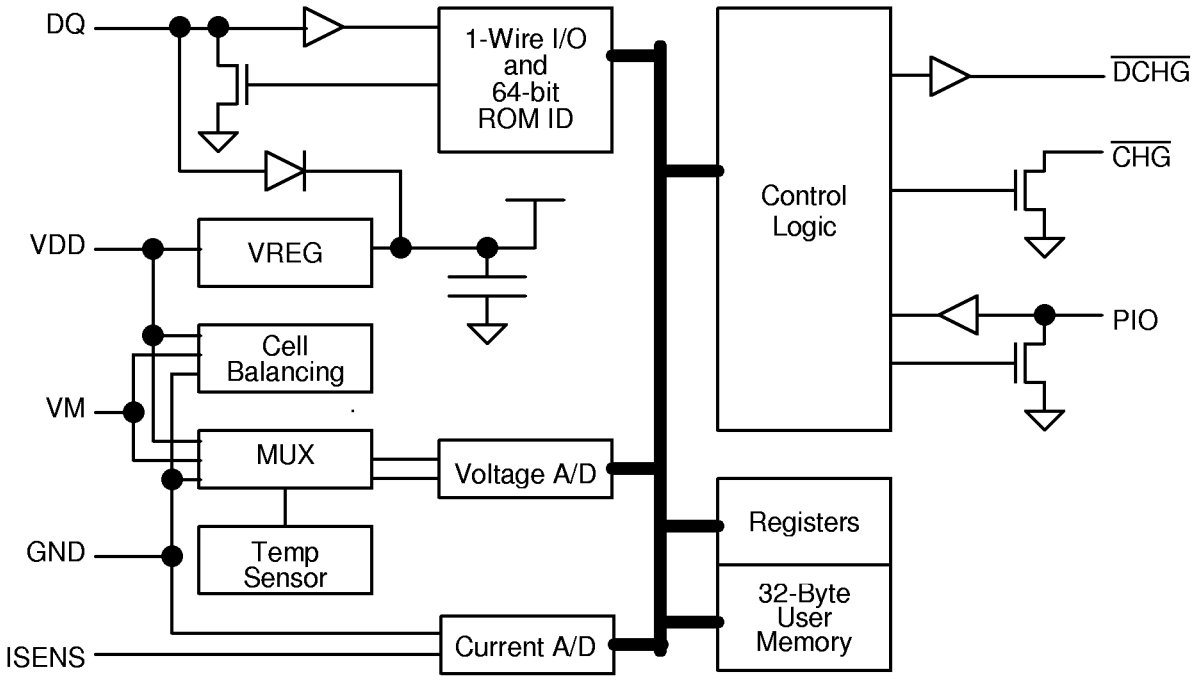
the battery pack in a low-power mode, implement cell balancing, and set various timing parameters. In addition, instrumentation registers on the chip present the host with high-accuracy temperature, voltage, and current measurements as well as information on remaining capacity and cycle life. Thirty-two bytes of general purpose memory in the DS2442 are available for storing pack-specific information.

When either cell voltage reaches the undervoltage cutoff, the DS2442 automatically enters a low-power mode in which it consumes only 1µA of battery current. When a battery charger is applied to the pack, the DS2442 automatically leaves its low-power mode to support charging. A refresh feature in the DS2442 allows even the most severely discharged battery packs to be refreshed and recharged. The DS2442 also features a programmable I/O pin that allows the host system to sense and control other electronics in the pack, such as vibration motors, speakers and LEDs.

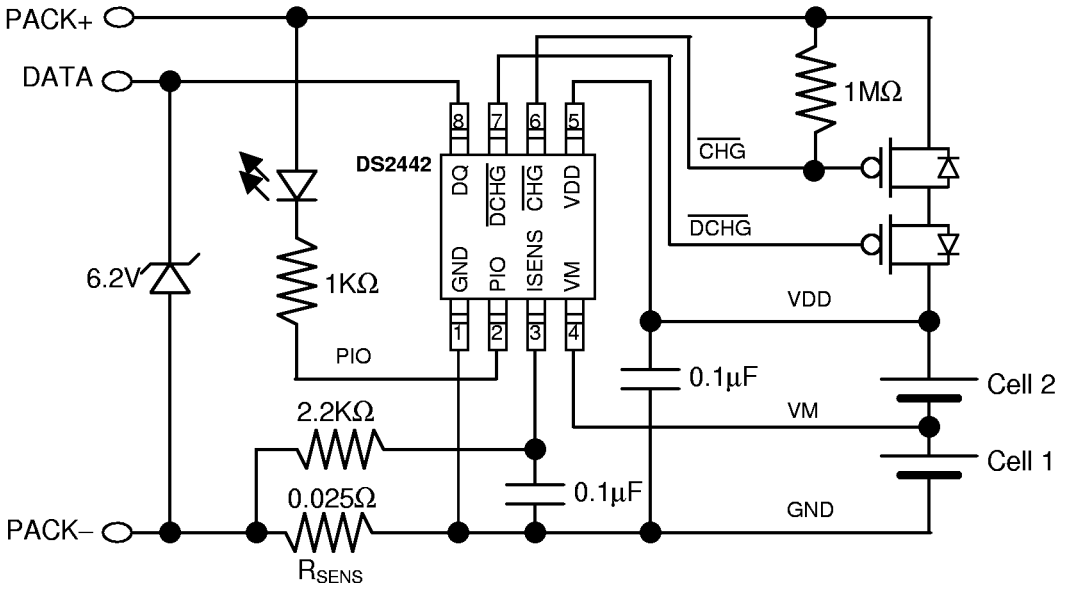
DETAILED PIN DESCRIPTION Table 1

Pin	Symbol	Description
1	GND	**Ground.** System voltage reference. Connect this pin to the most negative terminal of the cell stack and to one side of the current sense resistor.
2	PIO	**Programmable Digital I/O.** Use this user-definable pin to control features such as a vibration motor or an LED driver, or to monitor an input signal such as a tamper-sensing circuit.
3	ISENS	**Current Sense Input.** The DS2442 measures the voltage between this pin and GND to calculate the current flowing through the external sense resistor. Connect this pin through an RC low-pass filter to the PACK- side of the sense resistor.
4	VM	**Voltage Monitor Input.** The DS2442 uses this pin along with the V_{DD} and GND pins to monitor the voltage of the cells. Connect the negative terminal of the lower battery to GND and the positive terminal to VM. Then connect the negative terminal of the upper battery to VM and the positive terminal to V_{DD}. (The lower cell must be connected first.)
5	V_{DD}	**Power Supply Input.** The DS2442 draws operating power through this pin and uses this pin along with the VM and GND pins to monitor the voltage of the cells. Voltage on this pin must be between 2.4V and 10V for proper operation.
6	$\overline{CHG}$	**Charge Control Output.** Controls an external p-channel charge protection FET. Open-drain output driver.
7	$\overline{DCHG}$	**Discharge Control Output.** Controls an external p-channel discharge protection FET. Push-pull output driver.
8	DQ	**Data Input/Output.** 1-Wire data line. Parasite power supply for memory read/write operations. DS2442 power supply in Refresh Mode. Open-drain output driver. Connect this pin to the DATA terminal of the battery pack. In the host system, connect a 5 kΩ pullup from the DATA terminal to the PACK+ terminal.

BLOCK DIAGRAM Figure 1



APPLICATION EXAMPLE Figure 2



The circuit in Figure 2 depicts the DS2442 in a two-cell battery pack application. The circuit employs two p-channel power MOSFETs as charge and discharge protection switches along with a 1 MΩ pullup resistor to PACK+ to turn off the charge FET. The DS2442 tracks current in and out of the pack by measuring the voltage across the sense resistor R_{SENS} (i.e., the voltage on ISENS with respect to GND). The 0.1µF capacitor and 2.2 kΩ resistor on the ISENS pin form a low-pass filter to aid current measurement and accumulation. The diagram shows how the PIO pin can be used to drive an LED to implement a state-of-charge display. A zener diode limits the maximum voltage at the DQ terminal in the event that the pullup voltage is higher than the specified maximum DQ input voltage. Although the DS2442 has a 10 kV ESD rating, this diode is recommended to clamp ESD events safely outside the IC.

OVERVIEW

The DS2442 Block Diagram in Figure 1 shows the six major components of the DS2442:

- 1-Wire I/O port and 64-bit ROM ID
- Battery voltage A/D converter and monitor logic
- Battery current A/D converter and monitor logic
- Temperature sensor
- Registers and memory
- Control logic and outputs

CONFIGURATION

The DS2442 is designed to manage two-cell lithium-ion battery packs (see the application example in Figures 2). When assembling two-cell battery packs, the cell between VM and GND (Cell 1 in Figure 2) must be connected before the cell between V_{DD} and VM (Cell 2 in Figure 2) to ensure that the DS2442 correctly senses the number of cells attached.

POWER-ON RESET

The DS2442 executes a power-on reset (POR) whenever the voltages on both the VDD and DQ pins are below V_{POR} and then one or both voltages rise above V_{POR}. This includes the case where lithium-ion cells are first attached to the DS2442 with DQ low or unconnected. During a POR, the DS2442 sets the $\overline{POR}$ bit in the Configuration Register to logic 0, locks Page 0 memory against accidental overwrite, and loads default values into the following registers from laser ROM:

- Control Register
- Delay Timing Register
- Discharge Termination Warning Register
- Manufacturing ID Register
- Configuration Register

Also during a POR, the DS2442 sets the Temperature, Voltage, and Current registers to their most negative values, as shown in Table 2.

POR REGISTER VALUES Table 2

Register	Value	
	decimal	hex
Temperature	-128°C	80h
Voltage, Lower Cell	0 mV	0000h
Voltage, Upper Cell	0 mV	0000h
Current	-5.12C	FE00h

After reloading and resetting all of the registers mentioned above, the DS2442 enters its normal mode of operation, measuring voltage, current and temperature and reacting accordingly.

LI-ION PROTECTION CIRCUITRY

During normal operation, the DS2442 constantly monitors cell voltages, pack current and pack temperature to protect the cells from overcharge (overvoltage), overdischarge (undervoltage), excessive charge and discharge currents (overcurrent), and thermal runaway (overtemperature). The DS2442 monitors for and protects against each of these conditions with separate circuitry in order to properly protect lithium-ion cells from any single condition or combination of conditions that can arise. Conditions and DS2442 responses are described in the sections below and summarized in Table 3 and Figure 3.

LI-ION PROTECTION CONDITIONS AND DS2442 RESPONSES Table 3

Condition Name	Activation			Release	
	Threshold	Delay	Response	Threshold	Delay
Overvoltage	$V_{CELL1} > V_{OV}$ OR $V_{CELL2} > V_{OV}$	t_{OVD}	$\overline{CHG}$ off	$V_{CELL1} < V_{CE}$ AND $V_{CELL2} < V_{CE}$	0
Undervoltage	$V_{CELL1} < V_{UV}$ OR $V_{CELL2} < V_{UV}$	t_{UVD}	$\overline{CHG}$ off, $\overline{DCHG}$ high, Low Power Mode	exit Low Power Mode AND $V_{CELL1} > V_{UV}$ AND $V_{CELL2} > V_{UV}$	0
Overcurrent, Charge	$V_{ISENS} < -V_{OC}$	t_{OCD}	$\overline{CHG}$ off	none	t_{REL}
Overcurrent, Discharge	$V_{ISENS} > V_{OC}$	t_{OCD}	$\overline{DCHG}$ high	none	t_{REL}
	$V_{ISENS} > V_{SC}$	t_{SCD}			
Overtemp	$T_{MEAS} > T_{TRIP}$	0	$\overline{CHG}$ off, $\overline{DCHG}$ high	$T_{MEAS} < T_{TRIP} - T_{HYS}$	0

($V_{CELL1} = V_{DD}$ - VM. V_{CELL2} = VM. T_{MEAS} = measured temperature.)

Overvoltage. If the voltage of either cell exceeds overvoltage threshold V_{OV} for a period longer than overvoltage delay t_{OVD}, the DS2442 shuts off the external charge FET and sets the overvoltage protection flag, OV, in the Status Register. When both cell voltages fall below charge enable threshold V_{CE}, the DS2442 clears the OV flag and enables the charge FET (unless another protection condition prevents it). Except when a discharge protection condition also occurs, discharging remains enabled during overvoltage, with the discharge path consisting of the channel of the discharge FET and the body diode of the charge FET.

Undervoltage. If the voltage on either cell drops below undervoltage threshold V_{UV} for a period longer than undervoltage delay t_{UVD}, the DS2442 shuts off the charge and discharge FETs, asserts the undervoltage protection flag, UV, in the Status Register, and enters Low Power Mode to minimize the load it presents to the cells. See the section on Low Power Mode for more details.

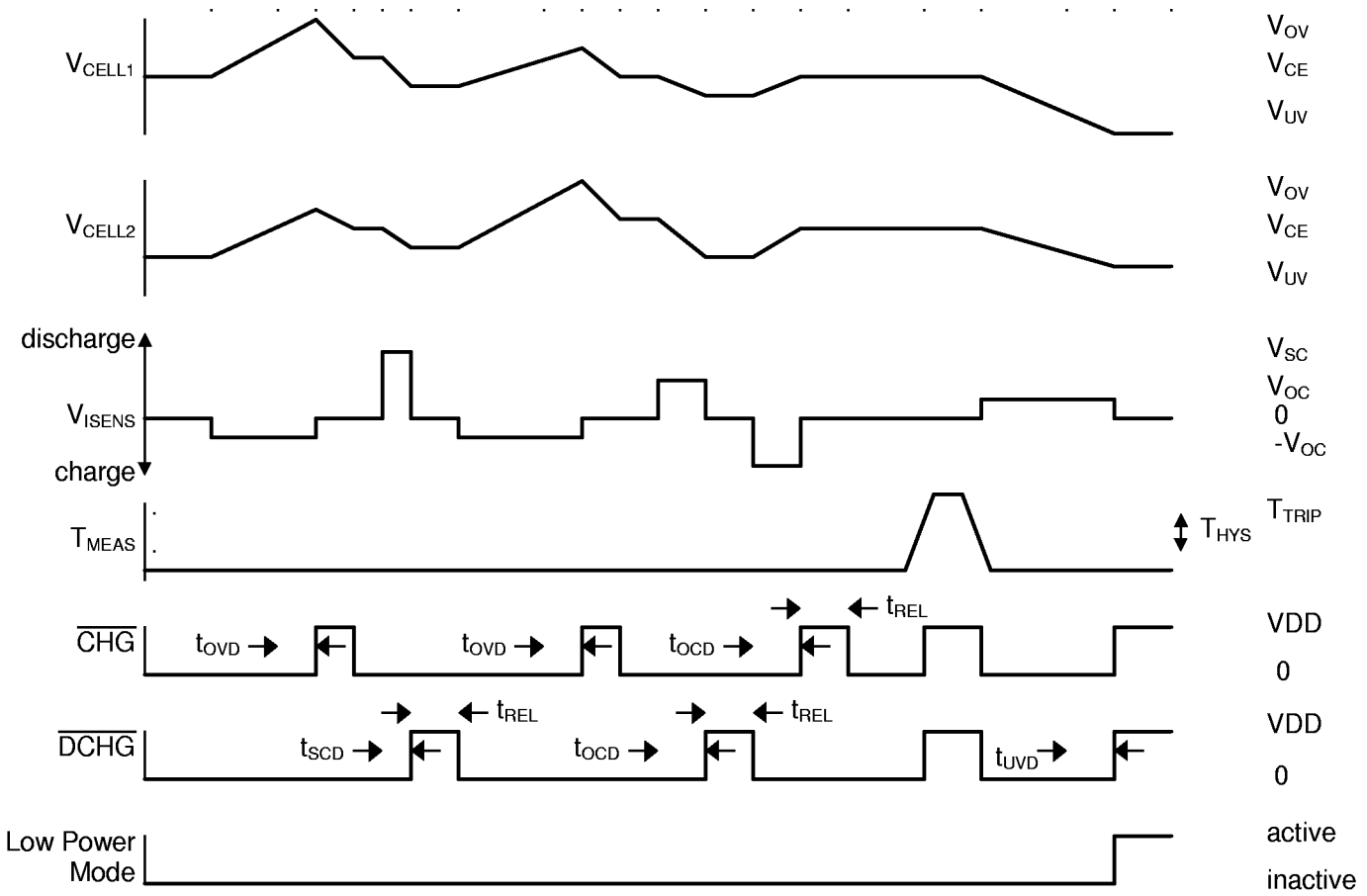
Overcurrent, Charge Direction. The voltage on the I_{SENS} pin with respect to GND (V_{ISENS}) is the voltage across current sense resistor R_{SENS}. If V_{ISENS} is less than $-V_{OC}$ (V_{OC} is the overcurrent threshold) for a period longer than overcurrent delay t_{OCD}, the DS2442 shuts off the external charge FET and sets the overcurrent protection flag, OC, in the Status Register. After the expiration of release delay t_{REL}, the DS2442 clears the OC flag and enables the charge FET (unless another protection condition prevents it). If the overcurrent condition persists for t_{OCD} after the charge FET is enabled, the DS2442 responds again. If the overcurrent condition persists indefinitely, the DS2442 cycles between protecting and releasing until an overvoltage condition arises in one or both cells. Except when a discharge protection condition

also occurs, discharging remains enabled during charge-direction overcurrent, with the path consisting of the channel of the discharge FET and the body diode of the charge FET.

Overcurrent, Discharge Direction. If V_{ISENS} is greater than overcurrent threshold V_{OC} for a period longer than overcurrent delay t_{OCD}, or if V_{ISENS} is greater than short circuit threshold V_{SC} for a period longer than short circuit delay t_{SCD}, the DS2442 shuts off the external discharge FET and sets the overcurrent protection flag, OC, in the Status Register. After the expiration of release delay t_{REL}, the DS2442 clears the OC flag and enables the discharge FET (unless another protection condition prevents it). If the overcurrent condition persists for t_{OCD} or t_{SCD} after the discharge FET is enabled, the DS2442 responds again. If the condition persists indefinitely, the DS2442 cycles between protecting and releasing until an undervoltage condition arises in one or both cells. Except when a charge protection condition also occurs, charging remains enabled during discharge-direction overcurrent, with the path consisting of the channel of the charge FET and the body diode of the discharge FET.

Overtemperature. If the temperature of the DS2442 exceeds T_{TRIP}, the DS2442 immediately shuts off both the charge and discharge FETs and sets the overtemperature flag, OT, in the Status Register. After the temperature drops below T_{TRIP} - T_{HYS}, the DS2442 clears the OT flag and enables the charge and discharge FETs (unless another protection condition prevents it). This feature provides a secondary safety back-up mechanism beyond overvoltage and overcurrent protection.

LITHIUM-ION PROTECTION CIRCUITRY EXAMPLE WAVEFORMS Figure 3



Summary. All of the protection conditions described above are ORed together to affect the $\overline{CHG}$ and $\overline{DCHG}$ outputs. Taking the OV, UV and OT bits from the Status Register and considering the OC Status Register bit to be the logical OR of DOC (discharge overcurrent) and COC (charge overcurrent), the equations for $\overline{CHG}$ and $\overline{DCHG}$ are as follows:

$\overline{DCHG}$ = OT or DOC or UV or Low Power Mode
$\overline{CHG}$ = OT or COC or OV or Low Power Mode

LOW POWER MODE

The DS2442 enters Low Power Mode when an undervoltage condition exists on either lithium-ion cell or when the host system sets the LPM bit in the Control Register. While in Low Power Mode, the DS2442 shuts off the external charge and discharge FETs and turns off most of its internal circuitry to reduce its load on the cells to I_{DD1} (1 µA typical). The DS2442 stays in Low Power Mode until it is "awakened" by the attachment of a charger to the battery pack (voltage on $\overline{CHG}$ pin > VDD) or a high-to-low transition on the DQ pin. After either stimulus, the DS2442 powers up fully, makes initial measurements with the charge and discharge FETs off (to prevent charging until it can verify the cells are not overvoltage), and then returns to its normal mode of operation.

Charging from Low Power Mode. Charging an undervoltage pack is as simple as applying a charger to the pack. The presence of the charger automatically triggers the DS2442 to leave Low Power Mode, make initial measurements with the FETs off, and return to its normal mode of operation. Generally the DS2442 starts normal operation with the discharge FET off (because the cells are still undervoltage) and the charge FET on, which allows charging to proceed. If the charger pulls both cell voltages above undervoltage threshold V_{UV} before the expiration of undervoltage delay t_{UVD}, the DS2442 remains in its normal mode of operation and charging can continue. If one or both cells remain below V_{UV} for t_{UVD}, the DS2442 shuts off the charge and discharge FETs, asserts the UV flag, and returns to Low Power Mode. Once back in Low Power Mode, the presence of the charger again triggers the DS2442 to go back to its normal mode of operation where charging can continue for at least t_{UVD}. As long as the charger is applied to the pack, the DS2442 repeatedly cycles between its normal mode of operation (for t_{UVD}) and Low Power Mode (for approximately 28 ms) until both cells have been charged above V_{UV}. After both cells are above V_{UV}, the DS2442 remains in its normal mode of operation and charging continues normally.

REFRESHING UNDERVOLTAGE PACKS

In the worst-case undervoltage situation, a battery can be so far discharged that V_{DD} is outside the specified operating range of the DS2442, leaving the DS2442 without a power supply and unable to allow the charging necessary to correct the situation. The Refresh bit (RFSH) in the Control Register and the ability to parasitically steal power from the DQ pin are features that allow any DS2442-based battery pack to be refreshed from even the deepest undervoltage situation.

Parasite Power. As is the case for many Dallas 1-Wire products, the DS2442 can, using an on-chip capacitor, parasitically steal enough power from the DQ line to support register and memory accesses even with no voltage present on the V_{DD} pin. DQ must be pulled up to at least 3V, and maximum pulse width specifications must be met to ensure proper parasite-powered operation.

Refresh Bit. Setting the RFSH bit in the Control Register to logic 1 causes the DS2442 to mask the effect of undervoltage on the $\overline{CHG}$ output, stay in the normal mode of operation (and out of Low Power Mode), and power all of its circuitry only from the DQ pin. Because all DS2442 circuitry is powered

from DQ when this bit is set, DQ must subsequently remain high to support this mode of operation. A high-to-low transition on DQ clears the RFSH bit.

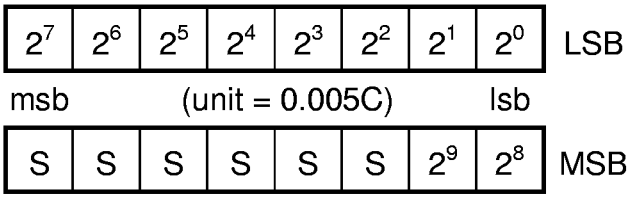
Refreshing Undervoltage Packs. To charge severely undervoltage DS2442-based battery packs, apply a charger to the pack and read the Status Register to check the value of the UV bit. If UV=1, set the RFSH bit to logic 1 and pull DQ high to function as the DS2442's power supply. The DS2442 draws power from DQ and allows charging to occur as long as DQ remains high and no charge protection condition arises. To periodically check whether the undervoltage condition remains, read the Status Register to check the value of UV. (The first high-to-low transition on DQ during the Status Register read will clear the RFSH bit. If the undervoltage condition remains, as soon as the RFSH bit is cleared the DS2442 will return to Low Power Mode, disabling charging.) If UV is still logic 1, set RFSH to logic 1 and pull DQ high to continue charging. Loop in this manner until UV=0. When UV is low, the DS2442 will be in its normal operating mode and will support normal charging.

CURRENT MEASUREMENT

The DS2442 measures current flow into and out of the battery pack by measuring the voltage across sense resistor R_{SENS} connected between the PACK- terminal of the battery pack and the negative terminal of the battery. To accomplish this, the GND pin on the DS2442 is connected to the negative terminal of the battery and the ISENS pin is connected, through a low-pass filter, to the PACK- terminal of the pack. To measure current, the DS2442 actually measures V_{ISENS} with respect to GND. In its normal mode of operation, the DS2442 takes current measurements continuously with no assistance from the host system. In Low Power Mode, the DS2442 suspends current measurements.

The DS2442 measures the voltage drop across R_{SENS} using a digital sampling and accumulation scheme. The use of an external low-pass filter with a corner frequency below 2 kHz on the V_{ISENS} pin is recommended. The current is measured with a signed 11-bit (0.005C) resolution. The last completed measurement is placed in the Current Register using a sign-extended, two's-complement format. This register is not updated while it is being read by the host system to ensure that only the last completed conversion is read out. The Current Register is scaled such that a count of 200_{10} corresponds to a current of 1C. Thus, the range of current flow that can be measured is from -5.115C (discharging) to +5.115C (charging). The sign (S) of the current measurement, indicating charge or discharge, resides in the six most significant bits of the Current Register, as shown in Figure 4. Some example Current Register values are shown in Table 4.

CURRENT REGISTER FORMAT Figure 4



CURRENT REGISTER EXAMPLE VALUES Table 4

Battery Current	Register Value	
	Binary	Hex
+5.115C	0000 0011 1111 1111	03 FF
+1.000C	0000 0000 1100 1000	00 C8
+0.100C	0000 0000 0001 0100	00 14
+0.010C	0000 0000 0000 0010	00 02
+0.005C	0000 0000 0000 0001	00 01
0C	0000 0000 0000 0000	00 00
-0.005C	1111 1111 1111 1111	FF FF
-0.010C	1111 1111 1111 1110	FF FE
-0.100C	1111 1111 1110 1100	FF EC
-1.000C	1111 1111 0011 1000	FE 38
-5.115C	1111 1100 0000 0001	FC 01

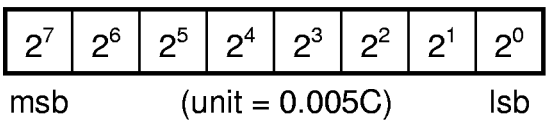
The value of current sense resistor R_{SENS} should be selected to provide a 48.8 mV drop across it at a 1C rate. This value corresponds to 1 LSB = 244 µV. Different voltage-to-current scaling factors can be used to accommodate a larger dynamic range, higher resolution, or less voltage loss at a given discharge current. Alternate scaling factors must be properly interpreted by the host system.

CURRENT ACCUMULATORS

The DS2442 maintains three different current accumulator registers. The Integrated Current Accumulator (ICA) facilitates battery gas gauging and remaining capacity reporting by tracking the net current flow into and out of the battery. The Charge Current Accumulator (CCA) and Discharge Current Accumulator (DCA) support battery end-of-life estimation by accumulating total charge current and discharge current respectively. Each completed current measurement increments or decrements the ICA and increments the CCA (if current is positive) or increments the DCA (if current is negative).

Integrated Current Accumulator. The ICA is an 8-bit, read/write, up/down counter with 0.005C resolution that represents the amount of capacity remaining in the battery in terms of the full capacity (1C), normalized to a count of 200_{10}. Thus, an ICA count of 200_{10} represents 1C of charge, 100% of capacity, or a fully charged battery. A count of 0 represents 0% of capacity, or a fully discharged battery. The ICA does count up to 255_{10}, but does not roll over if incremented above an equivalent of 1.27C. Because batteries have an inherent charging inefficiency, the ICA may read higher than 200 (or 1C) after a full charge. Two methods are available for handling ICA values greater than 200: (1) reduce the ICA to 200 after a full charge, or (2) leave the ICA value alone and instead create a scaling factor of 200÷ICA for use by the host system. Figure 5 shows the format of the ICA register.

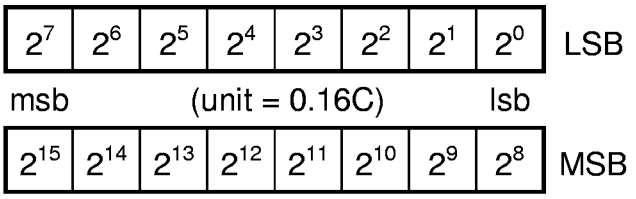
ICA REGISTER FORMAT Figure 5



Charge and Discharge Current Accumulators. The Charge Current Accumulator (CCA) is a 16-bit, read/write, up-only counter with 0.16C resolution which accumulates the total charging current the battery pack has seen since the CCA was last reset. It is only updated when current through sense resistor

R_{SENS} is positive; i.e., when the battery is being charged. Similarly, the Discharge Current Accumulator (DCA) is a 16-bit, read/write, up-only counter with 0.16C resolution which accumulates the total discharging current the battery pack has seen since the DCA was last reset. Each counter is incremented at the rate of once per 0.16C, thus allowing six updates for each complete charge or discharge cycle. Figure 6 shows the format of the CCA and DCA registers.

CCA AND DCA REGISTER FORMAT Figure 6



The ICA, CCA and DCA can be disabled by setting the ACC bit in the Configuration Register to logic 0. When the accumulators are disabled, bytes 0, 2, 3, 4 and 5 of Page 2 become general purpose memory available to the host system.

Current Accumulator Threshold. In order to allow accumulator adjustments for offset versus resolution, two Configuration Register bits (TH1 and TH2) can be used to set a threshold on the measured current below which the ICA, CCA and DCA won't accumulate. When the threshold is set larger than the maximum offset voltage of the internal A/D converter, the offset is effectively ignored by the accumulators. A higher threshold setting offers maximum granularity and is recommended for high-current use. A lower threshold setting is used to enhance long-term accuracy for light-duty battery use. Table 5 enumerates the available threshold settings.

CURRENT ACCUMULATOR THRESHOLD SETTINGS Table 5

TH2	TH1	Threshold
0	0	None (default)
0	1	±2 LSB
1	0	±4 LSB
1	1	±8 LSB

DISCHARGE TERMINATION WARNING

The DS2442 continuously compares the ICA value with the alarm threshold stored in the read/write Discharge Termination Warning (DTW) Register. If the ICA drops below the DTW threshold, the DS2442 sets the DTW flag in the Status Register to provide a low battery warning to the host system. The DTW flag is also set if either cell voltage falls below the discharge warning threshold V_{DW}. The V_{DW} voltage threshold provides a back-up warning in case extreme operating conditions cause ICA inaccuracy. The default DTW threshold value (0.000C) can be overwritten at any time. For a custom default value, consult the factory. The DTW Register has the same format as the ICA (see Figure 5).

VOLTAGE MEASUREMENT

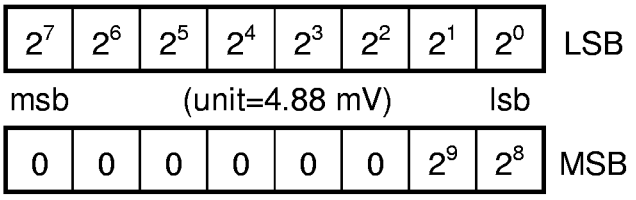
In its normal mode of operation, the DS2442 continuously measures the voltage of both cells. Voltage measurements are unsigned and have a 10-bit resolution. Each conversion cycle performs 32 consecutive voltage samples within 6.9ms (typical) for each cell. If the AVG bit of the Configuration Register is set to logic 1 (default), the average value of the 32 samples is stored in the appropriate Voltage Register. If the AVG bit is set to logic 0, the minimum value of the 32 samples is stored. This is summarized in Table 6. In Low Power Mode, the DS2442 suspends voltage measurements.

VOLTAGE CONVERSION CONFIGURATION SETTINGS Table 6

AVG bit	Result Stored
1	Average
0	Minimum

The Voltage Registers have the format shown in Figure 7.

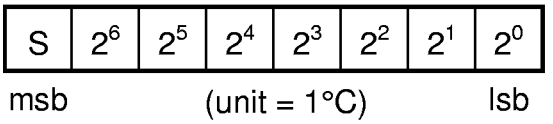
VOLTAGE REGISTER FORMAT Figure 7



TEMPERATURE MEASUREMENT

In its normal mode of operation, the DS2442 continuously measures pack temperature. After each measurement, 2's-complement temperature information is stored in the 8-bit Temperature Register. The Temperature Register has the format shown in Figure 8. Some example Temperature Register values are shown in Table 7. In Low Power Mode, the DS2442 suspends temperature measurements.

TEMPERATURE REGISTER FORMAT Figure 8



TEMPERATURE REGISTER EXAMPLE VALUES Table 7

Battery Temperature	Register Value	
	Binary	Hex
+85°C	0101 0101	55 h
+25°C	0001 1001	19 h
+2°C	0000 0010	02 h
+1°C	0000 0001	01 h
0°C	0000 0000	00 h
- 1°C	1111 1111	FF h
- 2°C	1111 1110	FE h
- 25°C	1110 0111	E7 h
- 40°C	1101 1000	D8 h

PROGRAMMABLE I/O

The programmable I/O port of the DS2442 allows for control and sensing of in-pack components such as speakers, vibration motors, FETs, LEDs and tamper control circuits. Using the Channel Access command with the R/$\overline{W}$ Configuration Register bit set to logic 1 (read), the host system can monitor the state of the PIO pin by having the DS2442 translate logic 0s and logic 1s on the PIO pin into 1-Wire Read 0 and Read 1 timeslots on the DQ pin. Using the Channel Access command with R/$\overline{W}$ set to logic 0 (write), the host system can control the PIO pin by having the DS2442 translate 1-Wire Write 0 and Write 1 timeslots on the DQ pin into logic 0s and logic 1s on the PIO pin. The DS2442 turns off the PIO output driver when it enters Low Power Mode or when a pack disconnection is sensed. See the Channel Access paragraph of the Function Command section and the Pack Disconnection section for more information.

CELL BALANCING

The DS2442 supports cell balancing—the compensation for cell voltage mismatch—by providing host-controlled low-current bleeding circuits across the upper and lower cells of the battery. The upper-cell bleeding circuit is enabled by setting the HBL bit in the Control Register to logic 1. The lower-cell bleeding circuit is enabled by setting the LBL bit in the Control Register to logic 1. The DS2442 resets both HBL and LBL to logic 0 when it enters Low Power Mode or when a pack disconnection is sensed. See the Pack Disconnection section for more information.

PACK DISCONNECTION

The DS2442 can sense the disconnection of the battery pack from the host system. When the pack is separated from the host, the 1-Wire bus pullup resistor in the host is disconnected from the DQ pin of the DS2442. Once this pullup has been removed, a small current sink (<5 µA) on the DQ pin pulls the DQ pin low. If the DQ pin remains low for more than 2 * $t_{RSTL,MAX}$ (approximately 2 ms) the DS2442 realizes that the extended low period represents a pack disconnection. When a pack disconnection is detected, the DS2442 turns off the PIO output driver and resets control bits HBL and LBL to logic 0 to turn off the cell balancing bleed circuits. These circuits are turned off so that they don't drain the cells during long disconnection periods. All other DS2442 circuitry remains active during pack disconnection.

64-BIT ROM ID

Each DS2442 contains a unique, factory-lasered ROM ID code that is 64 bits long. The first 8 bits of this ID are the 1-Wire family code (25h for DS2442). The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits (see Figure 9). The 64-bit ROM ID and the 1-Wire I/O circuitry

built into the device allow the DS2442 to adhere to the 1-Wire protocol detailed in the 1-Wire Bus System section below.

ROM ID FORMAT Figure 9

8-bit CRC	48-bit Serial Number	8-Bit Family Code (25h)

The ROM ID also aids in battery pack clone protection. The upper 12 bits of the 48-bit serial number within the ROM ID can be laser-programmed to indicate that a given DS2442 and the battery pack in which it resides belong to a particular manufacturer. Once reserved, a given pattern in this 12-bit field belongs exclusively to the company that requested it. That company can then create a software routine in their host systems to check for their specific pattern in the ROM ID each time a battery pack is attached to the host system. If the pack fails to produce a 64-bit ID with the proper pattern, it must be an unauthorized clone pack. The host system can then take appropriate action, such as refusing to operate from the clone pack or refusing to charge it.

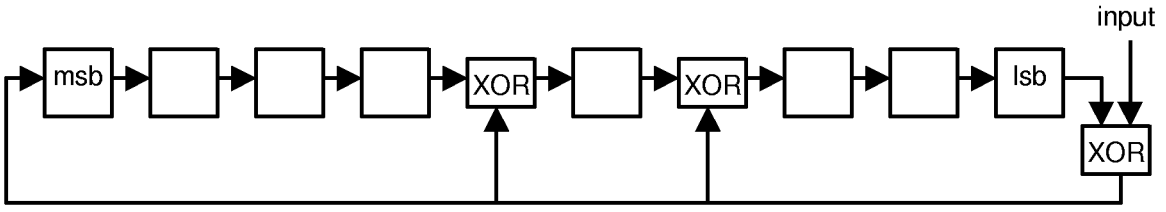
CRC GENERATION

The DS2442 has an 8-bit CRC stored in the most significant byte of its 64-bit ROM ID. To ensure error-free transmission of the ROM ID, the host system can compute a CRC value from the first 56 bits of the ROM ID and compare it to the CRC from the DS2442. The host system is responsible for verifying the CRC value and taking action as a result. The DS2442 does not compare CRC values and does not prevent a command sequence from proceeding as a result of a CRC mismatch. Proper use of the CRC can result in a communication channel with a very high level of integrity.

The 1-Wire CRC can be generated by the host using a circuit consisting of a shift register and XOR gates as shown in Figure 10, or it can be generated in software. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in Application Note 27 entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products. "

In the circuit in Figure 10, the shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value.

1-WIRE CRC GENERATOR BLOCK DIAGRAM Figure 10



MEMORY

The DS2442 contains four 32-byte pages of memory. See the page descriptions below, the Memory Map in Figure 11, and the detailed register descriptions on the pages that follow for more information. Locations labeled "Reserved" in the Memory Map always read out FFh.

Page 0 contains the Control, Delay Timing, Discharge Termination Warning, and Manufacturing ID registers. All of these registers are read/write except the read-only Manufacturing ID. This entire page can be locked against accidental write access by setting the LOCK bit of the Status Register to logic 1. During a power-on reset (POR) event, the DS2442 loads each of these registers with default values stored in laser ROM and set the Status Register LOCK bit. See the Discharge Termination Warning section and the sections on the Control, Delay Timing and Manufacturing ID registers for more details.

Page 1 is read only and contains the Status Register, the Temperature Register and the Voltage Registers. See the Temperature Measurement, Voltage Measurement and Status Register sections for more information.

Page 2 contains the Configuration Register, the Current Register and the ICA, CCA and DCA. During a power-on reset event the DS2442 loads the Configuration Register with its default value stored in laser ROM. The ICA, CCA and DCA registers power-on in a random state and should be set to a known value by the host system. See the Current Measurement, Current Accumulators and Configuration Register sections for more details.

Page 3 contains 32 bytes of user memory. All memory locations in this page power-on in a random state.

Since the registers and memory in the DS2442 are full-CMOS SRAM, battery pack data is maintained by battery power even during undervoltage conditions. If the battery pack is externally short-circuited, causing temporary battery voltage collapse, power circuitry in the DS2442 maintains acceptable voltage to the memory for at least t_{SCD} to allow time for the lithium-ion protection circuitry to turn off the discharge FET and remove the cause of the supply voltage collapse.

All registers and user memory in the DS2442 can be read and written under all power supply conditions, including loss of voltage on the VDD pin, via the parasite-powered 1-Wire bus.

MEMORY MAP Figure 11

Page 0 (lockable)		Address	Read/White
Control Register		00 h	R/W
Delay Timing Register		01 h	R/W
Discharge Termination Warning		02 h	R/W
Manufacturing ID	LSB	03 h	R
	MSB	04 h	
Reserved		05 h ↓ 1F h	R
Page 1		**Address**	**Read/White**
Status Register		00 h	R
Temperature Register		01 h	R
Voltage Register, Lower Cell	LSB	02 h	R
	MSB	03 h	
Voltage Register, Upper Cell	LSB	04 h	R
	MSB	05 h	
Reserved		06 h ↓ 1F h	R
Page 2		**Address**	**Read/Write**
Integrated Current Accumulator		00 h	R/W
Configuration Register		01 h	R/W
Charge Current Accumulator	LSB	02 h	R/W
	MSB	03 h	
Discharge Current Accumulator	LSB	04 h	R/W
	MSB	05 h	
Current Register	LSB	06 h	R
	MSB	07 h	
Reserved		08 h ↓ 1F h	R
Page 3		**Address**	**Read/Write**
User Byte 0 ↓ User Byte 31		00 h ↓ 1F h	R/W

CONTROL REGISTER

The format of this register is shown in Figure 12. The function of each bit is described in detail in the paragraphs below.

CONTROL REGISTER FORMAT Figure 12

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LPM	RFSH	HBL	LBL	$\overline{\text{CHG}}$	$\overline{\text{DCHG}}$	CHE	DCHE

LPM - Low Power Mode. Setting this bit to logic 1 puts the DS2442 into Low Power Mode. See the section on Low Power Mode for more details. The default value is 0 (inactive).

RFSH - Refresh Mode. Setting this bit to logic 1 puts the DS2442 into Refresh Mode. See the section on Refreshing Undervoltage Packs for more information. A high-to-low transition on the DQ pin clears this bit to logic 0 and disables Refresh Mode.

HBL - Upper-cell bleeding. Setting this bit to logic 1 connects a low-current bleeding circuit across the upper cell (between VDD and VM) to support cell balancing. Setting this bit to logic 0 disconnects the bleeding circuit from the upper cell. The power-on default value is logic 0 (no bleeding).

LBL - Lower-cell bleeding. Setting this bit to logic 1 connects a low-current bleeding circuit across the lower cell (between VM and GND) to support cell balancing. Setting this bit to logic 0 disconnects the bleeding circuit from the lower cell. The power-on default value is logic 0 (no bleeding).

$\overline{\text{CHG}}$ - State of $\overline{\text{CHG}}$ output pin. This read-only bit mirrors the state of the $\overline{\text{CHG}}$ output pin.

$\overline{\text{DCHG}}$ - State of $\overline{\text{DCHG}}$ output pin. This read-only bit mirrors the state of the $\overline{\text{DCHG}}$ output pin.

CHE - Charge enable. Writing logic 0 to this bit disables charging ($\overline{\text{CHG}}$ output driver off, external charge FET off) regardless of cell or pack conditions. Writing logic 1 to this bit enables charging, subject to override by the presence of any protection conditions.

DCHE - Discharge enable. Writing logic 0 to this bit disables discharging ($\overline{\text{DCHG}}$ output driver off, external discharge FET off) regardless of cell or pack conditions. Writing logic 1 to this bit enables discharging, subject to override by the presence of any protection conditions.

DELAY TIMING REGISTER

The Delay Timing Register provides a means to configure each of the protection delay times—t_{REL}, t_{OVD}, t_{UVD}, and t_{OCD}—to one of four values, allowing the DS2442 to be fine-tuned for its application environment. The format of the register is shown in Figure 13. The standard default value loaded from laser ROM during power-on reset is 00h. Contact the factory for a different default value. See the Lithium-Ion Protection section above for more details on these timing values.

DELAY TIMING REGISTER FORMAT Figure 13

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REL		OVD		UVD		OCD	

REL - t_{REL} timing. This field indicates one of four settings for t_{REL}, the length of time that charging and discharging are disabled following the detection of overcurrent conditions. See Table 8 for REL values and corresponding t_{REL} timing.

OVD - t_{OVD} timing. This field indicates one of four settings for t_{OVD}, the delay time during which the voltage of a cell must remain above overvoltage threshold V_{OV} before charging is disabled due to an overvoltage condition. See Table 8 for OVD values and corresponding t_{OVD} timing.

UVD - t_{UVD} timing. This field indicates one of four settings for t_{UVD}, the delay time during which the voltage of a cell must remain below undervoltage threshold V_{UV} before the DS2442 disables charging and discharging and enters Low Power Mode. See Table 9 for UVD values and corresponding t_{UVD} timing.

OCD - t_{OCD} timing. This field indicates one of four settings for t_{OCD}, the delay time during which pack current must be too high ($V_{ISENS} > V_{OC}$ for discharge or $V_{ISENS} < -V_{OC}$ for charge) before charging or discharging is disabled due to an overcurrent condition. See Table 10 for OCD values and corresponding t_{OCD} timing.

REL AND OVD SETTINGS Table 8

REL, OVD	t_{REL}, t_{OVD} (ms)		
	Min	Typ	Max
00	384	512	640
01	768	1024	1280
10	1536	2048	2560
11	3072	4096	5120

UVD SETTINGS Table 9

UVD	t_{UVD} (ms)		
	Min	Typ	Max
00	24	32	40
01	48	64	80
10	96	128	160
11	192	256	320

OCD SETTINGS Table 10

OCD	t_{OCD} (ms)		
	Min	Typ	Max
00	1.5	2	2.5
01	3	4	5
10	6	8	10
11	12	16	20

STATUS REGISTER

The Status Register contains seven read-only status flags. Bit 7 of the register is read-only and always returns logic 1. The format of the register is shown in Figure 14. The various flags are described in the paragraphs below.

STATUS REGISTER FORMAT Figure 14

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	PIO	LOCK	OT	OV	UV	OC	DTW

PIO - State of the PIO pin. This flag mirrors the logic state of the PIO pin, regardless of whether PIO is set up as an input or an output. The PIO flag is updated every time Page 1 of memory (the page containing the Status Register) is accessed by the host system.

LOCK - Page 0 Lock. This flag indicates whether Page 0 is locked so that it cannot be written (LOCK=1) or unlocked for read/write access (LOCK=0). This bit is set and cleared by the execution of the Lock Register and Unlock Register commands. The power-on default value for this bit is logic 1 (locked).

OT - Overtemperature. This bit indicates the presence (OT=1) or absence (OT=0) of an overtemperature protection condition.

OV - Overvoltage. This bit indicates the presence (OV=1) or absence (OV=0) of an overvoltage protection condition.

UV - Undervoltage. This bit indicates the presence (UV=1) or absence (UV=0) of an undervoltage protection condition.

OC - Overcurrent. This bit indicates the presence (OC=1) or absence (OC=0) of an overcurrent protection condition.

DTW - Discharge Termination Warning. This status bit is set to logic 1 when the Integrated Current Accumulator (ICA) value drops below the Discharge Termination Warning (DTW) threshold or any cell voltage drops below discharge warning threshold V_{DW}. This bit is reset to logic 0 when the ICA is higher than the DTW threshold and the voltage of both cells is above V_{DW}.

CONFIGURATION REGISTER

The Configuration Register contains six read/write configuration bits. Bits 3 and 2 are read only and always return logic 1 when read. The format of the register is shown in Figure 15. The various bits are described in the paragraphs below.

CONFIGURATION REGISTER FORMAT Figure 15

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ACC	TH2	TH1	$\overline{POR}$	1	1	R/$\overline{W}$	AVG

ACC - Accumulator enable. Setting this bit to a logic 0 disables the ICA, CCA and DCA functions, freeing up bytes 0, 2, 3, 4 and 5 in Page 2 for general purpose use. A logic 1 (power-on reset default) in this bit enables the accumulators.

TH1, TH2 - Accumulator threshold bits. When the current accumulators are active, TH1 and TH2 select one of four accumulator threshold values. See Table 5 for possible threshold values.

$\overline{POR}$ - Power-on reset. A logic 0 in this bit indicates that a power-on reset has occurred. Writing a logic 1 resets this flag so that subsequent power-on reset events can be detected.

R/$\overline{W}$ - PIO pin read/write direction bit. Setting this bit to a logic 1 configures the DS2442 to allow the host system to read from the PIO pin using the Access Channel command. A logic 0 in this bit configures the device to allow the host system to write to the PIO pin using the Access Channel command. The power-on reset default value of this bit is logic 1 (read).

AVG - Voltage A/D sampling method. This bit controls whether the average value (logic 1) or the minimum value (logic 0) of each 32-sample group is stored in the Voltage Registers. The power-on reset default value is logic 1 (average).

THE MANUFACTURING ID

The value stored in this 16-bit read-only register can be laser-programmed by Dallas Semiconductor to provide pack customization. Fields in this register can encode information such as the pack manufacturer, assembly location, type of cells and number of cells. Unless a custom value is requested, the DS2442 ships with 0000h in this register. Contact the factory to request a custom Manufacturing ID value.

1-WIRE BUS SYSTEM

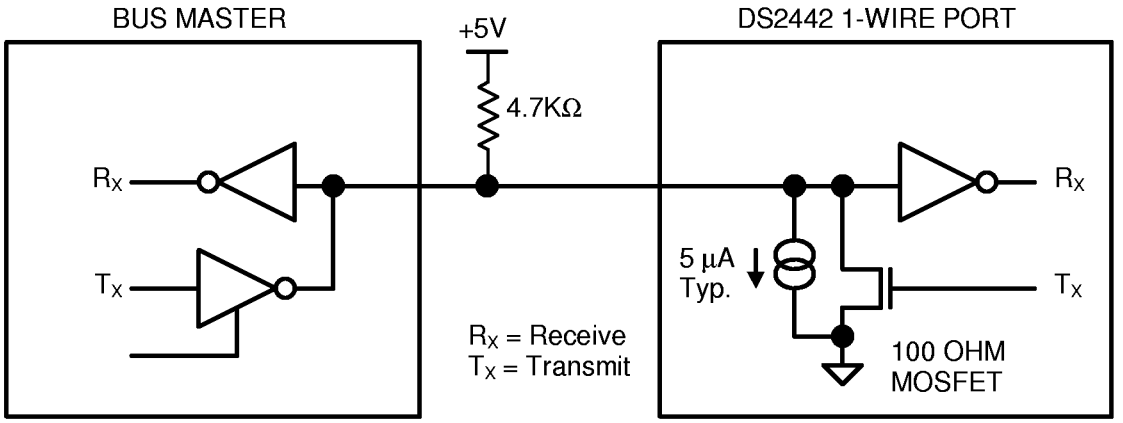
The 1-Wire bus is a system which has a single bus master and one or more slaves. A multi-drop bus is a 1-Wire bus with multiple slaves. A single-drop bus has only one slave device. In all instances, the DS2442 is a slave device. The bus master is typically a microcontroller in the host system. The discussion of this bus system below consists of three topics: Hardware Configuration, Transaction Sequence, and 1-Wire Signaling.

HARDWARE CONFIGURATION

Because the 1-Wire bus has only a single line, it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must connect to the bus with open-drain or tri-state output drivers. The DS2442 uses an open-drain output driver as part of the bi-directional interface circuitry shown in Figure 16. If a bi-directional pin is not available on the bus master, separate output and input pins can be tied together.

The 1-Wire bus must have a pullup resistor at the bus-master end of the bus. For short line lengths, the value of this resistor should be approximately 5 kΩ. The idle state for the 1-Wire bus is high. If, for any reason, a bus transaction must be suspended, the bus MUST be left in the idle state in order to properly resume the transaction later. If the bus is left low for more than 120 µs, slave devices on the bus begin to interpret the low period as a Reset Pulse, effectively terminating the transaction.

1-WIRE BUS INTERFACE CIRCUITRY Figure 16



TRANSACTION SEQUENCE

The protocol for accessing the DS2442 via the 1-Wire port is as follows:

- Initialization
- ROM Command
- Function Command
- Transaction/Data

The sections that follow describe each of these steps in detail.

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence consisting of a Reset Pulse transmitted by the bus master followed by a presence pulse simultaneously transmitted by the DS2442 and any other slaves on the bus. The presence pulse tells the bus master than one or more devices are on the bus and ready to operate. For more details, see the 1-Wire Signaling section below.

ROM COMMANDS

Once the bus master has detected the presence of one or more slaves, it can issue one of the four ROM Commands described below. The name of each ROM Command is followed by the eight-bit opcode for that command in square brackets. Figure 17 below presents a transaction flow chart of the four ROM Commands.

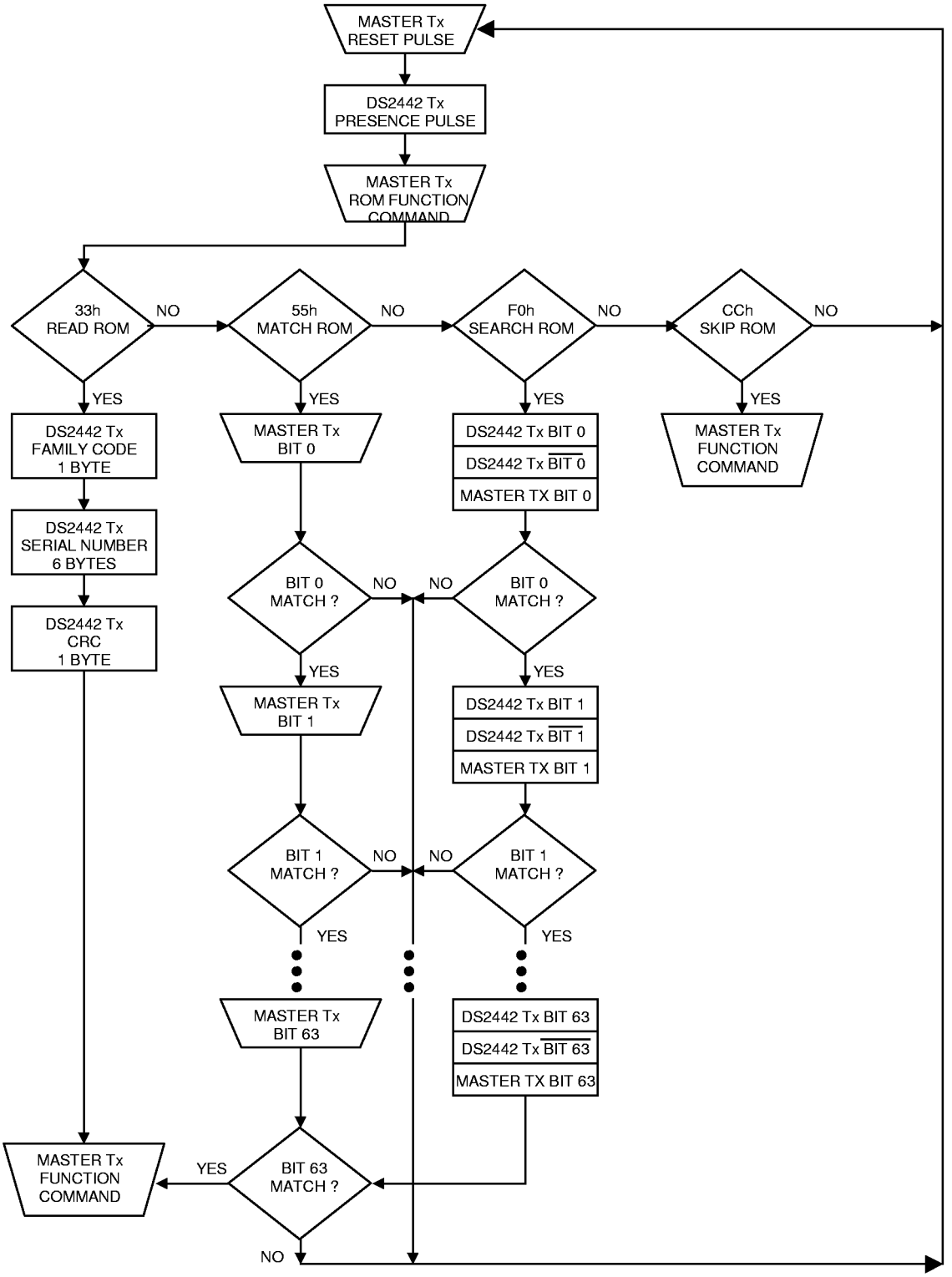
Read ROM [33h]. This command allows the bus master to read the DS2442's 8-bit family code (25h), unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result).

Match ROM [55h]. The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to specifically address one DS2442 on the 1-Wire bus. Only the DS2442 that exactly matches the 64-bit ROM sequence responds to the subsequent Function Command. All slaves that do not match the 64-bit ROM sequence wait for a reset pulse. This command can be used with one or more devices on the bus.

Skip ROM [CCh]. This command saves time when there is only one DS2442 on the bus by allowing the bus master to issue a Function Command without specifying the 64-bit ID of the slave. If more than one slave device is present on the bus and the subsequent Function Command instructs the slaves to send data to the master, a data collision occurs when all slaves transmit data at the same time.

Search ROM [F0h]. This command allows the bus master to use a process of elimination to identify the 64-bit ROM IDs of all slave devices on the bus. The ROM search process involves the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM ID. After one complete pass through all 64 bits, the bus master knows the ROM ID of one device. The remaining devices can then by identified on additional passes. See Chapter 5 of the Book of DS19xx iButton™ Standards for a comprehensive discussion of a ROM search, including an actual example.

ROM COMMAND FLOW CHART Figure 17



FUNCTION COMMANDS

After successfully completing one of the four ROM Commands, the bus master can access the features of the DS2442 with any of the six Function Commands described below. The name of each Function Command is followed by the 8-bit opcode for that command in square brackets.

Lock Register [43h]. This command locks (disables write access to) Page 0 memory and sets the LOCK bit in the Status Register.

Unlock Register [44h]. This command unlocks (enables write access to) Page 0 memory and clears the LOCK bit in the Status Register.

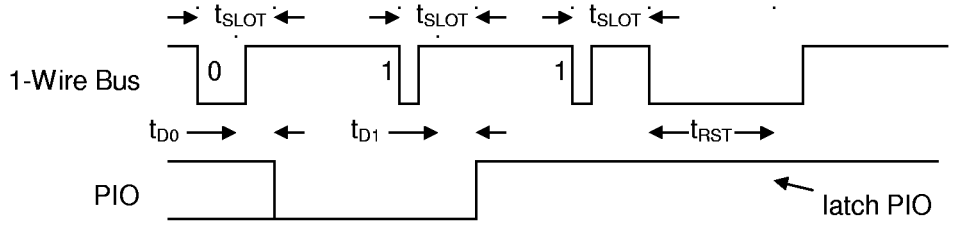
Read Register [BEh, XX]. This command reads the contents of page XX, starting at address 00h within the page. Valid page numbers are 00h through 03h. The page number byte must be entered immediately following the command opcode. The least significant bit from address 00h is available to be read immediately after the most significant bit of the page number has been entered. Reading proceeds automatically from address 00h to address 1Fh in the page. If the bus master continues to read beyond address 1Fh, the DS2442 continuously outputs logic 1. Data transfer may be terminated with a Reset Pulse at any point. The bus master need not read out whole pages or even whole bytes.

Write Register [4Eh, XX]. This command writes to page XX, starting at address 00h within the page. Valid page numbers are 00h, 02h and 03h (Page 1 is read-only). The page number byte must be entered immediately following the command opcode. Data to be written to address 00h must be entered immediately following the page number byte. The memory in the DS2442 is written a byte at a time, and data transfer may be terminated with a Reset Pulse at any byte boundary. Read-only bits and "Reserved" memory locations are not affected by the write operation. Incomplete bytes are not written.

Recall Setup [B8h]. This command reloads the power-on default values for the Control, Delay Timing, Discharge Termination Warning, Manufacturing ID and Configuration registers.

Channel Access [F5h]. This command directs the DQ bit stream to/from the PIO pin of the DS2442. If the $R/\overline{W}$ bit in the Configuration Register is logic 1 when this command is entered, read cycles on the 1-Wire bus return the state of the PIO pin. The state of the PIO pin can be read for any number of bus cycles. If the $R/\overline{W}$ bit is set to logic 0 when this command is entered, write cycles on the 1-Wire bus are translated into equivalent logic levels on the PIO pin. If data is written to the PIO pin, a Write 0 time slot enables the PIO pin's open-drain output driver after delay t_{D0}, while a Write 1 time slot disables the output driver after t_{D1}. A pullup resistor must be connected between the PIO pin and the VDD pin to achieve a logic 1 value on PIO. A Reset Pulse on the 1-Wire bus terminates the data stream. After a Channel Access write is terminated, the PIO pin latches and drives the last value written until a new Channel Access command is given. See Figure 18 for Channel Access write timing.

CHANNEL ACCESS COMMAND WRITE TIMING Figure 18



FUNCTION COMMANDS Table 11

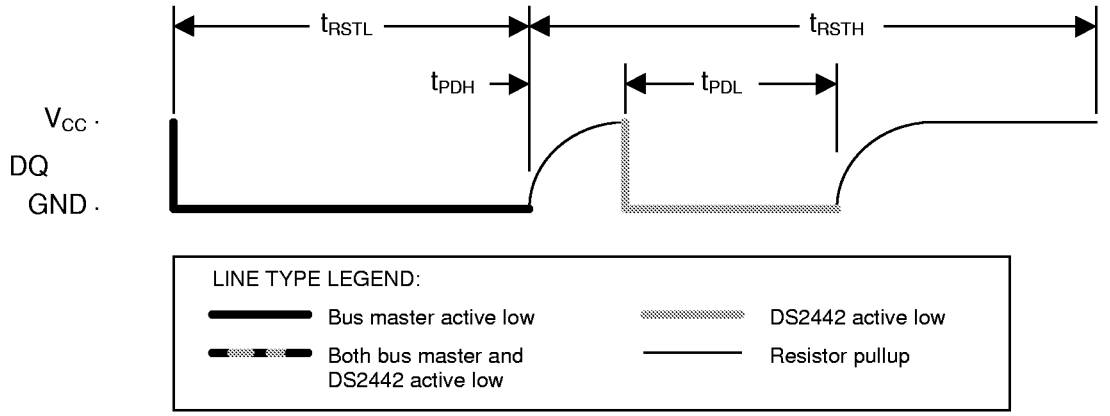
Command	Description	Command Protocol	Bus State After Command Protocol	Bus Data
Lock Register	Disables write access to Page 0	43h	Idle	none
Unlock Register	Enables write access to Page 0	44h	Idle	none
Read Register	Reads data from Page XX (XX = 00 to 03)	BEh, XX	Master R_X	up to 32 bytes of register data
Write Register	Writes data to Page XX (XX = 00, 02, 03)	4Eh, XX	Master Tx	up to 32 bytes of register data
Recall Setup	Recalls Control, Timing, DTW, Mfg. ID and Configuration register defaults	B8h	Idle	none
Channel Access	Controls or senses PIO pin state	F5h	Master R_X ($R/\overline{W}$ =1) Master T_X ($R/\overline{W}$ =0)	unlimited reads or writes

I/0 SIGNALING

The 1-Wire bus requires strict signaling protocols to insure data integrity. The four protocols used by the DS2442 are: the initialization sequence (Reset Pulse followed by Presence Pulse), Write 0, Write 1, and Read Data. All of these types of signaling except the Presence Pulse are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2442 is shown in Figure 19. A Presence Pulse following a Reset Pulse indicates the DS2442 is read to accept a ROM Command. The bus master transmits (T_X) a Reset Pulse for t_{RSTL}. The bus master then releases the line and goes into receive mode (R_X). The 1-Wire bus line is then pulled high by the pullup resistor. After detecting the rising edge on the DQ pin, the DS2442 waits for t_{PDH} and then transmits the Presence Pulse for t_{PDL}.

1-WIRE INITIALIZATION SEQUENCE (RESET PULSE AND PRESENCE PULSE) Figure 19



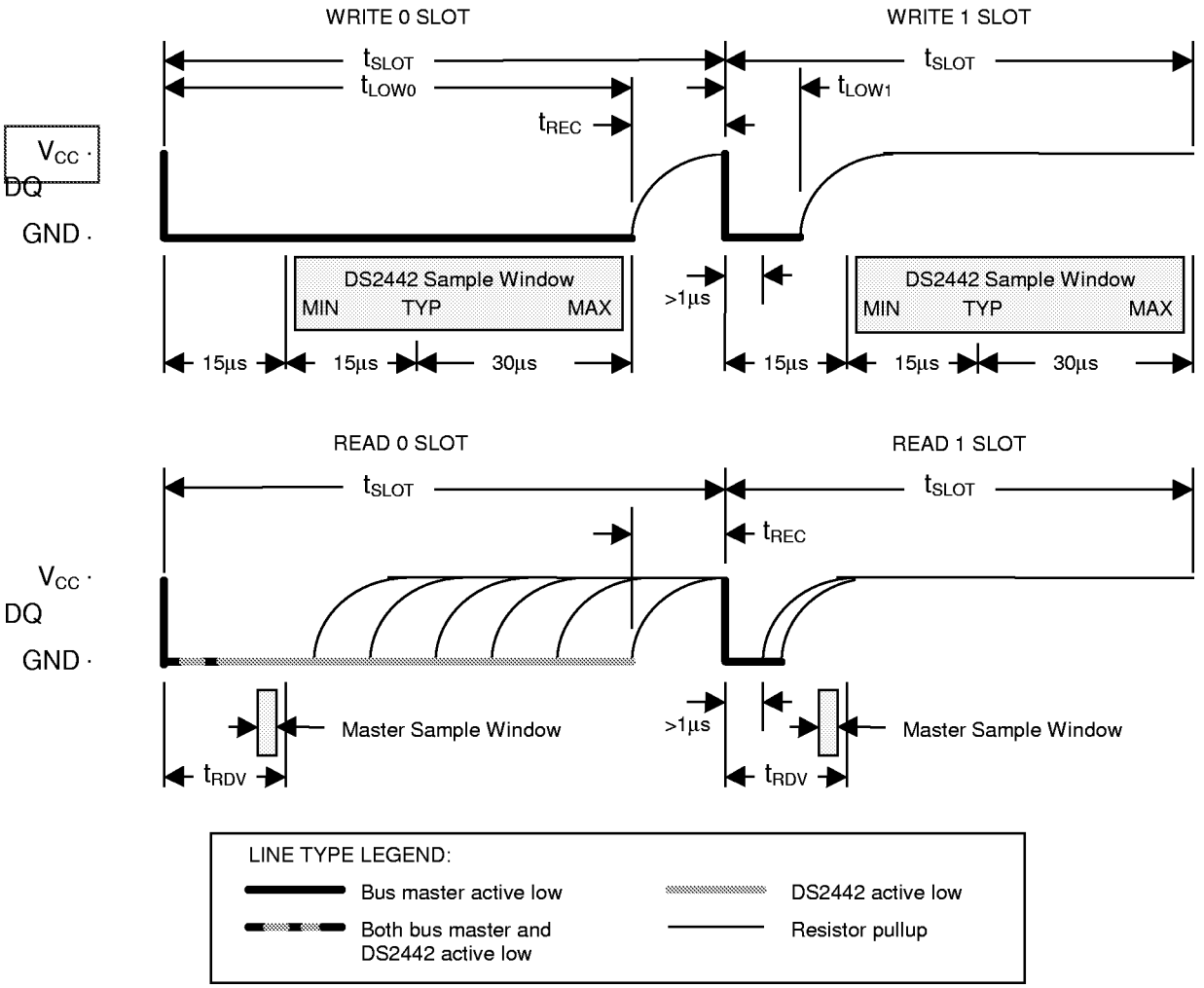
WRITE TIME SLOTS

A write time slot is initiated when the bus master pulls the 1-Wire bus line from a logic high (inactive) level to a logic low level. There are two types of write time slots: Write 1 time slots and Write 0 time slots. All write time slots must be t_{SLOT} (60 to 120 µs) in duration with a 1µs minimum recovery time, t_{REC}, between cycles. The DS2442 samples the 1-Wire bus line between 15 and 60 µs after the line falls. If the line is high when sampled, a Write 1 occurs. If the line is low when sampled, a Write 0 occurs (see Figure 20). For the bus master to generate a Write 1 time slot, the bus line must be pulled to a logic low level and then released, allowing the line to pull up to a logic high level within 15 µs after the start of the write time slot. For the host to generate a Write 0 time slot, the bus line must be pulled to a logic low level and remain low for the duration of the write time slot.

READ TIME SLOTS

A read time slot is initiated when the bus master pulls the 1-Wire bus line from a logic high level to logic low level. The bus master must keep the bus line low for at least 1µs and then release it to allow the DS2442 to present valid data. The bus master can then sample the data t_{RDV} (15 µs) from the start of the read time slot. By the end of the read time slot, the DS2442 releases the bus line and allow it to be pulled high by the external pullup resistor. All read time slots must be t_{SLOT} (60 to 120 µs) in duration with a 1 µs minimum recovery time, t_{REC}, between cycles. See Figure 20 for more information.

1-WIRE WRITE AND READ TIME SLOTS Figure 20



ABSOLUTE MAXIMUM RATINGS*

Voltage on $\overline{CHG}$ pin, Relative to Ground	-0.3V to +18V
Voltage on VDD, $\overline{DCHG}$, DQ, PIO, Relative to Ground	-0.3V to +12V
Voltage on any other pin, Relative to Ground	-0.3V to +7V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C, 2.4V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDD		2.4		10.0	V	1
Voltage Sense	VM		0		5.0	V	1
Data Pin	DQ		-0.3		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; 2.4V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Logic High	V_{IH}	At DQ, PIO	2.0			V	1
Input Logic Low	V_{IL}	At DQ, PIO	-0.3		0.5	V	1
Shutdown Current	I_{DD1}	DQ=0V, Low Power Mode		1.0	1.5	µA	2, 3
Active Current	I_{DD2}	DQ=5.0V, normal operation		70	100	µA	2, 4
Output Current	I_{PIO}	V_{OUT}=0.4V	-4			mA	
	I_{DQ}	V_{DQ}=0.4V	-4			mA	
	$\overline{CHG}$, $\overline{DCHG}$	Sink	-1			mA	5
		Source			0.3		
Input Resistance	R_I	DQ		500		kΩ	6, 10
Power-On Reset Voltage	V_{POR}			1.8V			1
Discharge Warning Voltage	V_{DW}		2.65	2.70	2.75	V	1

ELECTRICAL CHARACTERISTICS: PROTECTION CIRCUITRY

(-40°C to +85°C; 2.4V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Overvoltage Detect	V_{OV}		4.300	4.350	4.400	V	1, 9
Charge Enable	V_{CE}		3.9	4.0	4.1	V	1, 9
Undervoltage Detect	V_{UV}		2.45	2.5	2.55	V	1, 9
Overcurrent Detect	V_{OC}		103	105	107	mV	1
Short Circuit Detect	V_{SC}		350	450	550	mV	1
Overtemperature Trip Point	T_{TRIP}		82	85	88	°C	
Overtemperature Hysteresis	T_{HYS}			4		°C	
Overvoltage Delay	t_{OVD}	OVD=00(min)	384	512	640	ms	9
		OVD=11(max)	3072	4096	5120	ms	
Undervoltage Delay	t_{UVD}	UVD=00(min)	24	32	40	ms	9
		UVD=11(max)	192	256	320	ms	
Overcurrent Delay	t_{OCD}	OCD=00(min)	1.5	2	2.5	ms	9
		OCD=11(max)	12	16	20	ms	
Short Circuit Delay	t_{SCD}			30	100	µs	
Release Delay	t_{REL}	REL=00(min)	384	512	640	ms	9
		REL=11(max)	3072	4096	5120	ms	

ELECTRICAL CHARACTERISTICS: CURRENT ACCUMULATOR

(-40°C to +85°C; 2.4V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Timer Accuracy	t_{ERR}			±1	±3	%	
		At 25°C, VDD=7.2V		±0.5	±1	%	
Conversion Error	I_{ERR}	At I_{SENS}		±1		%	8

ELECTRICAL CHARACTERISTICS: VOLTAGE CONVERTER

(-40°C to +85°C; 2.4V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Sampling Period	t_{SH}	For 32 samples		6.9		ms	
Conversion Time	t_{VCONV}	Single conversion		215		µs	
Conversion Error	V_{ERR}	For VM or VDD - VM		±10	±50	mV	
Conversion Cycle	t_{CYCL}	Cell Voltages and Temp			14.4	ms	

ELECTRICAL CHARACTERISTICS: THERMOMETER

(-40°C to +85°C; 2.4V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Conversion Time	t_{TCONV}			215		µs	
Thermometer Error	T_{ERR}	at 0°C		±2	±3	°C	7

ELECTRICAL CHARACTERISTICS: BLEEDING CIRCUIT

(-40°C to +85°C; 2.4V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Cell Balancing Current	I_{BAL}	VDD to VM or VM to GND	30	50	100	µA	9

ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE

(-40°C to +85°C; 2.4V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}		60		120	µs	
Recovery Time	t_{REC}		1			µs	
Write 0 Low Time	t_{LOW0}		60		120	µs	
Write 1 Low Time	t_{LOW1}		1		15	µs	
Read Data Valid	t_{RDV}				15	µs	
Reset Time High	t_{RSTH}		480			µs	
Reset Time Low	t_{RSTL}		480		960	µs	
Presence Detect High	t_{PDH}		15		60	µs	
Presence Detect Low	t_{PDL}		60		240	µs	
DQ Capacitance	C_{DQ}				25	pF	

ELECTRICAL CHARACTERISTICS: PROGRAMMABLE I/O

(-40°C to +85°C; 2.4V ≤ V_{DD} ≤ 10.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Logic 1 prop. delay	t_{d1}		15		60	µs	
Logic 0 prop. delay	t_{d0}				300	ns	

NOTES

1. All voltages are referenced to GND.
2. Shutdown and active currents specified for the range 0°C to 70°C.
3. I_{DD1} specified with each cell voltage at V_{UV}.
4. I_{DD2} specified with V_{DD} = 10.0 V.
5. $\overline{CHG}$ is open drain and does not source current.
6. Input load is to GND.
7. Maximum error values are guaranteed by design over the full temperature range.
8. Current measurement accuracy is ±2 LSB or ±1%, whichever is greater.
9. Contact the factory for different voltage trip points and default delay periods.
10. This input resistance is not present when the DS2442 is in Refresh Mode and the DQ pin is serving as a power supply input.