Preliminary Information

NJU25301

Dolby® Digital (AC-3) Decoder

Description

The NJU25301 is a complete low-cost 5.1 channel AC-3® decoder intended for use in Dolby Digital® consumer and multimedia applications. The NJU25301 contains on-chip firmware for decoding and processing Dolby Digital (AC-3) bitstreams and linear PCM data. It also includes a Dolby Pro Logic® decoder for decoding matrix surround encoded PCM data or 2 channel Dolby Surround® encoded digital data. It is also the industry's first Dolby certified, Class A Dolby Digital decoder IC to include 8 separate Bass Management Configurations. All features are implemented in on-chip memory (program ROM) eliminating the need for external memory devices. The decoder is controlled via a serial host interface which includes a choice of industry-standard I²C-Bus® or SPI bus communication protocols. Standard digital audio data formats are supported, including I²S, MSB-first right-justified, and MSB-first left-justified.

NJU25301 utilizes a 24-bit DSP architecture developed by NJRC . The highly accurate processing of the NJU25301 makes it suitable for applications such as A/V Receivers, DVD players, Digital Multimedia Speakers, and HDTV set-top decoders.

Features

- **Complete Class A Dolby Digital Decoder**
  - Supports 16-, 18-, 20-, or 24-bit data words
  - Audio sample rates: 32 kHz, 44.1 kHz, 48 kHz
  - Decodes up to 5.1 channel, 448 kbps Dolby Digital bitstream
- **Eight Dolby Certified Bass Management Modes**
  - 5 Dolby Configurations for Processing Dolby Digital
  - 3 Dolby Configurations for Processing Dolby Pro Logic
- **Automatic Bitstream Detection**
- **Small 80-pin PQFP package**
- **On-chip features:**
  - AC-3 Decoding
  - Dolby Pro Logic Decoding
  - Surround and Center Channel Delays
  - Pink Noise Generator
  - Automatic Bass Management Mode Adjustment (upon detection of change from 5.1 (AC-3) to Pro Logic encoded material, or vice versa)

Figure 1 NJU25301 Block Diagram

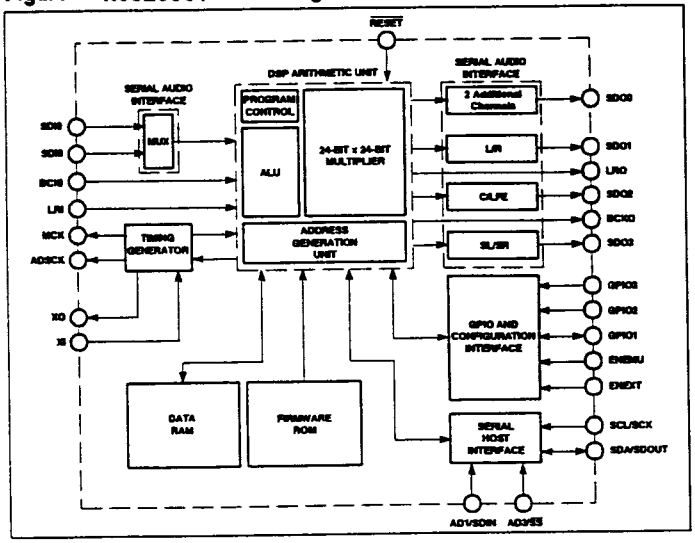

Figure 2 Typical Room Setup

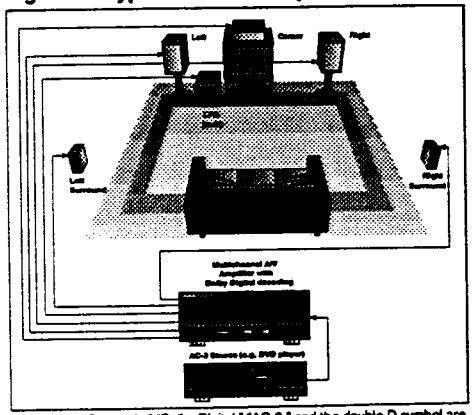

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Figure 3 NJU25301 Pin Configuration

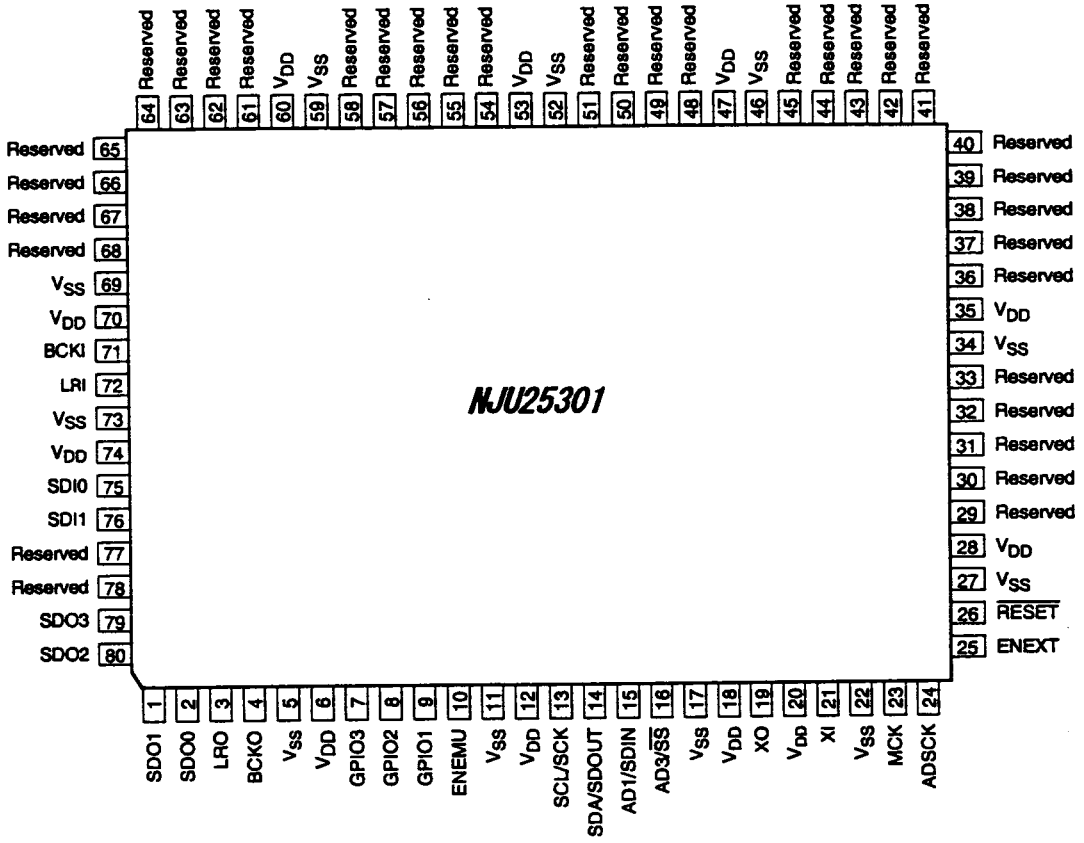


Figure 4 Typical A/V Receiver Configuration with 5.1 Channels

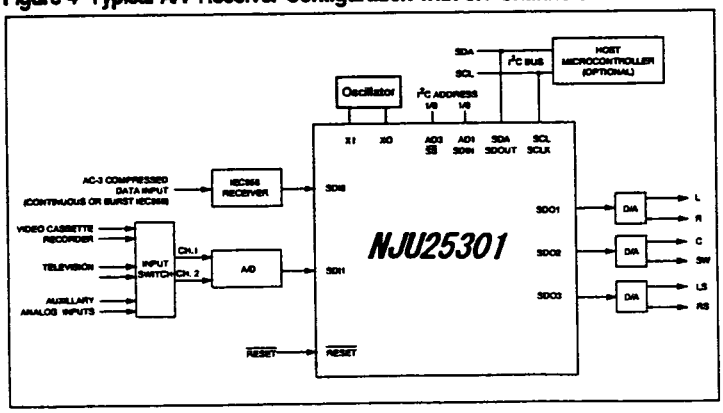


Figure 5 PQFP-80 Package

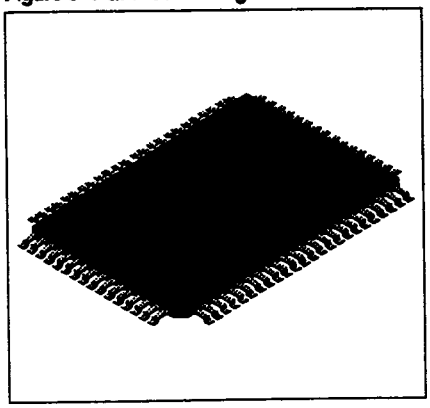


Table 1 Pin Description

No.	Symbol	I/O	Function	No.	Symbol	I/O	Function
1	SDO1	O	Digital audio serial data output	41	NC		No connect
2	SDO0	O	Digital audio serial data output	42	NC		No connect
3	LRO	O	Left/right word clock output	43	NC		No connect
4	BCKO	O	Digital audio serial clock output	44	NC		No connect
5	VSS	I	Ground	45	NC		No connect
6	VDD	I	Power supply terminal: +5V	46	VSS	I	Ground
7	GPIO3[1]	I	Host type select. SPI bus = L, I²C-bus = H	47	VDD	I	Power supply terminal: +5V
8	GPIO2[1]	I	AC-3 Downmix Mode default power-up setting. 5.1 ch = L, 2.1 ch = H	48	NC		No connect
9	GPIO1	I/O	General purpose interface	49	NC		No connect
10	ENEMU		Test pin (tie low for normal operation)	50	NC	I	No connect
11	VSS	I	Ground	51	NC		No connect
12	VDD	I	Power supply terminal: +5V	52	VSS		Ground
13	SCL/SCK	I	I²C-bus host serial clock/SPI bus host serial clock	53	VDD		Power supply terminal: +5V
14	SDA/SDOUT	I/O	I²C-bus host serial data/SPI bus host serial data output	54	NC		No connect
15	AD1/SDIN	I	I²C-bus host serial address/SPI bus host serial data input	55	NC		No connect
16	AD3/$\overline{SS}$	I	I²C-bus host serial address/SPI bus host slave select	56	NC		No connect
17	VSS	I	Ground	57	NC		No connect
18	VDD	I	Power supply terminal: +5V	58	NC		No connect
19	XO	O	Crystal	59	VSS	I	Ground
20	VDD	I	Power supply terminal: +5V	60	VDD	I	Power supply terminal: +5V
21	XI	I	Crystal/External clock input	61	NC		No connect
22	VSS	I	Ground	62	NC		No connect
23	MCK	O	256Fs master clock for A/D, D/A converters	63	NC		No connect
24	ADSCK	O	32Fs/64Fs option serial clock for A/D, D/A converters and microcontrollers (default 32Fs)	64	NC		No connect
25	ENEXT	I	Test pin (tie low for normal operation)	65	NC		No connect
26	RESET	I	Reset	66	NC		No connect
27	VSS	I	Ground	67	NC		No connect
28	VDD	I	Power supply terminal: +5V	68	NC		No connect
29	NC		No connect	69	VSS	I	Ground
30	NC		No connect	70	VDD	I	Power supply terminal: +5V
31	NC		No connect	71	BCKI	I	Digital audio serial clock input
32	NC		No connect	72	LRI	I	Left/right frame clock input
33	NC		No connect	73	VSS	I	Ground
34	VSS	I	Ground	74	VDD	I	Power supply terminal: +5V
35	VDD	I	Power supply terminal: +5V	75	SDI0	I	Digital audio serial data input
36	NC		No connect	76	SDI1	I	Digital audio serial data input
37	NC		No connect	77	NC		No connect
38	NC		No connect	78	NC		No connect
39	NC		No connect	79	SDO3	O	Digital audio serial data output
40	NC		No connect	80	SDO2	O	Digital audio serial data output

1. Only sensed upon power-up.

Functional Description

The NJU25301 is a high performance dedicated digital signal processor designed to decode Dolby Digital, and matrix surround encoded (Dolby Surround) digital audio bitstreams. All decoding algorithms are contained in preprogrammed firmware, thus reducing time-to-market for the user. The DSP core has been optimized for audio processing which reduces cost compared to general-purpose DSPs.

The NJU25301 automatically detects the type of input data, allowing it to switch between compressed Dolby Digital or linear PCM bitstreams. No external commands are required to recognize and decode incoming bitstreams. The Dolby Digital bitstream contains decoding information which indicate how the audio is processed. Through a simple and flexible command protocol, the user can manually override certain bitstream elements (such as compression modes) to obtain desired audio playback characteristics.

The NJU25301 includes two stereo digital audio inputs [SDI0:1] and four stereo digital audio outputs [SDO0:3], however only three of these stereo digital audio outputs [SDO1:3] are used for this Dolby Digital solution. Dolby digital data, conventionally formatted as a stereo digital audio signal, can be applied to the SDI0 input while an optional stereo A/D converter can be connected to the second input, SDI1. The digital inputs and outputs can be configured to 16, 18, 20 or 24 bits resolution using any of I^2S, left-justified or right-justified formats allowing connection to virtually any type of audio A/D and D/A converters.

The NJU25301 can also accept inputs from an IEC958 (S/PDIF) receiver. IEC958 is typically used to transfer Dolby Digital (AC-3) data between consumer audio equipment. The NJU25301 transfers serial audio clocking signals when receiving digital audio data from an external source such as an IEC958 receiver. This default (start-up) mode of operation is referred to as SLAVE mode as the external audio source establishes the audio clock rate. The NJU25301 can also be programmed to generate serial audio clocking signals (MASTER mode). MASTER mode can be used to receive analog audio inputs from an A/D converter when an external digital source is not chosen or is not available.

The NJU25301 serial host interface can be enabled to operate with either I^2C-bus format or SPI bus format. The NJU25301 has a command-based instruction set simplifying microcontroller programming. No knowledge of DSP coding is required to use the NJU25301 . Commands include AC-3 decoder parameters, compression modes, Pro Logic variables, channel delays, and downmix modes. For very simple applications, NJU25301 may be operated without a microcontroller as a 5.1 channel or 2.1 channel (downmixed) AC-3 decoder. The bitstream auto-detect feature allows proper decoding of either AC-3 or Linear PCM audio streams without user input.

The DSP core consists of a 24-bit processor with a 48-bit accumulator. All required memory elements, including data RAM, program ROM, and delay RAM are included on chip. The core's 24-bit processing allows for improved accuracy compared to 16-bit or 20-bit cores, delivering superior signal-to-noise performance for complex and low-level signals.

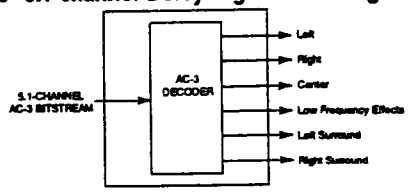
The NJU25301 is ideally suited for multi-channel home theater applications, where high performance Dolby Digital decoding must be performed at low cost. With an optional A/D converter connected to the second input, the NJU25301 can perform Pro Logic processing of analog source material.

The bass management engine alleviates the need for a system designer to handle bass management in the analog domain. The NJU25301 offers 8 different bass management modes, all of which have been approved by Dolby Laboratories. This method of bass management saves both time and money. It simplifies the system design, saves board real estate and shortens the approval period taken by Dolby Laboratories upon review of the "pre-production prototype" in a two fold method: Since bass management is performed in the digital domain, it will result in a much lower noise floor from the final product and since this method of bass management is already approved by Dolby, there is a reduced need to review post AC-3 decoding schematics.

Decoding Configurations

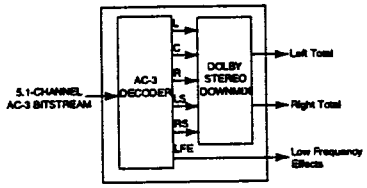
The NJU25301 as different decoding configurations that take into consideration different speaker arrangements. This is helpful in handling situations where the user may not desire a full 5.1 channel output with all the corresponding speakers.

Figure 6 5.1-channel Dolby Digital Decoding



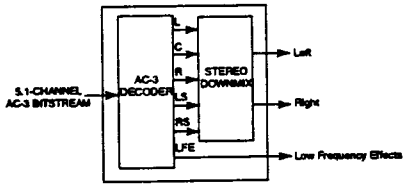
The default configuration for NJU25301 is 5.1-channel Dolby Digital decoding. No external components, memory elements, or microprocessor are required for this configuration. This is configuration is displayed above in Figure 6.

Figure 7 5.1-channel Dolby Digital with Dolby Surround (L_t, R_t) Downmix



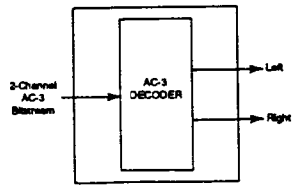
5.1-channel AC-3 bitstreams may be downmixed to two channels which contain Dolby Surround encoding. These outputs can be used with Dolby Pro Logic receivers. This mode can also be selected without a microcontroller.

Figure 8 5.1-channel Dolby Digital with Stereo (L_O, R_O) Downmix



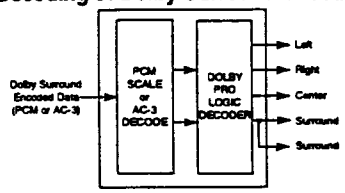
5.1-channel bitstreams can be decoded and downmixed into two channels for normal stereo output. The Low Frequency Effects channel is available as an optional subwoofer output.

Figure 9 2-channel encoded bitstream decoding



NJU25301 decodes Dolby Digital sources containing from 1 to 5.1 channels. Here, the NJU25301 decodes a 2-ch AC-3 bitstream.

Figure 10 Decoding of Dolby Surround Encoded Material



PCM data which has Dolby Surround (Pro Logic) encoding can be decoded and processed by NJU25301. Surround channels are monaural by definition.

Audio Processing Description

The NJU25301 processes audio signals received and returned by way of the Serial Audio Interface. Details of the audio processing functions are shown in Figure 12. Audio processing functions can be programmed by commands sent via the Serial Host Interface. Most commands as described in the Command Table change parameters of the audio processing functions. Other commands configure the Serial Audio Interface and read or write data at the General Purpose Input/Output (GPIO) Interface.

Figure 11 NJU25301 Functional Drawing

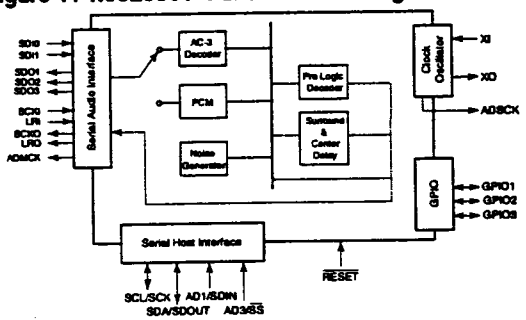
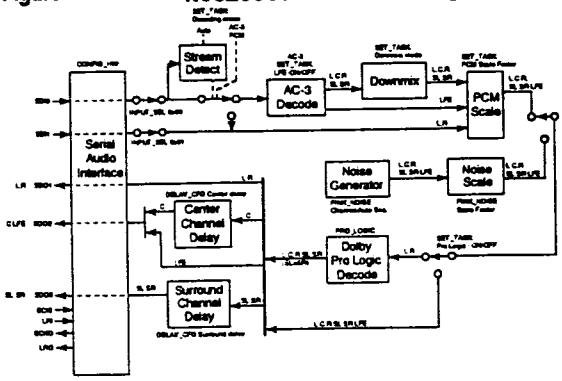


Figure 12 Detail of NJU25301 Audio Processing Functions



Compression Modes Overview

Custom Mode 0 (Analog) – Summary of features:

- Dialog normalization (*Dialnorm*) always off
- -11dB gain shift imposed when downmixing, in order to prevent peak level overload
- *Dynrng* compression variable used
- Low-level boost compression (Dynsclh) scaling allowed
- High-level cut compression (Dynscll) scaling allowed

Custom Mode 0 (Analog) allows the degree of compression applied to be scaled down or defeated under any condition. The only restriction is that when downmixing is active, an -11dB gain shift is imposed to ensure no signal overload will occur. End products using the Custom Mode 0 (Analog) will require +11dB of selectable gain correction after the external D/A converter. Under these conditions, the final audio outputs may exhibit a higher noise floor. In addition, dialog normalization must be accomplished in analog circuitry external to the NJU25301 decoder IC. This is usually done in the master volume control, under the control of the dialnorm variable in the bitstream.

Custom Mode 1 (Digital) – Summary of features:

- Dialog normalization (*Dialnorm*) always off
- -11dB gain shift imposed when downmixing, in order to prevent peak level overload
- *Dynrng* compression variable used
- Low-level boost compression (Dynsclh) scaling allowed
- High-level cut compression (Dynscll) scaling allowed

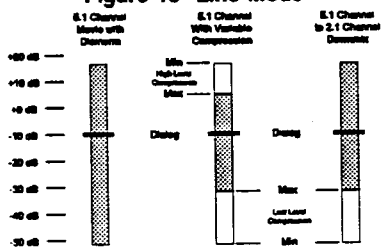
Custom Mode 1 (Digital) allows the degree of compression applied to be scaled down or defeated under any condition. The only restriction is that when downmixing is active, an -11dB gain shift is imposed to ensure no signal overload will occur. End products using the Custom Mode 1 (Digital) will require +11dB of selectable gain correction after the external D/A converter. Under these conditions, the final audio outputs may exhibit a higher noise floor. However, unlike Custom Mode 0 (Analog), dialog normalization is handled internally.

Line Mode – Summary of features:

- Dialog normalization (*Dialnorm*) always on
- Dialog is reproduced at a constant level
- *Dynrng* compression variable is used
- Low-level boost compression scaling (Dynsclh) is allowed
- High-level cut compression scaling (Dynscll) is allowed, provided no downmix is requested (downmix mode set to 111b)

One of the conditions of the Line Mode is the full high-level compression is applied whenever downmixing is active, so its effect cannot be reduced. Below, Figure 13 depicts the signal relationships, under different conditions when the device is in Line Mode. Note that the average program loudness remains constant, regardless of the downmix or compression settings.

Figure 13 Line Mode

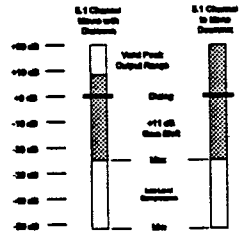


RF Mode – Summary of features:

- Dialog normalization is always on
- Dialog reproduced at a constant level (-20 dB FS)
- *Dynrng* and *compr* compression variables used
- Compression scaling not allowed
- +11dB gain shift imposed

This mode is optimized for products generating a downmixed signal for subsequent "channel 3" RF demodulation. The overall program level is raised 11dB, while the peaks are limited to prevent signal overload in the external D/A converters. By limiting headroom to a maximum of 20 dB above average dialog level, overmodulation of television receivers is prevented while providing an average RF modulation level that compares well with quality television broadcasts and premium movie channels. Below, Figure 14 depicts the signal relationships, under different conditions when the device is in RF Mode. Note that the average program loudness remains constant, regardless of the downmix setting. Compression remains fully on at all times.

Figure 14 RF Mode



Bass Management Overview

The traditional AC-3 speaker configuration consists of separate speakers for Front Left and Right, Center, Surround Left and Right, and Subwoofer. These are usually referred to as L, R, C, SL, SR, SW respectively. This configuration is commonly referred to as "5.1"channels of output, rather than "six", since the Subwoofer generally has a much lower bandwidth than the other five speakers. It is also assumed that the other five speakers are "full-range" speakers with good response below 100 Hz. Frequencies much lower than that are difficult for the ear to determine point-source direction, and are therefore usually placed on the "Subwoofer" (SW) channel.

In typical AC-3 systems, the "Low Frequency Effects" (LFE) goes directly to the Subwoofer. But for some systems, this may not be the optimal configuration. Often one or more of the five main speakers is capable of truly low frequency response, reaching down into the lowest octave of audible range. This is most often the case in systems which were upgraded from a high-quality stereo (two speaker) system. Usually in such arrangements, the Left and Right Stereo speakers become the Front Left and Right speakers in a multichannel system. In such cases, it may not be necessary to have a Subwoofer, or it may be desirable to transfer the lower frequencies to the higher-quality speakers. This function is called "Bass Management." Additionally, since many home systems were previously Pro Logic enabled, it is entirely plausible that not all of the speakers (especially those previously dedicated for the Pro Logic surround information) were designed to have a full-range frequency response. From this consideration, one can easily see the value that Bass Management adds to a Dolby Digital system.

Mode 0 (Bass Management Off)

Mode 0 is the default mode, and Bass Management is off. All the Gain Block coefficients (a0 ~ a5) = 1, as does (c3). This results in each of the audio signals passing through unchanged. This mode is recommended for systems that have full-range speakers on each of the primary five channels, plus a Subwoofer for LFE information.

Figure 15 Bass Management Configuration Mode 0: Recommended Room Setup

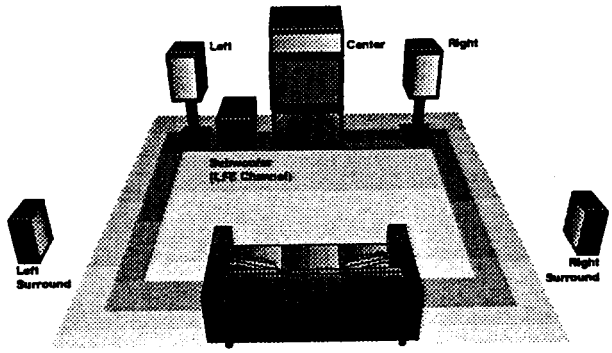
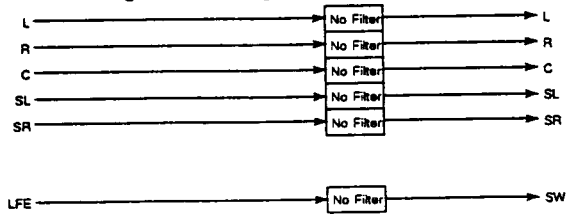


Figure 16 Bass Management Configuration Mode 0: Signal Block Diagram



Bass Management Mode 1 (AC-3 Mode)

Mode 1 adds all of the five main channels to the output of the Low Frequency Effects (LFE) channel. This summation is then filtered to allow only the low frequencies to pass, and the gain is increased by 6dB. Other than using a High-Pass filter, no other processing is done on the main five channels. This mode is recommended for systems that have limited low-frequency response on the primary five channels, but have a Subwoofer.

Figure 17 Bass Management Configuration Mode 1: Recommended Room Setup

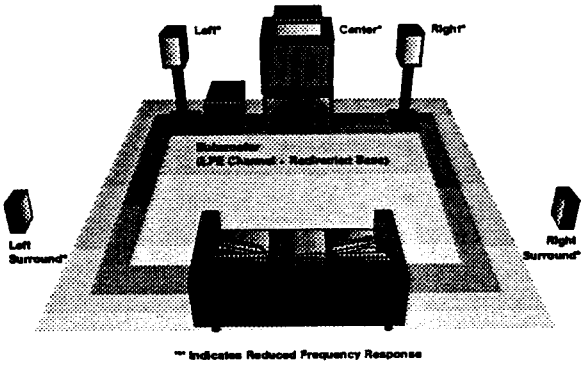


Figure 18 Bass Management Configuration Mode 1: Signal Block Diagram[1]

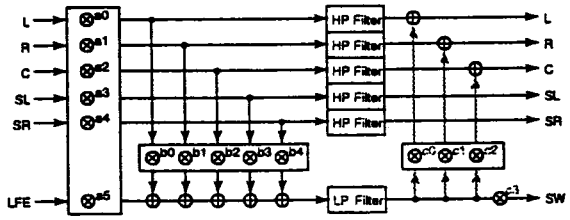


Table 2 Default Coefficient Set for Bass Management Configuration Mode 1[1]

Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value
a0	7FFF	1	b0	16C2	0.177	c0	xxxx	x
a1	7FFF	1	b1	16C2	0.177	c1	xxxx	x
a2	7FFF	1	b2	16C2	0.177	c2	xxxx	x
a3	7FFF	1	b3	16C2	0.177	c3	xxxx	x
a4	7FFF	1	b4	16C2	0.177			
a5	47FA	0.562						

1. "xxxx" indicate that the setting of these coefficients is not applicable.

1. Arrows and coefficients in gray indicate that there is no fundamental connection or have been grayed-out for illustrative purposes.

Bass Management Mode 2 (AC-3 Mode)

Mode 2 uses the two Front output channels to augment the bass response of the Subwoofer output by adding the Center and Surround channels to the LFE channel, low-pass filtering it, and adding the filtered response to the two Front channels. This configuration could be used for five-speaker systems where the two front speakers are of extended bass range.

Figure 19 Bass Management Configuration Mode 2: Recommended Room Setup

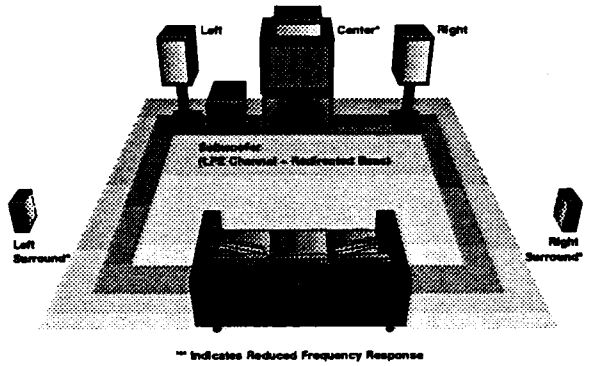


Figure 20 Bass Management Configuration Mode 2: Signal Block Diagram[1]

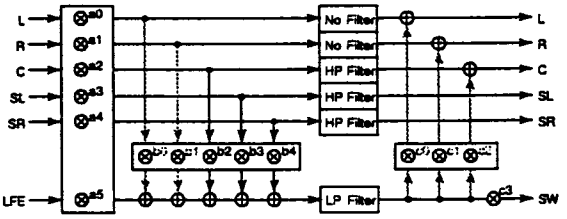


Table 3 Default Coefficient Set for Bass Management Configuration Mode 2[1]

Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value
a0	7FFF	1	b0	0000	0	c0	0000	0
a1	7FFF	1	b1	0000	0	c1	0000	0
a2	7FFF	1	b2	16C2	0.177	c2	0000	0
a3	7FFF	1	b3	16C2	0.177	c3	7FFF	1
a4	7FFF	1	b4	16C2	0.177			
a5	47FA	0.562						

1. "xxxx" indicate that the setting of these coefficients is not applicable.

1. Arrows and coefficients in gray indicate that there is no fundamental connection or have been grayed-out for illustrative purposes.

Bass Management Mode 3 (AC-3 Mode)

Mode 3 uses a different connection diagram than the previous three modes. In this configuration, the Center channel is high-pass filtered and that output goes to the Center speaker. It is also low-pass filtered, and that output goes to the two Front outputs. This configuration could be used for five-speaker systems where the two front speakers are of extended bass range, and the Center speaker is of limited bandwidth.

Figure 21 Bass Management Configuration Mode 3: Recommended Room Setup

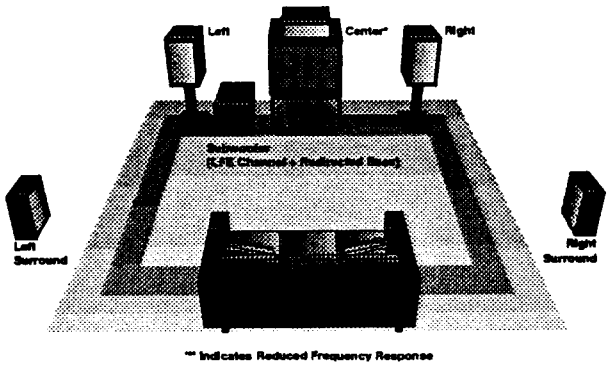


Figure 22 Bass Management Configuration Mode 3: Signal Block Diagram[1]

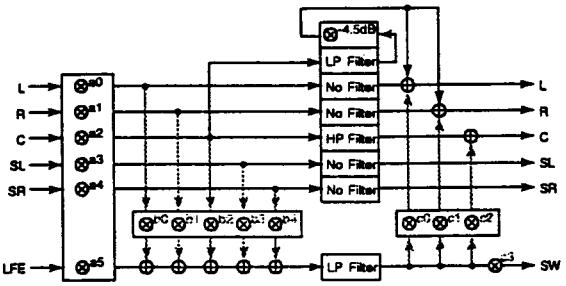


Table 4 Default Coefficient Set for Bass Management Configuration Mode 3[1]

Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value
a0	50C2	0.631	b0	xxxx	x	c0	xxxx	x
a1	50C2	0.631	b1	xxxx	x	c1	xxxx	x
a2	50C2	0.631	b2	xxxx	x	c2	xxxx	x
a3	50C2	0.631	b3	xxxx	x	c3	xxxx	x
a4	50C2	0.631	b4	xxxx	x			
a5	50C2	0.631						

1. "xxxx" indicate that the setting of these coefficients is not applicable.

1. Arrows and coefficients in gray indicate that there is no fundamental connection or have been grayed-out for illustrative purposes.

Bass Management Mode 4 (AC-3 Mode)

Mode 4 uses a different connection diagram than Modes 1 - 3. In this configuration, the Center channel is high-pass filtered and that output goes to the Center output. It is also low-pass filtered, and that is added to the two Front outputs. In addition, the LFE output is summed with the two Front speakers as well as the Surround channels. This configuration could be used for five-speaker systems where the Front and Surround speaker pairs are of extended bass range.

Figure 23 Bass Management Configuration Mode 4: Recommended Room Setup

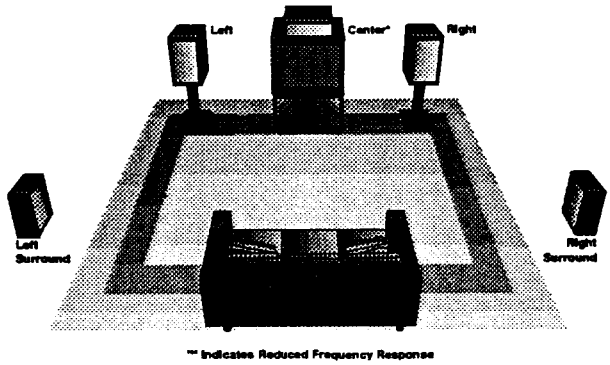


Figure 24 Bass Management Configuration Mode 4: Signal Block Diagram[1]

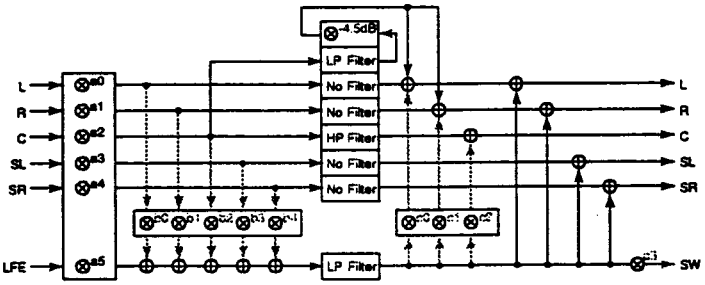


Table 5 Default Coefficient Set for Bass Management Configuration Mode 4[1]

Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value
a0	32FA	0.398	b0	xxxx	x	c0	xxxx	x
a1	32FA	0.398	b1	xxxx	x	c1	xxxx	x
a2	32FA	0.398	b2	xxxx	x	c2	xxxx	x
a3	32FA	0.398	b3	xxxx	x	c3	xxxx	x
a4	32FA	0.398	b4	xxxx	x			
a5	32FA	0.398						

1. "xxxx" indicate that the setting of these coefficients is not applicable.

1. Arrows and coefficients in gray indicate that there is no fundamental connection or have been grayed-out for illustrative purposes.

Bass Management Mode 5 (Pro Logic Mode)

This is the Pro Logic adaptation of Mode 1. However, there is only one Surround channel produced, and no Low Frequency Effects output. Mode 5 synthesizes all 5.1 channels with filtering and summations. Note that while the Surround channel is high-pass filtered, no contribution is made to the Subwoofer channel. This is due to the phasing of the signals and the reduced low-end frequency response that this channel inherently has. It is a configuration similar to NJRC current Dolby Pro Logic devices.

Figure 25 Bass Management Configuration Mode 5: Recommended Room Setup

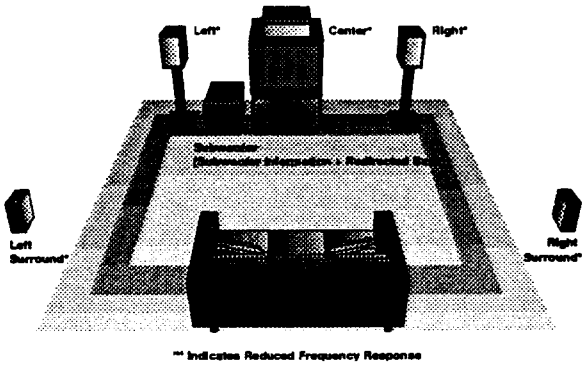


Figure 26 Bass Management Configuration Mode 5: Signal Block Diagram[1]

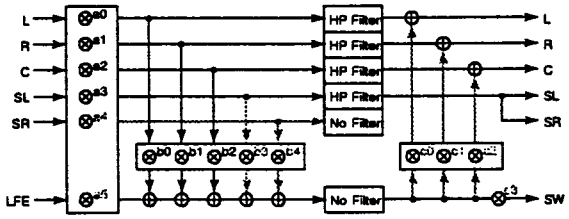


Table 6 Default Coefficient Set for Bass Management Configuration Mode 5[1]

Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value
a0	7FFF	1	b0	16C2	0.177	c0	xxxx	x
a1	7FFF	1	b1	16C2	0.177	c1	xxxx	x
a2	7FFF	1	b2	16C2	0.177	c2	xxxx	x
a3	7FFF	1	b3	0000	0	c3	xxxx	x
a4	0000	0	b4	0000	0			
a5	0000	0						

1. "xxxx" indicate that the setting of these coefficients is not applicable.

1. Arrows and coefficients in gray indicate that there is no fundamental connection or have been grayed-out for illustrative purposes.

Bass Management Mode 7 (Pro Logic Mode)

This is the Pro Logic adaptation of Mode 2. However, there is only one Surround channel produced, and no Low Frequency Effects output. While similar to Mode 5 or 6, this time there is Subwoofer channel contribution from the Center Channel. Mode 7 synthesizes all 5.1 channels with filtering and summations. Note that while the Surround channel is high-pass filtered, no contribution is made to the Subwoofer channel. This is a configuration for systems with a Subwoofer, and extended bass on all but the Center channel.

Figure 27 Bass Management Configuration Mode 7: Recommended Room Setup

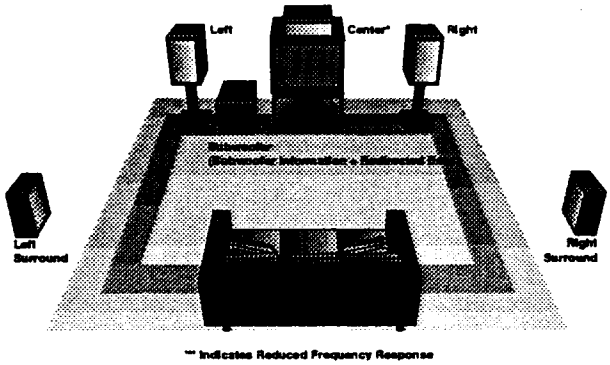


Figure 28 Bass Management Configuration Mode 7: Signal Block Diagram[1]

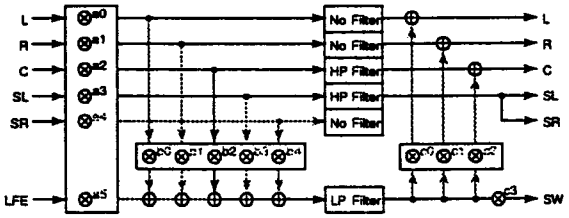


Table 7 Default Coefficient Set for Bass Management Configuration Mode 7[1]

Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value
a0	7FFF	1	b0	0000	0	c0	0000	0
a1	7FFF	1	b1	0000	0	c1	0000	0
a2	7FFF	1	b2	16C2	0.177	c2	0000	0
a3	7FFF	1	b3	0000	0	c3	7FFF	1
a4	0000	0	b4	0000	0			
a5	0000	0						

1. "xxxx" indicate that the setting of these coefficients is not applicable.

1. Arrows and coefficients in grey indicate that there is no fundamental connection or have been grey-out for illustrative purposes.

Bass Management Mode 8 (Pro Logic Mode)

This is the Pro Logic adaptation of Mode 10. However, there is only one Surround channel produced, and no Low Frequency Effects output. While similar to Mode 7, this time the low frequency component is summed back into the Front outputs. Mode 8 does not produce a Subwoofer output. Note that while the Surround channel is high-pass filtered, no contribution is made to the Subwoofer channel. It is for systems with extended bass on the front speakers, and no Subwoofer.

Figure 29 Bass Management Configuration Mode 8: Recommended Room Setup

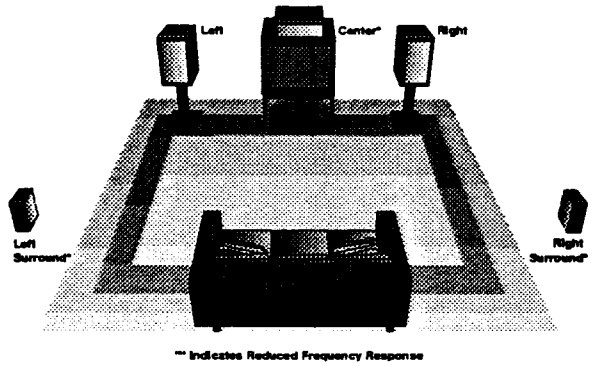


Figure 30 Bass Management Configuration Mode 8: Signal Block Diagram[1]

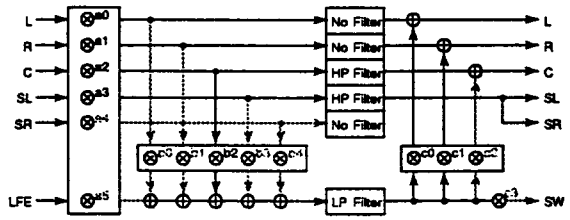


Table 8 Default Coefficient Set for Bass Management Configuration Mode 8[1]

Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value
a0	7FFF	1	b0	0000	0	c0	7FFF	1
a1	7FFF	1	b1	0000	0	c1	7FFF	1
a2	7FFF	1	b2	4C3F	0.595	c2	0000	0
a3	7FFF	1	b3	0000	0	c3	0000	0
a4	0000	0	b4	0000	0			
a5	0000	0						

1. "xxxx" indicate that the setting of these coefficients is not applicable.

1. Arrows and coefficients in gray indicate that there is no fundamental connection or have been grayed-out for illustrative purposes.

Bass Management Mode 10 (AC-3 Mode)

This is an AC- 3 configuration. As such, there is a Low Frequency Effects output. While similar to Mode 2, this time the low frequency component of the Center and Surround channels is summed back into the Front outputs. Mode 10 keeps the LFE separate, going directly to the Subwoofer output. This configuration is used where the Front speakers are of extended range.

Figure 31 Bass Management Configuration Mode 10: Recommended Room Setup

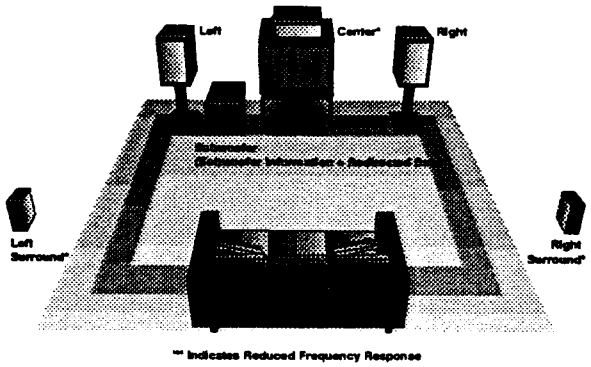


Figure 32 Bass Management Configuration Mode 10: Signal Block Diagram[1]

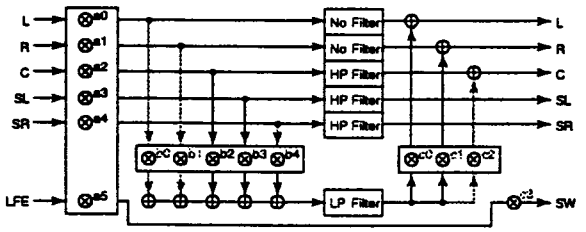


Table 9 Default Coefficient Set for Bass Management Configuration Mode 10[1]

Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value	Coefficient	Hex Value	Decimal Value
a0	7FFF	1	b0	0000	0	c0	xxxx	x
a1	7FFF	1	b1	0000	0	c1	xxxx	x
a2	7FFF	1	b2	4C3E	0.595	c2	xxxx	x
a3	7FFF	1	b3	4C3E	0.595	c3	xxxx	x
a4	7FFF	1	b4	4C3E	0.595			
a5	7FFF	1						

1. "xxxx" indicate that the setting of these coefficients is not applicable.

1. Arrows and coefficients in gray indicate that there is no fundamental connection or have been grayed-out for illustrative purposes.

NJU25301 Commands

NJU25301 allows for user configuration of the decoder with microcontroller commands entered via the Host I/O interface (I^2C-bus or SPI bus). The following table summarizes the available user commands.

Table 10 NJU25301 Command Table

No.	Command	Mnemonic	Description
1.	Set Task	SET_TASK_CMD	Sets primary decoding mode: AC-3, Dolby Pro Logic, or Linear PCM
2.	AC-3 Decode	AC3_CMD	Sets AC-3 compression and dialog normalization modes
3.	Pro Logic Decode	PRO_LOGIC_CMD	Sets the variables for Pro Logic decoding
4.	Bass Management Configuration	BASS_MGMT_CFG_CMD	Sets Bass Management Configuration Mode
5.	Delay Configuration	DELAY_CFG_CMD	Sets amount of delay in Center channel and Surround channels
6.	Pink Noise Generator	PINK_NOISE_CMD	Sets variables for the noise generator (used for system setup)
7.	Play	PLAY_CMD	Resumes playing after a stop command
8.	Stop	STOP_CMD	Stops operation and mutes the output
9.	Mute	MUTE_CMD	Mutes the output without interrupting internal operation
10.	Unmute	UNMUTE_CMD	Restores output after a mute command
11.	Status	STAT_CMD	Reads the AC-3 bitstream commands (status register)
12.	Version number	VERSION_NUM_CMD	Reads the version number
13.	Audio Interface	AUDIOIF_CFG_CMD	Configures serial audio interface format, ADSCK, divider ratios, LR & BCK Master/Slave, etc.
14.	Set I/O	SETIO_CMD	Sets and reads the device general purpose I/O (GPIO) pins
15.	Input Select	INPUT_SEL_CMD	Selects serial audio source connected at input SDI0 or SDI1

NJU25301 Command Details[1]

Command 1: Set Task

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
1.	SET_TASK_CMD	0xC0	6	0

Set Task Command Details

The Set Task command controls the decoder's main operating characteristics. These are: Decode Mode (AC-3 or Linear PCM), Pro Logic decoding (ON/OFF), LFE (ON/OFF), Downmix Mode, PCM Scale Factor and Maximum Frame Repeat Before Muting.

Table 11 Set Task Parameters

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Decoding Mode			Pro Logic	Reserved			
2	Reserved				LFE	Downmix Mode		
3	PCM Scale Factor (Upper Byte)							
4	PCM Scale Factor (Lower Byte)							
5	Maximum Frame Repeat Before Muting (Upper Byte)							
6	Maximum Frame Repeat Before Muting (Lower Byte)							

1. Reset state default values are indicated by asterisks (*) or by text (default) in the command descriptions. Italicized text refers to variables in the AC-3 bitstream.

Parameter 1. Decoding Mode (Byte 1: Bits 7, 6, 5)

Sets the primary decoding mode.

Table 12 Set Task: Decoding Mode

Value	Description
000	AC-3 Decode (Test Only)
001	Reserved
010	Linear PCM Mode (Test Only)
011	Pink Noise Generator
100	Reserved (silence)
101	Reserved (silence)
110	Reserved (silence)
111*	Automatic Stream Detection*1

1. Automatic Stream Detection mode enables AC-3 decoding if an AC-3 input stream is detected, otherwise processes input as a Linear PCM stream.

Parameter 2. Pro Logic (Byte 1: Bit 4)

A value of 1 enables the Pro Logic decoder when the input is either PCM, or 2-channel Surround encoded AC-3. A value of 0 (default) disables the function.

Parameter 3. Low Frequency Effects (Byte 2: Bit 3)

A value of 1 (default) enables Dolby Digital LFE processing (subwoofer channel), while a value of 0 disables LFE processing. (It should be noted that only when an AC-3 encoded stream contains LFE information will audio be produced out of the subwoofer).

Parameter 4. Downmix Mode (Byte 2: Bits 2, 1, 0)

These bits are used to specify the output channel configurations for AC-3 decoding.

Table 13 Set Task: Downmix Mode

Value	Description	
000	1+1 (Dual Mono Mode)	L_O, R_O (Stereo)
001	1/0 (1 Front, 0 Rear)	C
010*1	2/0 (2 Front, 0 Rear)	L_T, R_T (Matrixed Surround)*1
011	3/0 (3 Front, 0 Rear)	L, C, R
100	2/1 (2 Front, 1 Rear)	L, R, S (Mono Surround)
101	3/1 (3 Front, 1 Rear)	L, C, R, S (Mono Surround)
110	2/2 (2 Front, 2 Rear)	L, R, SL, SR
111*2	3/2 (3 Front, 2 Rear)	L, C, R, SL, SR*2

1. Default if GPIO2=HIGH state during reset sequence.
2. Default if GPIO2=LOW state during reset sequence.

Parameter 5. PCM Scale Factor (Bytes 3, 4)

The PCM scale factor allows for volume control of all output channels. Byte 3 is the upper byte and byte 4 is the lower byte of the 16-bit scale multiplier. This multiplier is a two's complement fraction between zero 0x0000 and 0x7FFF (2^{15} -1). Multiplier values from 0x8000 to 0xFFFF are not used. Default parameter is 0x7FFF (0dB).

Parameter 6. Maximum Frame Repeat (Bytes 5, 6)

Byte 5 is the high byte and byte 6 is the low byte for the frame repeat function. In case of CRC error or an invalid bitstream, this command will allow the decoder to repeat the last valid frame until a new valid frame is received. The 16-bit control word indicates the maximum number of frames which will be repeated before the output will be muted. Default is 0x0000 (no repeat).

Command 2: AC-3 Decode

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
2.	AC3_CMD	0xC1	5	0

AC-3 Decode Command Details

These parameters are used to control specific aspects of the AC-3 decoding engine. These are: Dynamic Range Boost Factor (Dynscih), Dynamic Range Cut Factor (Dynscil), Compression Mode (Compmod) and Dual Mode (Dualmode).

Table 14 AC-3 Decode Parameters

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Dynscih (Upper Byte)							
2	Dynscih (Lower Byte)							
3	Dynscil (Upper Byte)							
4	Dynscil (Lower Byte)							
5	Reserved				Compmod		Dualmode	

Parameter 1. Dynamic Range Boost Factor (Dynscih) (Bytes 1, 2)

Byte 1 is the high byte and byte 2 is the low byte for dynamic range boost scale factor. The scale factor is a two's complement fraction between zero 0x0000 and 0x7FFF (2^{15} -1) which is used to scale the dynamic range. Parameter values from 0x8000 to 0xFFFF are not allowed. Default parameter is 0x0000. A value of zero disables dynamic range boost.

Parameter 2. Dynamic Range Cut Factor (Dynscil) (Bytes 3, 4)

Byte 3 is the high byte and byte 4 is the low byte for dynamic range cut scale factor. The parameter is a two's complement fraction between zero 0x0000 and 0x7FFF (2^{15} -1). Parameter values from 0x8000 to 0xFFFF are not allowed. Default parameter is 0x0000. A value of zero disables dynamic range cut.

Parameter 3. Compression Modes (Compmod) (Byte 5: Bits 3, 2)

Table 15 AC-3 Decode: Compression Modes

Value	Description
00	Custom Mode (Analog)[1]
01	Custom Mode (Digital)[1]
10*	Line Mode*
11	RF Mode

1. Both Custom Modes, Analog and Digital, defeat some or all of the features of the Line and RF Modes, thus shifting the burden to the product designer for implementation elsewhere in the audio path. If the Custom Modes are used, dialog normalization, dynamic compression, and downmixing functions must be accomplished external to the decoder IC.

Parameter 4. Dual Mode (Dualmode) (Byte Bits 1, 0)

Table 16 AC-3 Decode: Dual Mode

Value	Description
00*	Independent Channels*
01	Left Channel Copied to Both Left and Right Channels
10	Right Channel Copied to Both Left and Right Channels
11	Inputs Scaled by -6dB, Summed, and Sent to Both Channels

Command 3: Pro Logic Decode

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
3.	PRO_LOGIC_CMD	0xC4	1	0

Pro Logic Decode Command Details

This command configures variables for Pro Logic decoding such as: setting the decoding coefficients to match the audio sampling rate, Wide Surround (ON/OFF), Auto Balance (ON/OFF), Stereo 3 (ON/OFF), and Phantom Center (ON/OFF).

Table 17 Pro Logic Decode Parameters

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved		Sample Rate		Wide Surround	Auto Balance	Stereo 3	Phantom Center

Parameter 1. Sample Rate (Samprate) (Byte 1: Bits 5, 4)

Sets Pro Logic decoding coefficients to match the system audio sample rate. Note: This command does not cause or determine the sampling rate at the serial audio interface.

Table 18 Pro Logic Decode: Sample Rate

Value	Description
00*	Sample Rate = 48 kHz*
01	Sample Rate = 44.1 kHz
10	Sample Rate = 32 kHz
11	Sample Rate = 22.05 kHz

Parameter 2. Wide Surround (Byte 1: Bit 3)

A value of 0 (default) applies a 7 kHz low pass filter and a Dolby B noise reduction on the surround channel. A value of 1 allows for the surround channel to have full audio bandwidth.

Parameter 3. Auto Balance (Byte 1: Bit 2)

A value of 1 enables auto balance, while a value of 0 (default) disables the function.

Parameter 4. Stereo 3 (Byte 1: Bit 1)

A value of 1 enables the surround channel, while a value of 0 (default) disables the surround channel.

Parameter 5. Phantom Center (Byte 1: Bit 0)

A value of 1 disables the center speaker, mixing the left and right to create a phantom center channel, while a value of 0 (default) enables the center channel.

Command 4: Bass Management Configuration

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
4.	BASS_MGMT_CFG_CMD	0xC5	1	0

Bass Management Configuration Command Details

This command sets the Bass Management Configuration. Byte 1, Bits 3-0 set which mode the NJU25301 will be set to. Mode 0 disables Bass Management altogether.

Table 19 Bass Management Configuration Parameters[1]

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	0	0	Bass Management Configuration Mode			

1. Byte 2, bits 7-4 must be set to zero.

Table 20 Bass Management Configuration Modes

Value[1]	Configuration	Mode Legal Only When Processing...	Configuration Description
0000"	Mode 0"	Either Class of Stream	Bass Management Disabled"
0001	Mode 1[2]	AC-3 Discrete Channel Stream	Bass from all 5 channels is redirected to the Subwoofer. This is in addition to the LFE information the Subwoofer is already receiving.
0010	Mode 2[3]	AC-3 Discrete Channel Stream	Bass from Center and Surround channels is redirected to the Left and Right channels and Subwoofer. For the Left and Right channels, this is additional bass. For the Subwoofer, this is in addition to the LFE information.
0011	Mode 3	AC-3 Discrete Channel Stream	Bass from the Center channel is redirected to the Left and Right channels. For the Left and Right channels, this is additional bass. The Subwoofer only receives LFE information.
0100	Mode 4	AC-3 Discrete Channel Stream	Bass from Center channel and all LFE information is redirected to the Front and Surround channels. No information is sent to the Subwoofer.
0101	Mode 5	Pro Logic Encoded Stream	Bass from Left, Right and Center channels are redirected to the Subwoofer.
0111	Mode 7	Pro Logic Encoded Stream	Bass from Center channel is redirected to the Subwoofer.
1000	Mode 8	Pro Logic Encoded Stream	Bass from Center channel is redirected to Left and Right channels. No information is sent to the Subwoofer.
1010	Mode 10[4]	AC-3 Discrete Channel Stream	Bass from Center and Surround channels is redirected to Left and Right channels. Only LFE information is sent to the Subwoofer.

1. All other values than those listed here are invalid.
2. Applies only when NJU25301 is processing an AC-3 discrete channel stream only. Should the NJU25301 be sent a Pro Logic encoded stream, it will automatically switch to Mode 5. Vice Versa scenario applies.
3. Applies only when NJU25301 is processing an AC-3 discrete channel stream only. Should the NJU25301 be sent a Pro Logic encoded stream, it will automatically switch to Mode 7. Vice Versa scenario applies.
4. Applies only when NJU25301 is processing an AC-3 discrete channel stream only. Should the NJU25301 be sent a Pro Logic encoded stream, it will automatically switch to Mode 8. Vice Versa scenario applies.

Command 5: Delay Configuration

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
5.	DELAY_CFG_CMD	0xC6	4	0

Delay Configuration Command Details

Delay Configuration sets the time delay applied to surround channels and center channel when AC-3 or Pro Logic decoding is active. Center and surround delays are expressed as 16-bit words that represent delay as a number of audio sample periods. Thus the delay time is a function of the audio sampling rate: Delay(mS)= DELAY/Audio Sample Rate(kHz).

Maximum allowed delay settings for AC-3 decoding and delay time at 48kHz sample rate:
Center: DELAY=0x00EF(max)/48 kHz = 5mS
Surround: DELAY=0x02CF(max)/48 kHz = 15mS

Maximum allowed delays for Dolby ProLogic decoding at 48kHz sample rate:
Center: DELAY=0x00EF(max)/48 kHz = 5mS
Surround: DELAY=0x059F(max)/48 kHz = 30mS

Table 21 Delay Configuration Parameters[1]

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Surround Delay (Upper Byte)							
2	Surround Delay (Lower Byte)							
3	Center Delay (Upper Byte)							
4	Center Delay (Lower Byte)							

1. Surround Delay default value is 0 ms (0x0000). Center Delay default value is 0 ms (0x0000).

Command 6: Pink Noise Generator

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
6.	PINK_NOISE_CMD	0xC7	3	0

Pink Noise Generator Command Details

This command sets the global variables for the pink noise generator function.

Table 22 Pink Noise Generator Parameters[1]

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved	Sequence	Left	Right	Center	Left Surround	Right surround	Subwoofer
2	Noise Scale Factor (Upper Byte)							
3	Noise Scale Factor (Lower Byte)							

1. All Bits in Byte1 are mutually exclusive. If more than one are set, the least most significant bit is effective. The default value of Byte 1 is 01000000b.

A value of 1 in bits 6:0 enables pink noise for the selected channel. Bit 6 (sequence) automatically sequences noise as L, C, R, SL, SR, in two second intervals. The Noise Scale Factor (bytes 2 and 3) is a 16-bit word which controls noise amplitude. Scale factor is a two's complement fraction between zero 0x0000 and 0x7FFF (2^{15} -1). Values from 0x8000 to 0xFFFF are not used. Default parameter is 0x7FFF (0dB).

Command 7: Play

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
7.	PLAY_CMD	0xC9	0	0

Play Command Details

The Play command resumes operation of the selected function and restores the output after a Stop command. Play and Stop commands do not apply to Noise Generator.

Command 8: Stop

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
8.	STOP_CMD	0xCA	0	0

Stop Command Details

The Stop command stops operation of the selected function and mutes the output. New data is ignored until a new Play command is sent. Play and Stop commands do not apply to Noise Generator.

Command 9: Mute

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
9.	MUTE_CMD	0xCB	0	0

Mute Command Details

The Mute command mutes the output without interrupting the selected function. Mute and Unmute commands do not apply to Noise Generator.

Command 10: Unmute

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
10.	UNMUTE_CMD	0xCC	0	0

Unmute Command Details

The Unmute command restores the output while continuing the selected function. Mute and Unmute commands do not apply to Noise Generator.

Command 11: Status

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
11.	STAT_CMD	0xCD	0	11

Status Command Details

The Status command returns for 11 words of the status register to the host.

Table 23 Status Parameters

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	run_stat (run status)		out_stat (AC-3 decode status)			in_stat (AC-3 frame information status)		
2	fscod (sample rate)		frmsizcod (input data rate in kilobits per second)					
3	Reserved				lfeon	acmod (coding configuration)		
4	bsid (bitstream identification number of five bits)					bsmod (bitstream mode)		
5	cmixlev (center mix level)		smixlev (surround mix level)		dsurmod (Dolby surround)	copyrightb[1]	origbs[2]	
6	Reserved			dialnorm (dialogue normalization for channel 2 in dual mono mode)				
7	Reserved			dialnorm (dialogue normalization value for normal operation)				
8	langod2 (language code for channel 2 in dual mono mode)							
9	langod (language code for normal operation)							
10	audprodie2[3]	roomtyp2 (room type)[4]		mixlevel2 (mix level for channel 2)[4]				
11	audprodie[5]	roomtyp[6]		Mixlevel (mix level)[6]				

1. copyrightb = copyright information
2. origbs = original bitstream information
3. audprodie2 = production information in dual mono operation mode
4. mixlevel2, roomtyp2 = mix level and room type in dual mono operation mode
5. audprodie = production information in normal operation mode
6. mixlevel, roomtyp = mix level and room type in normal operation mode

Command 12: Version Number

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
12.	VERSION_NUM_CMD	0xCE	0	4

Version Number Command Details

The Version Number command returns four bytes representing version of the ROM-encoded firmware.

Table 24 Status Parameters

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Firmware Version [31:24]							
2	Firmware Version [23:16]							
3	Firmware Version [15:8]							
4	Firmware Version [7:0]							

Command 13: Serial Audio Interface Configuration

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
13.	AUDIO_CFG_CMD	0xCF	9	0

Serial Audio Interface Configuration Command Details

The Serial Audio Interface Configuration command sets serial audio format and clock configurations. The command also set divide ratios for BCK clock outputs, Serial Audio Word Size, Audio Format, Clocks per Frame, Internal Bit Clock Divider and MASTER/SLAVE mode.

Table 25 Serial Audio Interface Configuration Parameters[1]

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	0	0	0	0	0	0
2	0	1	ADSCK[2]	1	0	1	0	0
3	1	0	0	0	0	0	0	0
4	0	1	1	1	0	1	0	0
5	0	1	0	0	Serial Audio Word Size[3]			Audio Format[4]
6	Audio Format[4]	Clocks/Frame[5]	0	Internal Bit Clock Divider[6] (BCKO)			MASTER[7]	0
7	0	0	0	0	0	0	0	0
8	0	0	MASTER[7]	0	0	MASTER[7]	0	0
9	1	1	1	0	0	0	1	0

1. All fixed bits must be set by the host microcontroller for proper operation.
2. Divide ratios for ADSCK are set here. When ADSCK is set HIGH, the system clock rate provided at XI is divided by 64 and output on the ADSCK pin, giving 64Fs. When ADSCK is set LOW (default), the output is the system clock divided by 128, giving 32Fs. This signal is usually used for clocking a system microcontroller, but can drive A/Ds and D/As. BCKO is the signal that is normally connected to A/Ds and D/As.
3. The Serial Audio Word Size is set here. Bit 3 is the MSB and Bit 1 is the LSB. Set the word size to either: 000 = 16-bits, 001 = 18-bits, 010 = 20-bits, or 011 = 24-bits (default).
4. The Serial Audio Data Format is set here. Byte 5, Bit 0 is the MSB. Byte 6, Bit 7 is the LSB. Hence, 00 = MSB-First Right-Justified Format, 01 = MSB-First Left-Justified Format, 10 = I^2S Format (default).
5. Setting Clocks/Frame to HIGH (default) sets the device to expect 64 clocks per LR Frame. Setting Clocks/Frame to LOW set the device to set expect 32 clocks per LR Frame.
6. The divide ratio for the internal bit clock is set here. If the device is in MASTER mode, then this parameter needs to be set to 001 so that the 256Fs source is divided by 4, giving a 64Fs bit clock. If the device is in SLAVE mode, the clock source is BCKI, hence the parameter should be set to 000 (divide ratio of 1). In either case, this signal is output on BCKO. ADSCK and BCKO are independent of each other.
7. Must be set HIGH if in the NJU25301 is to operate in MASTER mode or set LOW if in SLAVE mode (default). This determines the generator source for the LRO and BCK pins.

MCK and BCK pins deliver constant frequency clocks generated by dividing the DSP clock at input pin XI. MCK is intended to provide system clock for A/D and D/A converters when NJU25301 operates as the MASTER serial audio clock source. Both MCK and ADSCK halt when RESET input is LOW.

Table 26 Typical Serial Audio Data Format, ADSCK, Clocks/Frame, and Master/Slave Configurations[1]

Serial Audio Data Format	Word Size	ADSCK	Clocks/Frame	LR & BCK in SLAVE Mode	LR & BCK in MASTER Mode
I^2S	16-bit	32Fs	32	00 54 80 74 41 00 00 00 E2	00 54 80 74 41 06 00 24 E2
Left-Justified	16-bit	32Fs	32	00 54 80 74 40 80 00 00 E2	00 54 80 74 40 86 00 24 E2
Right-Justified	16-bit	32Fs	32	00 54 80 74 40 00 00 00 E2	00 54 80 74 40 06 00 24 E2
I^2S	18-bit	64Fs	64	00 74 80 74 43 40 00 00 E2	00 74 80 74 43 46 00 24 E2
Left-Justified	18-bit	64Fs	64	00 74 80 74 42 C0 00 00 E2	00 74 80 74 42 C6 00 24 E2
Right-Justified	18-bit	64Fs	64	00 74 80 74 42 40 00 00 E2	00 74 80 74 42 46 00 24 E2
I^2S	24-bit	64Fs	64	00 74 80 74 47 40 00 00 E2	00 74 80 74 47 46 00 24 E2
Left-Justified	24-bit	64Fs	64	00 74 80 74 46 C0 00 00 E2	00 74 80 74 46 C6 00 24 E2
Right-Justified	24-bit	64Fs	64	00 74 80 74 46 40 00 00 E2	00 74 80 74 46 46 00 24 E2

1. The entire serial audio interface configuration sequence of bytes is listed under the corresponding SLAVE or MASTER Clock Mode columns. It is assumed that the Internal Bit Clock divider is set to 4 when in MASTER Mode and 1 when in SLAVE Mode

Command 14: Set I/O

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
14.	SETIO_CMD	0xD1	1	1

Set I/O Command Details

This command is used to read and write the device four general purpose I/O pins, GPIO3-GPIO0 (pins 10, 9, 8, and 7). The upper four bits [7:4] set the direction of GPIO3-GPIO0, where 0 = Input and 1 = Output. The lower four bits [3:0] are either data bits for GPIO3-GPIO0 or status bits, depending on whether the user is writing or reading to the GPIO registers.

Table 27 Set I/O Write Byte Parameters

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	GPIO3 I/O	GPIO2 I/O	GPIO1 I/O	GPIO0 I/O	GPIO3 Data	GPIO2 Data	GPIO1 Data	GPIO0 Data

Table 28 Set I/O Read Byte Parameters

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	GPIO3 I/O	GPIO2 I/O	GPIO1 I/O	GPIO0 I/O	GPIO3 Status	GPIO2 Status	GPIO1 Status	GPIO0 Status

Command 15: Input Select

No.	Mnemonic	OpCode +	Bytes Written	Bytes Read
15.	INPUT_SEL_CMD	0xD7	1	0

Input Select Command Details

This command selects input terminal SDI0 (pin 75) or SDI1 (pin 76) as the active serial data input for decoding. Input SDI0 accepts either AC-3 or PCM data. Input SDI1 accepts only PCM data.

Table 29 Input Select Parameters[1]

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	X	X	X	X	X	X	X	SDI[2]

1. X = Don't Care.
2. When SDI is set LOW, SDI0 is the active input. When SDIO is set HIGH, SDI1 is the active input.

Serial Audio Interface

The serial audio interface carries audio data, both encoded and decoded, to and from the NJU25301 . Industry standard serial data formats of I^2S, MSB-first left-justified or MSB-first right-justified are supported. These serial audio formats define a pair of digital audio signals (stereo audio) on each data line. Two clock lines, BCK (bit clock) and LR (left/right word clock) establish timing for serial data transfers. More than one data line can be associated with a pair of BCK and LR clock lines.

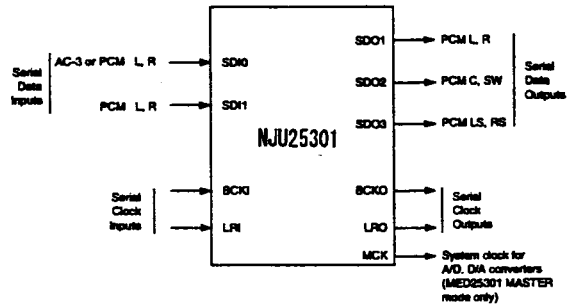
The NJU25301 serial audio interface includes two data input lines; SDI0 and SDI1 and three data output lines, SDO1, SDO2, SDO3 as shown in the figure below. Primary data input SDI0 accepts encoded AC-3 (Dolby Digital data) or stereo linear PCM (pulse-coded modulation) data. Auxiliary data input SDI1 accepts only stereo linear PCM data. Data outputs SDO1, SD02, and SDO3 deliver up to six channels of audio output data to external D/A converters.

NJU25301 has a pair of left/right clock lines (LRI and LRO) and a pair of bit clock lines (BCKI and BCKO). Normally, data transfer on all five serial data inputs and outputs are timed relative to serial clock outputs BCKO and LRO. Clock inputs BCKI and LRI are used to accept timing signals from an external device when the NJU25301 is operating in SLAVE clock mode.

System clock output, MCK, is provided for delta-sigma A/D and D/A converters when NJU25301 operates in MASTER mode.

ADSCK is not usually connected to A/Ds or D/As, but can may be required for older A/Ds and D/As. The ADSCK is normally used to drive the system clock for the host microcontroller. At 32Fs it provides approximately a 3MHz clock.

Figure 33 NJU25301 Pinout for Serial Audio Interface



Serial Audio Data Formats

The NJU25301 can exchange data using any of three industry-standard digital audio data formats: I^2S, Left-justified, or Right-justified. Bit order is MSB-first, LSB-last for all formats.

The three serial formats differ primarily in the placement of the audio data word relative to the LR clock. Left-justified format places the most-significant data bit (MSB) as the first bit after an LR transition. I^2S format places the most-significant data bit (MSB) as the second bit after an LR transition (one bit delay relative to left-justified format). Right-justified format places the least-significant data bit (LSB) as the last bit before an LR transition.

Clock LR (LRI, LRO) marks data word boundaries and clock BCK (BCKI, BCKO) clocks the transfer of serial data bits. One period of LR defines a complete stereo audio sample and thus the rate of LR equals the audio sample rate (Fs). All formats transmit the stereo sample left channel first. Note that polarity of LR is opposite in I^2S format (LR:LOW = Left channel data) compared to Left-Justified or Right-Justified formats.

BCK is the serial data bit clock. Transmitting devices always change data on the falling edge of BCK while receiving devices accept data on the rising edge of BCK. The number of BCK cycles must equal or exceed the number of data bits in the stereo audio sample. Extra BCK clock cycles that exceed the number of data bits are ignored. For older A/Ds and D/As, sometimes a 32Fs or 64Fs clock is required. The various serial audio word sizes and formats, in combination with ADSCK settings of 64Fs and 32Fs, are shown in the figures on the following pages. 64Fs is a commonly chosen rate for ADSCK when handling serial audio data over 16-bits.

Since right-justified format justifies data at the least-significant data bit the position of most-significant data bit will shift with data word length. Word length configuration of senders and receivers must therefore match when using right-justified mode or data will not transfer correctly. By contrast, I^2S and left-justified formats justify data at the most-significant bit (MSB). Configuring senders and receivers with different word lengths will limit data size to the minimum of the two word length settings but will not otherwise cause data transmission errors. Example: Connect both an 18-bit and a 24-bit D/A converter to the NJU25301 using I^2S format. Configure the NJU25301 to 24-bit word length. The 18-bit D/A converter will ignore the six least-significant bits and operate correctly at 18-bit resolution.

Serial Audio Data Functional Timing Diagrams

Figure 34 Left-Justified Data Format, ADSCK = 64 Fs, 24-bit Data

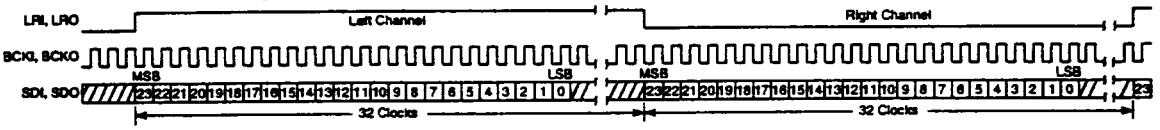


Figure 35 Right-Justified Data Format, ADSCK = 64 Fs, 24-bit Data

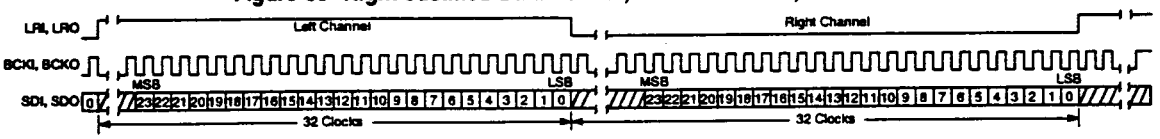


Figure 36 I²S Data Format, ADSCK = 64 Fs, 24-bit Data

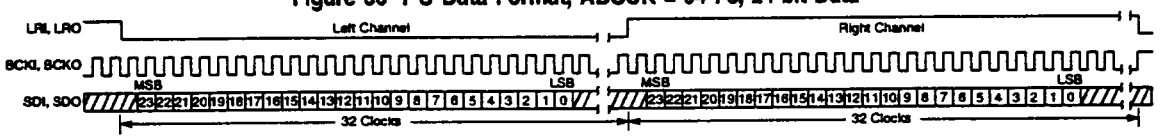


Figure 37 Left-Justified Data Format, ADSCK = 64 Fs, 20-bit Data

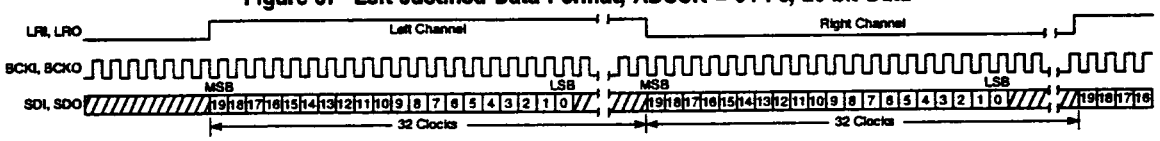


Figure 38 Right-Justified Data Format, ADSCK = 64 Fs, 20-bit Data

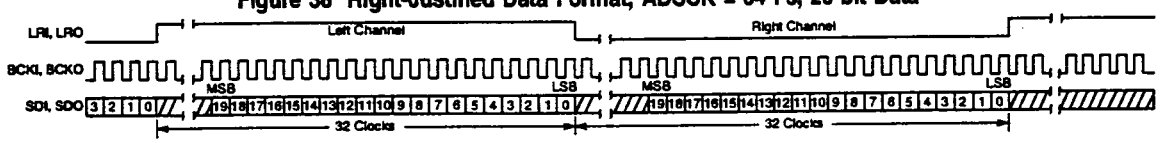


Figure 39 I²S Data Format, ADSCK = 64 Fs, 20-bit Data

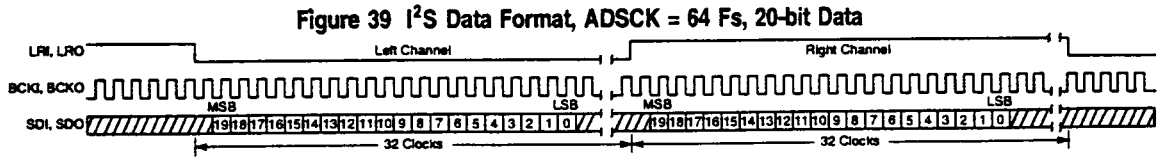
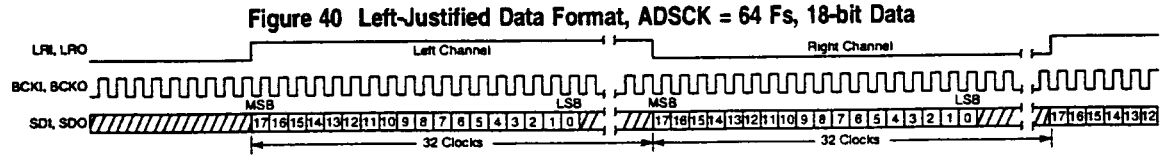


Figure 40 Left-Justified Data Format, ADSCK = 64 Fs, 18-bit Data



Serial Audio Data Functional Timing Diagrams (continued)

Figure 41 Right-Justified Data Format, ADSCK = 64 Fs, 18-bit Data

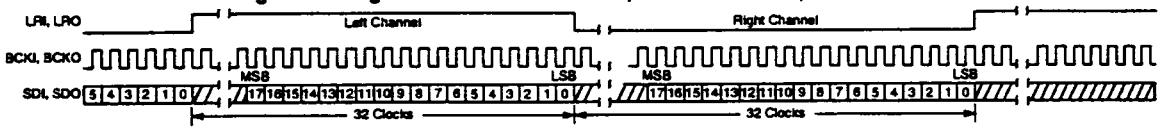


Figure 42 I²S Data Format, ADSCK = 64 Fs, 18-bit Data

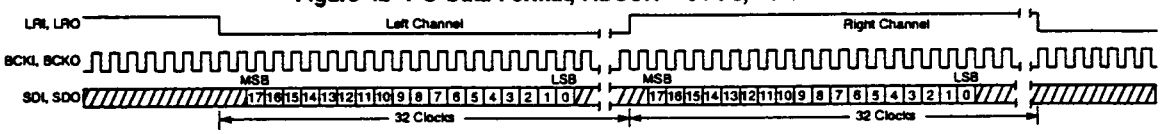


Figure 43 Left-Justified Data Format, ADSCK = 32 Fs, 16-bit Data

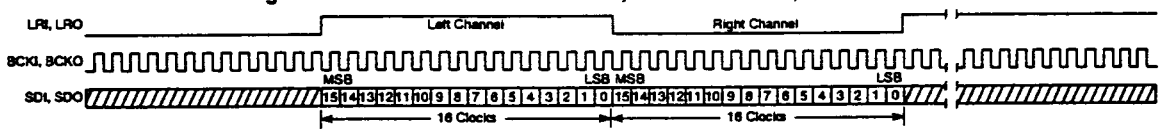


Figure 44 Right-Justified Data Format, ADSCK = 32 Fs, 16-bit Data

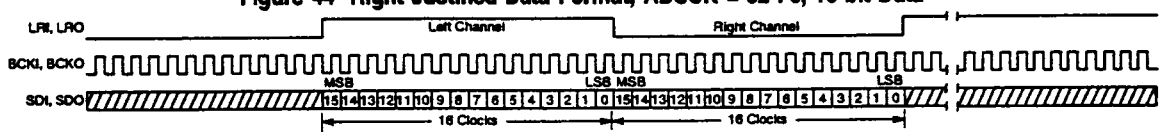
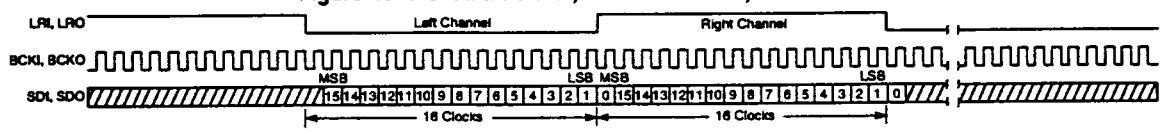


Figure 45 I²S Data Format, ADSCK = 32 Fs, 16-bit Data



Serial Audio Clocks

Three types of clock signals are included in the serial audio interface. Two of the clock signals LR (LRI and LRO) and BCK (BCKI and BCKO) establish data transfer on the serial data lines as described in the previous section. A third clock, MCK, is not associated with serial data transfer but is required by delta-sigma A/D and D/A converters. In older A/Ds and D/As, an additional clock of 32Fs or 64Fs is required. This is what ADSCK can be used for.

The frequency of the LR clock is, by definition, equal to the digital audio sample rate, Fs. BCK and MCK operate at multiples of the LR clock rate. Therefore the signals LR, BCK and MCK must be locked, that is, they must be generated or derived from a single frequency reference.

The LR clock frequency also establishes the rate that the NJU25301 digital signal processor processes audio samples. Some digital audio processes of NJU25301 have time constants or frequency response that are a function of the audio sample period (1/Fs). In order to maintain constant time and frequency response for different audio sample rates information about the current sample rate must be sent to the NJU25301 by a host I/O interface command (see PRO_LOGIC_CMD; sample rate command).

System Master Clock Source

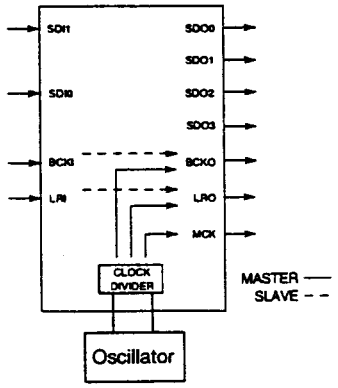
Audio data samples must be transferred in synchronism between all components of the digital audio system. That is, for each audio sample originated by an audio source there must be one and only one audio sample processed by the NJU25301 and delivered to the D/A converters[1]. To accomplish this, one device in the system is selected to generate the audio sample rate; the remaining devices are designated to follow this sample rate. The device that generates the audio sample rate is called the MASTER device; all devices following this sample rate are called SLAVE(s).

Table 30 Typical Serial Audio Clock Frequencies and their corresponding BCK and MCK Rates[1]

Clock Signal	Typical Multiples	32 kHz	44.1 kHZ	48 kHz
LR	1Fs (by definition)	32 kHz	44.1 kHz	48 kHz
BCK	64Fs	2.048 MHz	2.822 MHz	3.072 MHz
MCK	256Fs	8.192 MHz	11.289 MHz	12.288 MHz

1. Some common audio sample rates and data types are: 44.1 kHz - Music (PCM) on Compact Disk (CD); 48 kHz - Dolby Digital (AC-3) on Laserdiscs and DVDs.

Figure 46 Master/Slave Configuration



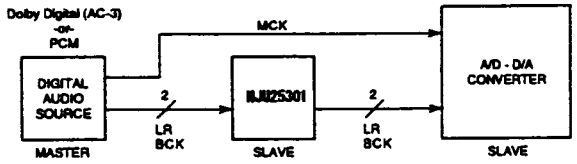
1. Note: Although AC-3 data does not correlate to audio signals on a sample by sample basis, AC-3 data packets are encoded to transfer at the same rate as the audio sample rate.

NJU25301 Master/Slave Mode System Examples

System Example 1

A digital audio source supplies Dolby Digital or PCM data to the NJU25301 decoding system. The digital audio source is the clock MASTER and delivers LR and BCK clock signals to the NJU25301 processor (SLAVE), which in turn passes these same clocks to the A/D and D/A converters (also SLAVES). All serial audio data transfers (not shown in drawing) are timed by these LR and BCK clocks. System clock MCK, also generated by the digital audio source, is delivered only to the A/D and D/A converters.

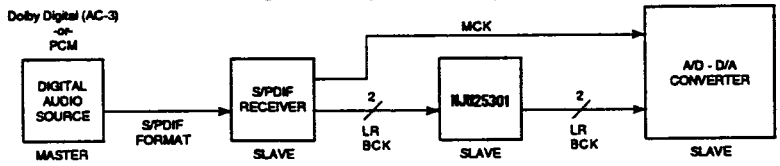
Figure 47 System Example 1



System Example 2

Similar to Example 1, except a S/PDIF receiver receives data from the digital audio source in S/PDIF format. S/PDIF is commonly used to transport digital audio data from a source such as a DVD player or CD player to a decoder such as an A/V Receiver. The S/PDIF receiver is a SLAVE device since it regenerates LR, BCK, and MCK signals from the clock reference in the Digital Audio Source (MASTER).

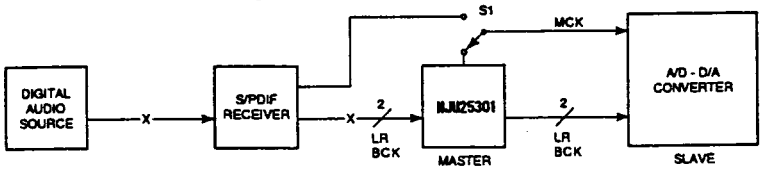
Figure 48 System Example 2



System Example 3

When the digital audio source is not running or is disconnected, the master clock must be supplied from another source. NJU25301 can be enabled to operate as a clock MASTER by sending a command over the Serial Host interface. Switch S1 is implemented in hardware to supply MCK signals for the A/D and D/A converters. S1 connects to the NJU25301 MCK output when NJU25301 is in MASTER mode and connects to the other MASTER device supplying MCK when NJU25301 is in SLAVE mode.

Figure 49 System Example 3



The table below shows the NJU25301 clock modes permissible with system example three above.

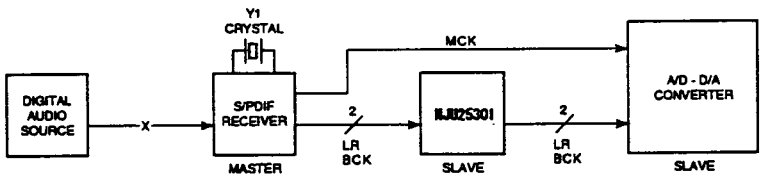
Table 31 Available NJU25301 Clock Modes vs. Audio Functions and Digital Input Stream

NJU25301 Audio Function	Digital Audio Source Stream Present?	
	Yes	No
Input from Digital Audio Source (AC-3 or PCM)	SLAVE	N/A
Input from Local A/D Converter (PCM)	SLAVE or MASTER	MASTER
Generate Pink Noise	SLAVE or MASTER	MASTER

System Example 4

Another way to supply MASTER clock when digital audio source is disconnected is to use a S/PDIF receiver with MASTER or SLAVE capability. This S/PDIF receiver automatically switches to become a clock MASTER when a valid S/PDIF input is not detected. LR, BCK and MCK clocks are generated from crystal Y1 when S/PDIF receiver is in MASTER mode and from the digital audio source when S/PDIF receiver is in SLAVE mode.

Figure 50 System Example 4



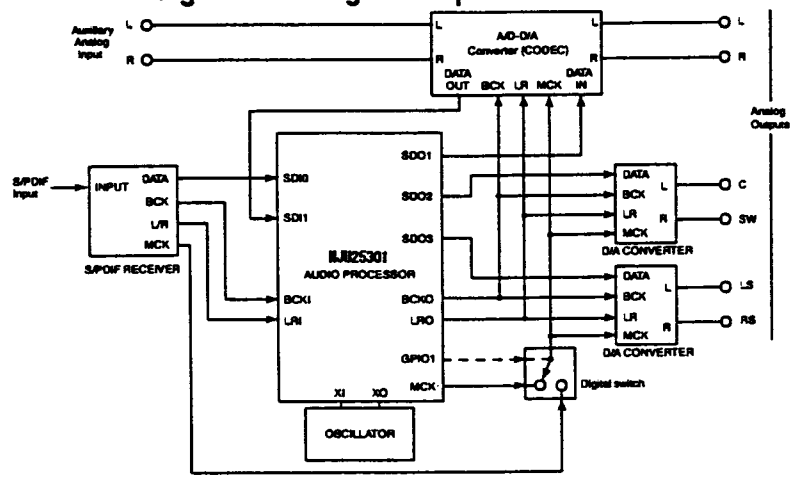
Note that in system example four the NJU25301 operates solely in SLAVE mode. The NJU25301 must always be set to SLAVE clock mode to receive inputs originating from the independently-clocked digital audio source. The NJU25301 may also operate in SLAVE mode to receive input from the A/D converter or to generate pink noise but only if a valid signal from the digital audio source is present to provide clocks. MASTER mode can always be used for A/D converter inputs or pink noise regardless of the digital audio source. The NJU25301 audio interface includes two sets of data timing signals: BCKI, LRI which are inputs and BCKO, LRO which are outputs. In SLAVE mode the BCKI, LRI inputs accept timing signals and transfer these signals to BCKO, LRO outputs. In MASTER mode the NJU25301 generates signals for BCKO and LRO outputs by dividing the clock connected at pin XI. Signals at inputs BCKI and LRI are ignored.

The standard application configuration is to connect the clock from an external data source to inputs BCKI and LRI and to connect all SLAVE devices requiring clocks to outputs BCKO and LRO. The NJU25301 can be configured in MASTER or SLAVE configurations by sending commands to the NJU25301 Host I/O.The table below shows the NJU25301 clock modes permissible with system example three above (note that in system example four the NJU25301 operates solely in SLAVE mode). The NJU25301 must always be set to SLAVE clock mode to receive inputs originating from the independently-clocked digital audio source. NJU25301 may also operate in SLAVE mode to receive input from the A/D converter or to generate pink noise but only if a valid signal from the digital audio source is present to provide clocks. MASTER mode can always be used for A/D converter inputs or pink noise regardless of the digital audio source.

Design Example with S/PDIF

Following is an example of a typical system where the NJU25301 accepts S/PDIF (AES/EBU) digital format input and delivers from two to six analog outputs. An optional stereo analog input can be selected in place of the S/PDIF input.

Figure 51 Design Example with S/PDIF



Control Interface

Functional states of the NJU25301 are determined initially by the reset state and are subsequently altered by commands sent to the Serial Host Interface. The Command Table describes the complete NJU25301 command set.

Reset States

The NJU25301 is forced into reset state by pulling the device $\overline{\text{RESET}}$ input LOW, then set HIGH. A minimum of 1mS should be allowed for the Reset Sequence to complete before the host sends the first command. Reset state is described in terms of default command equivalents listed in the NJU25301 command table. Reset state is also a function of the logic levels applied to GPIO pin 2 and GPI0 pin 3 during the reset sequence.

The level at GPIO2 input during reset sequence establishes the AC-3 Downmix mode. If GPIO2 is set LOW, then downmixing is disabled allowing a 3/2 stream to play out of all 5.1 channels. If GPIO2 = HIGH, then a downmix to 2.1 channels is performed, allowing a 3/2 stream to play out of only 2.1 channels. (It should be noted that in either case audio will only be present from the subwoofer if there exits LFE information in the AC-3 stream. Neither of these modes redirects bass to the subwoofer, but only lets it pass through to the LFE output). For applications without a system microcontroller, GPIO2 can be hard-wired to initialize NJU25301 in either a 5.1 channel or 2.1 channel Dolby Digital decoding output configuration. Input Serial Audio Format auto-detect is active on initialization so either Dolby Digital or linear PCM inputs can be processed automatically.

The level at GPIO3 input configures the Serial Host Interface (SHI) to operate in I^2C-bus or SPI bus serial format. If GPIO3 is set LOW, then SPI bus is the chosen SHI protocol. If GPIO3 is set HIGH, the I^2C-bus is the chosen SHI protocol.

Both GPIO2 and GPIO3 are sampled within 1mS after $\overline{\text{RESET}}$ goes HIGH. Both GPIO2 and GPIO3 can be programmed for other I/O purposes by the SHI after the 1mS reset sequence completes. On device power up, $\overline{\text{RESET}}$ should remain LOW for at least 10ms after supply voltage reaches a minimum of 4.75 V, in order to allow the crystal oscillator to stabilize.

Serial Host Interface

The NJU25301 can be controlled via a Serial Host Interface (SHI) using either of two industry standard serial bus formats: I²C-bus or SPI bus. Serial bus format is selected by GPIO3 pin during device initialization. Data transfers are in eight bit packets (one byte) when using either format. The SHI operates only in a slave fashion. A host microcontroller connected to the interface always drives the clock (SCL/SCK) line and initiates data transfers, regardless of the chosen communication protocol.

Table 32 Pin Connections of the NJU25301 Serial Host Interface

Pin Name	Pin Number	I²C-Bus Format Function	SPI Bus Format Function
SCL/SCK	13	Serial Clock	Serial Clock
SDA/SDOUT[1]	14	Serial Data (Bi-directional)	Serial Data Output
AD1/SDIN	15	I²C-bus Address, Bit 1	Serial Data Input
AD3/$\overline{SS}$	16	I²C-bus Address, Bit 3	Slave Select

1. SDA/SDOUT pin is an open-drain output. A pullup resistor (4.7k nominal) is required for either I²C-bus or SPI bus communication protocols.

SPI Bus

The serial host interface can be configured for SPI (Serial Peripheral Interface) bus communication by clearing the GPIO3 pin during the Reset Sequence initialization. SPI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the slave select pin LOW ($\overline{SS}$ = 0). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transition of $\overline{SS}$.

I²C-Bus

When configured for I²C-bus communication the serial host interface transfers data on the SDA pin and clocks data with the SCL pin. SDA is an open drain pin requiring an external pull-up resistor (4.7k ohm nominal). Pins AD1 and AD3 are used to configure the seven-bit slave address of the serial host interface. This offers additional flexibility in a system design by offering four different possible slave addresses for which the NJU25301 will respond to.

Table 33 I²C-Bus Slave Address[1]

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit 0
1	0	0	1	1	1	1	AD1	R/$\overline{W}$[2]

When R/W is set HIGH, this indicates to the device that it is in READ mode. When R/W is set LOW, this indicates that it is in WRITE mode. Please refer to the I²C-bus specification for further explanation.

The figure on the following page shows the basic timing relationships for data transfers. A transfer is initiated with a START condition, followed by the slave address byte. The slave address consists of the seven-bit slave address followed by a read/$\overline{write}$ (R/$\overline{W}$) bit. When the serial host interface recognizes a valid address, it returns an acknowledge bit on the ninth clock cycle by pulling the SDA line LOW.

The R/$\overline{W}$ bit in the slave address byte sets the direction of data flow until a STOP condition terminates the transfer: R/$\overline{W}$ = 0 indicates the host will send data to the NJU25301 while R/$\overline{W}$ = 1 indicates the host will receive data from the NJU25301. Any number of bytes may be sent or received during a transfer under the I²C-bus standard, however single-byte transfers are recommended for NJU25301 communication as described in the next section. Repeat START conditions, in which the host does not have to generate a STOP condition before a second START, are not supported. The serial host interface supports both "Standard-Mode" (100kbps) and "Fast-Mode" (400kbps) I²C-bus data transfers. For further explanation of the I²C-bus, please refer to the "THE I²C-BUS SPECIFICATION: VERSION 2.0, 1998" available from Philips Electronics N.V.

Communication Protocol

The NJU25301 commands are composed as sequences of one or more bytes. Commands may consist as a single opcode, or as an opcode followed by a specified number of parameters. Some commands return data values to the host. The opcode, number of bytes written and number of bytes returned are specified in the Command Table for each command.

Communication between the host and NJU25301 is bidirectional. The host (bus MASTER) drives command sequences by sending bytes to the NJU25301 (bus SLAVE). The NJU25301 generates a single byte response for every byte received from the host. In addition to the command sequence initializing opcode and the subsequent bytes written, the host will issue two types of flow control bytes to drive communication. READ bytes are issued when the host expects a return of data values according to the command specification. No operation (NOP) bytes are issued at the end of a command sequence and in wait-loops when the host tests if the MED25301 is ready for the next command.

The NJU25301 response to the host includes three classes of bytes: Command Bytes Remaining Count, Data and Status. Data bytes are returned when a READ byte is received from the host. The total count of command bytes is returned after the host issues the specified command. This count value begins at the number of bytes expected (number under "Bytes Written" in each Command Table) for the particular command and decrements as the command sequence proceeds. Status Bytes are returned when the command opcode is issued by the host, when the command sequence terminates, and during wait-loops.

Table 34 Classes of Bytes Sent from the Host to the NJU25301

Byte Class	Value	Description
Opcode	(See Command Table)	Command Operation Code
Command	(See Command Table)	Command Data (included for some commands)
Flow Control: READ	0xD4	Prompts Status Data to be Sent from MED25301
Flow Control: NOP	0xFF	Terminates Command Sequence

Table 35 Classes of Bytes Sent from the NJU25301 to the Host

Byte Class	Value	Description
Command Bytes Remaining Count	Number of Bytes Remaining (1 to N)	Number of Bytes Expected to Complete Command Table
Data	Data	Data Returned (included for some commands)
Status: READY/OK	0x00	The MED25301 is ready for the next command
Status: COMMAND ACCEPTED	0x80	The last command sent to the MED25301 was valid
Status: COMMAND ERROR	0x81	Invalid Opcode or invalid number of READ bytes received
Status: NOT READY	0x83	Busy, not ready for next command

Command Sequence Using I^2C-Bus

Communication between the host and the NJU25301 is synchronized by byte stream content. I^2C-bus START and STOP conditions do not delineate the beginning or end of a command sequence. In order to read response bytes from NJU25301 the host must alternate single-byte I^2C-bus writes with single-byte I^2C-bus reads. Command sequence steps are driven by writes from the host. If multiple bytes are written from the host, NJU25301 responses will be missed. Multiple reads by the host without an intervening write will return identical byte values.

Table 36 General Command Sequence for I²C-Bus[1]

Sequence Steps	Sent from Host	Response from NJU25301
Operation Code	Opcode	Status Byte Returned: either 0x00, 0x81, or 0x83
Send All Bytes from Command Table	Command Byte 1	Command Byte Count: N
	Command Byte 2	Command Byte Count: N-1
	⋮	⋮
	Command Byte N	Command Byte Count: 1
Return Data	READ	Data Byte 1
	⋮	⋮
	READ	Data Byte N
Termination	NOP	Status Byte: either 0x80, 0x81, or 0x83
Loop Until Read (if Status Byte: 0x83)	NOP	Status Byte: either 0x00 or 0x83

1. Each entry on this table represents a single-byte I²C-bus write to the NJU25301 followed by a single-byte I²C-bus read from the NJU25301 .

The host initiates a command sequence by sending the operation code (opcode) for the command. NJU25301 responds with 0x00 if opcode is accepted or with 0x81 if the opcode is not valid. Next, the host sends command bytes as required by the command. The NJU25301 responds, first, with a value indicating the number of bytes expected and decrements this value after each command byte is received by the host. After sending all the command for writing data to the NJU25301 , the host issues the number of READ requests specified by the command to prompt the NJU25301 to return data (if applicable).

Once the specified number of READ requests (if any) have been issued, the host sends a NOP byte to terminate the sequence and checks the response from NJU25301 :

0x00 – indicates command accepted; NJU25301 is ready to receive next command sequence.
0x81 – indicates error; NJU25301 has received more or fewer READ bytes than specified for the command.
0x83 – indicates busy; NJU25301 is processing current command and is not yet ready for next command.

The host may not initiate a new command sequence while the NJU25301 returns a busy byte (0x83) in response to a NOP from the host[1]. The host must reissue NOP bytes and recheck the NJU25301 response until a status byte of 0x00 is received. This indicates that the current command is accepted and a new command sequence can be initiated, by sending a new opcode.

Table 37 I²C-Bus Example: Sending a Sequence of 3 Commands[1]

Command Sequence	Sent from Host	Response from NJU25301
DELAY_CFG_CMD	0xC6 (Delay Configuration Opcode)	0x00
	0x00 (Command Byte 1)	0x04
	0xEF (Command Byte 2)	0x03
	0x02 (Command Byte 3)	0x02
	0xCF (Command Byte 4)	0x01
	0xFF (NOP)	0x83
- wait loop -	0xFF (NOP)	0x83
	0xFF (NOP)	0x83
	0xFF (NOP)	0x00
UNMUTE_CMD	0xCC (Unmute Opcode)	0x00
	0xFF (NOP)	0x80
SETIO_CMD	0xD1 (Set I/O Opcode)	0x00
	0x01 (Command Byte 1)	0x01
	0xD4 (READ)	0x11 (Data Value of GPIO0)
	0xFF (NOP)	0x80

1. The three commands sent are: Delay Configuration (4 writes, 0 reads), Unmute (0 writes, 0 reads), and Set I/O (1 writes, 1 reads).

1. Execution of a given command may or may not generate a busy response (0x83) from the NJU25301

Command Sequence using SPI Bus

Communication between the host and the NJU25301 is synchronized by byte-stream content. Transitions on the SPI serial strobe (SS) signal do not delineate the beginning or end of a command sequence. The NJU25301 will respond to bytes sent by the host on the following SPI byte cycle (one cycle delay).

Table 38 General Command Sequence for SPI Bus[1]

Sequence Steps	Sent from Host	Response from NJU25301
Operation Code	Opcode	No response is expected until the next SPI transaction
Send All Bytes from Command Table	Command Byte 1	Status Byte Returned: either 0x00, 0x81, or 0x83
	Command Byte 2	Command Byte Count: N
	⋮	Command Byte Count: N-1
	Command Byte N	⋮
Return Data	READ	Command Byte Count: 1
	⋮	Data Byte 1
	READ	⋮
Termination	NOP	Data Byte N
	NOP	Status Byte: either 0x80, 0x81, or 0x83
Loop Until Read (if Status Byte: 0x83)	NOP	Status Byte: either 0x00 or 0x83

1. Each entry on this table represents a single-byte I²C-bus write to the NJU25301 followed by a single-byte I²C-bus read from the NJU25301.

The Communication sequence for SPI format is identical to that described for I²C-bus format except that each response from NJU25301 is delayed by one SPI transaction. One extra NOP byte (independent of busy loop NOPs) is therefore required to complete a command sequence.

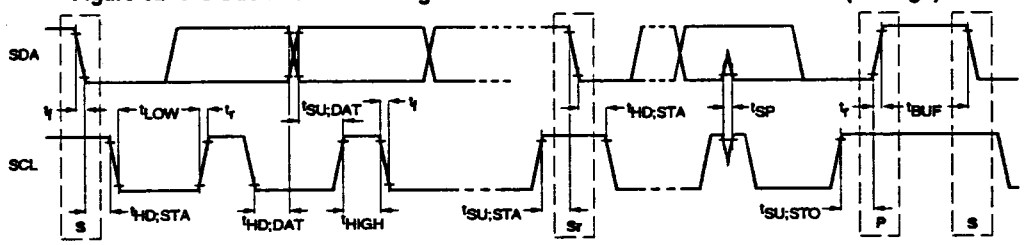
Microcontroller Interface Timing Parameters and Timing Diagram for I²C-Bus Mode

Table 39 I²C-Bus Interface Timing Parameters[1] (V_{DD} = 5V ± 5%, TA = 0°C to +70°C, f_{CLK} = 49.152MHz)

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Setup Time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250	-	100	-	ns
Rise Time of both SDA and SCL signals	t_r	-	1000	-	300	ns
Fall Time of both SDA and SCL signals	t_f	-	300	-	300	ns
Setup Time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs

1. Standard-Mode values referred to V_{IHmin} and V_{ILmax}. LOW level input voltage (V_{IL}) is assumed to have a minimum of -0.5 Volts and a maximum of 1.5 Volts for Standard-Mode. HIGH level input voltage (V_{IH}) is assumed to have a minimum of 3.0 Volts and a maximum of VDD + 0.5 Volts for Standard-Mode.

Figure 52 I²C-Bus Interface Timing for both Standard-Mode and Fast-Mode (SS High)



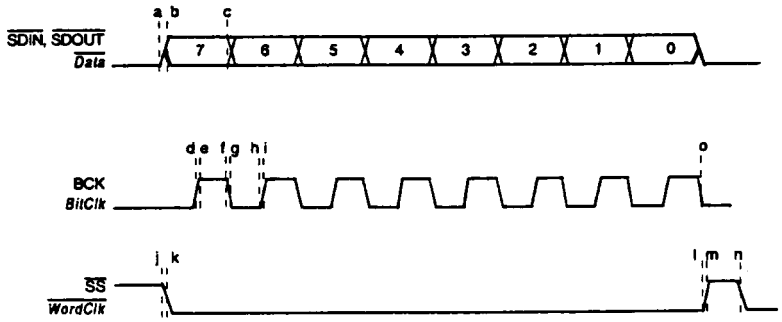
Microcontroller Interface Timing Parameters and Timing Diagram for SPI Bus Mode

Table 40 SPI Bus Timing Parameters[1] (V_{DD} = 5V ± 5%, T_A = 0°C to +70°C, f_{CLK} = 49.152 MHz)

Parameter	Timelines	Symbol	Minimum	Typical	Maximum	Unit
Serial Data Rise Time	a-b	t_{MSDr}			5	ns
Serial Data Fall Time	a-b	t_{MSDf}			5	ns
Serial Data Valid	b-c	t_{MSDv}		40		ns
Serial Clock Rise Time	d-e	t_{MSCr}			5	ns
Serial Clock Fall Time	f-g	t_{MSCf}			5	ns
Serial Clock Asserted	e-f	t_{MSCa}		160		ns
Serial Clock Negated	g-h	t_{MSCn}		160		ns
Serial Clock Cycle Time	e-i	t_{MSCc}		320		ns
Serial Data Input (to DSP) Setup	b-e	t_{MSisu}		20		ns
Serial Data Input (to DSP) Hold	e-c	t_{MSih}		20		ns
Serial Data Output (from DSP) Valid	g-c	t_{MSosu}		20		ns
Serial Data Output (from DSP) Hold	e-c	t_{MSoh}				ns
Serial Strobe Rise Time	j-k	t_{MSSf}			5	ns
Serial Strobe Fall Time	l-m	t_{MSSr}			5	ns
Serial Strobe to Clock Active	k-e	t_{MSSCa}		0		ns
Serial Strobe Active	k-m	t_{MSSa}		5.12		µs
Serial Strobe Negated	m-n	t_{MSSn}		20		ns
Serial Clock to Strobe Negated	o-m	t_{MSCSn}		20		ns

1. All values are assumed V_{DD} is 0 Volts and V_{SS} is 5 Volts.

Figure 53 SPI Bus (Serial Peripheral Interface) Timing (SS Low)



Serial Audio Data Timing Parameters and Timing Diagrams

Table 41 Serial Data Input Timing Parameters (V_{DD} = 5V ± 5%, T_A = 0°C to +70°C, f_{CLK} = 49.152 MHz)

Parameter	Symbol	Minimum	Maximum	Unit
BCKI Period		160	-	ns
L Pulse Width	t_{SIL}	80	-	ns
H Pulse Width	t_{SIH}	80	-	ns
BCKI to LRI Time	t_{SLI}	40	-	ns
LRI to SCKI Time	t_{LSI}	40	-	ns
Data Setup Time	t_{DS}	40	-	ns
Data Hold Time	t_{DH}	40	-	ns

Figure 54 Serial Audio Data Input Timing

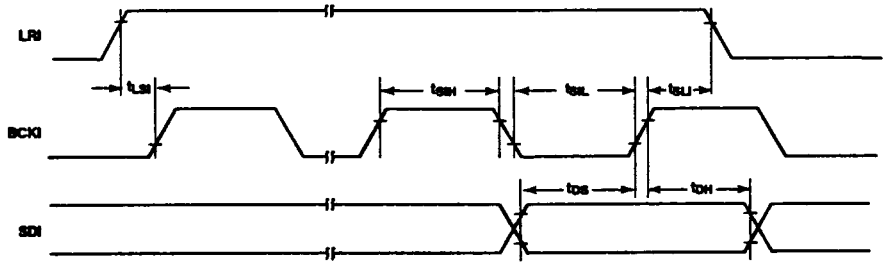
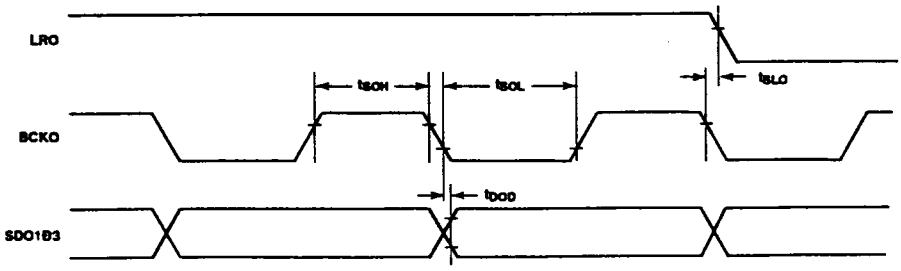


Table 42 Serial Audio Data Output Timing Parameters (V_{DD} = 5V ± 5%, T_A = 0°C to +70°C, f_{CLK} = 49.152 MHz, C_L: LRO, BCKO, SDO = 5 pF)

Parameter	Symbol	Minimum	Maximum	Unit
BCKO Period		160	-	ns
L Pulse Width	t_{SOL}	80	-	ns
H Pulse Width	t_{SOH}	80	-	ns
BCKO to LRO Time	t_{SLO}	-	10	ns
Data Output Delay	t_{DOD}	-	10	ns

Figure 55 Serial Audio Data Output Timing



Electrical Specifications

Table 43 Absolute Maximum Ratings[1] (V_{SS} = 0 V)

Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage (T_A = 25°C)	V_{DD}	-0.3	7	V
Input, Output Pin Voltage (T_A= 25°C)	V_x	-0.3	V_{DD} + 0.3	V
Operating Temperature	T_{OPR}	0	70	°C
Storage Temperature	T_{STG}	-65	150	°C

1. Absolute maximum ratings are stress ratings only, and functional operation beyond these limits is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

Table 44 Electrical Characteristics (T_A = 0°C to +70°C)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Unit
Operating Voltage	V_{DD}	V_{DD} pins	4.75		5.25	V
Operating Current	I_{DD}	f_{osc} = 49.152 MHz	-	300	-	mA
High Level Input Voltage	V_{IH}		0.80 V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}		V_{SS}		0.10 V_{DD}	V
High Level Input Current	I_{IH}	V_{IN} = V_{DD}	-		10	µA
Low Level Input Current	I_{IL}	V_{IN} = V_{SS}	-		10	µA
High Level Output Voltage	V_{OH}	I_{OH} = 2 mA	V_{DD} - 1.0		-	V
Low Level Output Voltage	V_{OL}	I_{OH} = 2 mA	-		0.5	V
Input Capacitance	C_{IN}		-	5	10	pF
Clock Frequency	f_{OSC}		-	49.152	52	MHz
Ext. System Clock Duty Cycle	r_{EC}		45		55	%

Figure 56 Plastic QFP-80 Dimensions

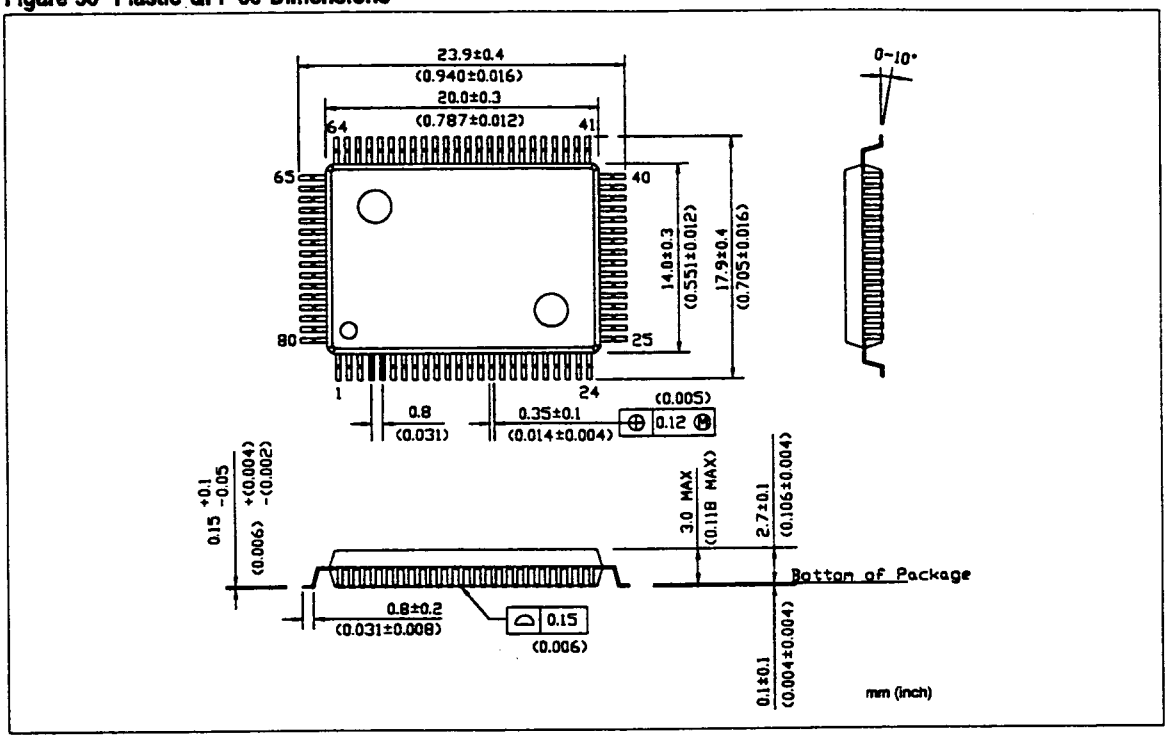
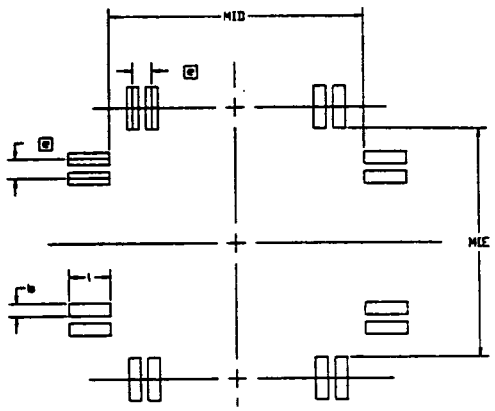


Figure 57 QFP-80 Solder Pads



Plastic QFP-80 Solder Pad Dimensions

	PKG SIZE	b	l	e	MID	MIE
Millimeters	20 x 14	0.50	2.00	0.80	20.4	14.4
Inches	0.787 x 0.551	0.020	0.079	0.031	0.803	0.567