EDO DRAM Board 512Mbyte (32M x 144-Bit) organized as 4Banks of 8Mx144, 4K Ref., 3.3V, ECC Part No. HCPMEM-512

GENERAL DESCRIPTION

The HCPMEM-512 is a 32M x 144 bit Dynamic RAM high-density module, organized with four banks of 8M x 144 bits. The HCPMEM-512 consists of thirty six 8M x 16, 4K refresh DRAMs in TSOPII packages, five 16 bit buffer/drivers and one PLD. The PLD controls the WRITE Enable and Output Enable signals to the DRAMS. Connectors on each side of the module allow two memories to mated together.

FEATURES

- VTTL compatible inputs and outputs
- 10 bit Column addressing
- Single 3.3V +/- .3 power supply
- Buffered Address and Control lines
- Mezzanine stackingAccess time: 60 ns (max)
- Power dissipation
  * Active: 7.5 W (max)
  * Standby : 400 mW (max) (CMOS interface)
- EDO page mode capability
- CAS-before-RAS refreshRefresh cycles
- FR4-PCB design
- Application : Sun Microsystem CP 1400/1500

• The used device is HM5113165F-6

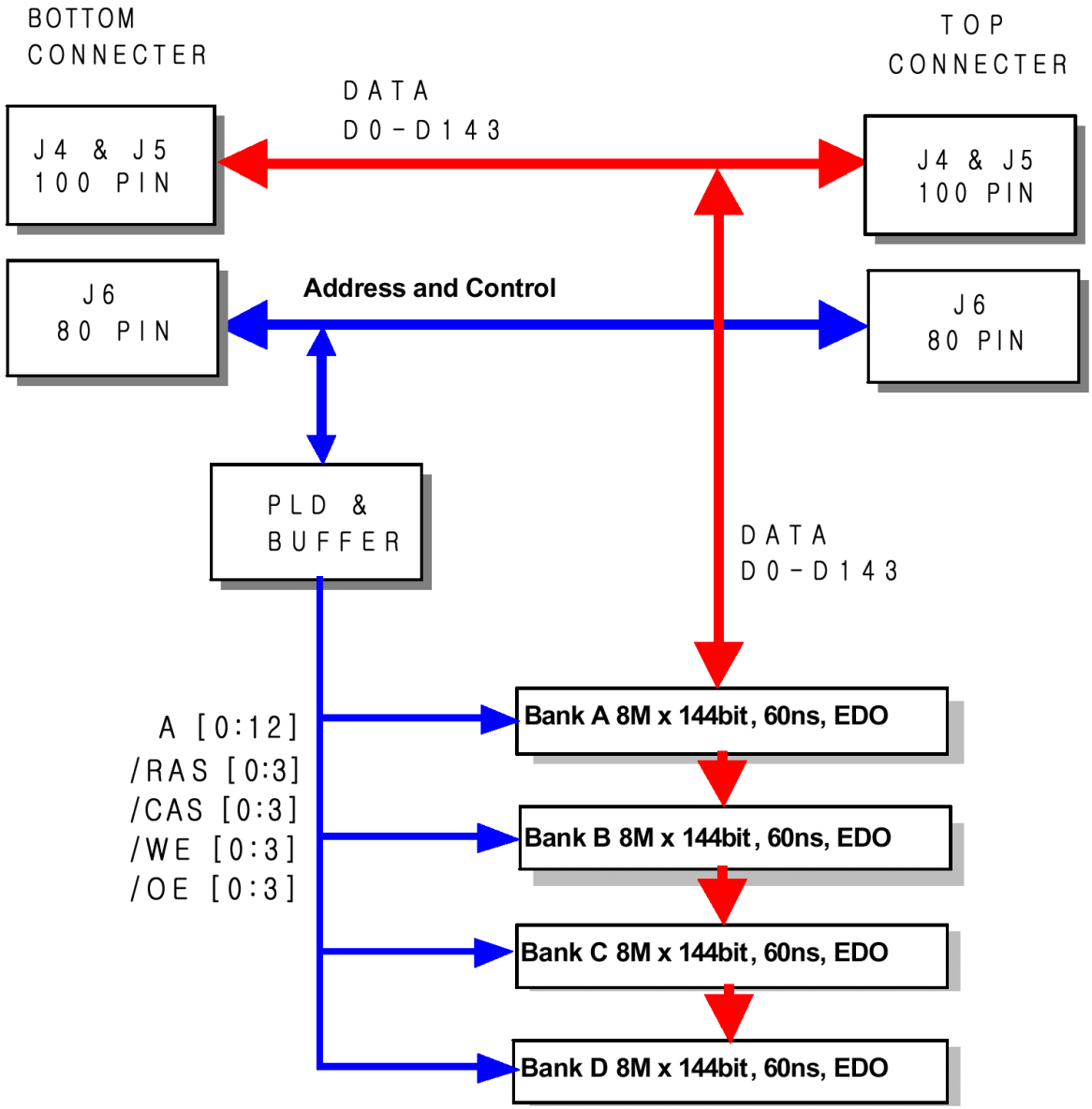
Pin Configuration (TOP)

J1				J2				J3			
1	GND	51	GND	1	GND	51	GND	1	GND	41	GND
2	D0	52	D36	2	D72	52	D108	2	A0	42	/RASB1_L
3	D1	53	D37	3	D73	53	D109	3	A1	43	EN U1 3
4	D2	54	D38	4	D74	54	D110	4	VDD	44	VDD
5	VDD	55	VDD	5	VDD	55	VDD	5	A2	45	/RAST1_L
6	D3	56	D39	6	D75	56	D111	6	A3	46	GND
7	D4	57	D40	7	D76	57	D112	7	GND	47	GND
8	D5	58	D41	8	D77	58	D113	8	A4	48	/CAS0(0)_
9	GND	59	GND	9	GND	59	GND	9	A5	49	/CAS0(1)_
10	D6	60	D42	10	D78	60	D114	10	VDD	50	VDD
11	D7	61	D43	11	D79	61	D115	11	A6	51	GND
12	D8	62	D44	12	D80	62	D116	12	A7	52	/CAS1(0)_
13	VDD	63	VDD	13	VDD	63	VDD	13	GND	53	/CAS1(1)_
14	D9	64	D45	14	D81	64	D117	14	A8	54	VDD
15	D10	65	D46	15	D82	65	D118	15	A9	55	VDD
16	D11	66	D47	16	D83	66	D119	16	VDD	56	NC
17	GND	67	GND	17	GND	67	GND	17	A10	57	GND
18	D12	68	D48	18	D84	68	D120	18	A11	58	/WE0_L
19	D13	69	D49	19	D85	69	D121	19	GND	59	VDD
20	D14	70	D50	20	D86	70	D122	20	A12	60	VDD
21	VDD	71	VDD	21	VDD	71	VDD	21	GND	61	VDD
22	D15	72	D51	22	D87	72	D123	22	GND	62	XOE_L
23	D16	73	D52	23	D88	73	D124	23	/RASB2_L	63	GND
24	D17	74	D53	24	D89	74	D125	24	NC	64	GND
25	GND	75	GND	25	VDD	75	GND	25	VDD	65	XOEA_L
26	GND	76	GND	26	VDD	76	GND	26	/RAST2_L	66	50_60NS_RA
27	D18	77	D54	27	D90	77	D126	27	NC	67	VDD
28	D19	78	D55	28	D91	78	D127	28	GND	68	VDD
29	D20	79	D56	29	D92	79	D128	29	/RAB3_L	69	NC
30	VDD	80	VDD	30	VDD	80	VDD	30	VDD	70	GND
31	D21	81	D57	31	D93	81	D129	31	VDD	71	TDI
32	D22	82	D58	32	D94	82	D130	32	/RAST3_L	72	TDO
33	D23	83	D59	33	D95	83	D131	33	GND	73	VDD
34	GND	84	GND	34	GND	84	GND	34	GND	74	TMS1
35	D24	85	D60	35	D96	85	D132	35	/RASB0_L	75	VDD
36	D25	86	D61	36	D97	86	D133	36	NC	76	NC
37	D26	87	D62	37	D98	87	D134	37	VDD	77	GND
38	VDD	88	VDD	38	VDD	88	VDD	38	/RAST0_L	78	TCLK1
39	D27	89	D63	39	D99	89	D135	39	NC	79	GND
40	D28	90	D64	40	D100	90	D136	40	GND	80	GND
41	D29	91	D65	41	D101	91	D137				
42	GND	92	GND	42	GND	92	GND				
43	D30	93	D66	43	D102	93	D138				
44	D31	94	D67	44	D103	94	D139				
45	D32	95	D68	45	D104	95	D140				
46	VDD	96	VDD	46	VDD	96	VDD				
47	D33	97	D69	47	D105	97	D141				
48	D34	98	D70	48	D106	98	D142				
49	D35	99	D71	49	D107	99	D143				
50	GND	100	GND	50	GND	100	GND				

Pin Configuration (BOTTOM)

J4				J5				J6			
1	GND	51	GND	1	GND	51	GND	1	GND	41	GND
2	D0	52	D36	2	D72	52	D108	2	A0	42	/RASB3_L
3	D1	53	D37	3	D73	53	D109	3	A1	43	EN U1 3
4	D2	54	D38	4	D74	54	D110	4	VDD	44	VDD
5	VDD	55	VDD	5	VDD	55	VDD	5	A2	45	/RAST3_L
6	D3	56	D39	6	D75	56	D111	6	A3	46	GND
7	D4	57	D40	7	D76	57	D112	7	GND	47	GND
8	D5	58	D41	8	D77	58	D113	8	A4	48	/CAS0(0)_
9	GND	59	GND	9	GND	59	GND	9	A5	49	/CAS0(1)_
10	D6	60	D42	10	D78	60	D114	10	VDD	50	VDD
11	D7	61	D43	11	D79	61	D115	11	A6	51	GND
12	D8	62	D44	12	D80	62	D116	12	A7	52	/CAS1(0)_
13	VDD	63	VDD	13	VDD	63	VDD	13	GND	53	/CAS1(1)_
14	D9	64	D45	14	D81	64	D117	14	A8	54	VDD
15	D10	65	D46	15	D82	65	D118	15	A9	55	VDD
16	D11	66	D47	16	D83	66	D119	16	VDD	56	NC
17	GND	67	GND	17	GND	67	GND	17	A10	57	GND
18	D12	68	D48	18	D84	68	D120	18	A11	58	/WE0_L
19	D13	69	D49	19	D85	69	D121	19	GND	59	VDD
20	D14	70	D50	20	D86	70	D122	20	A12	60	VDD
21	VDD	71	VDD	21	VDD	71	VDD	21	GND	61	VDD
22	D15	72	D51	22	D87	72	D123	22	GND	62	XOE_L
23	D16	73	D52	23	D88	73	D124	23	/RASB0_L	63	GND
24	D17	74	D53	24	D89	74	D125	24	NC	64	GND
25	GND	75	GND	25	VDD	75	GND	25	VDD	65	XOEA_L
26	GND	76	GND	26	VDD	76	GND	26	/RAST0_L	66	50_60NS_RA
27	D18	77	D54	27	D90	77	D126	27	NC	67	VDD
28	D19	78	D55	28	D91	78	D127	28	GND	68	VDD
29	D20	79	D56	29	D92	79	D128	29	/RAB1_L	69	NC
30	VDD	80	VDD	30	VDD	80	VDD	30	VDD	70	GND
31	D21	81	D57	31	D93	81	D129	31	VDD	71	TDI
32	D22	82	D58	32	D94	82	D130	32	/RAST1_L	72	TDO
33	D23	83	D59	33	D95	83	D131	33	GND	73	VDD
34	GND	84	GND	34	GND	84	GND	34	GND	74	TMS1
35	D24	85	D60	35	D96	85	D132	35	/RASB2_L	75	VDD
36	D25	86	D61	36	D97	86	D133	36	NC	76	NC
37	D26	87	D62	37	D98	87	D134	37	VDD	77	GND
38	VDD	88	VDD	38	VDD	88	VDD	38	/RAST2_L	78	TCLK1
39	D27	89	D63	39	D99	89	D135	39	NC	79	GND
40	D28	90	D64	40	D100	90	D136	40	GND	80	GND
41	D29	91	D65	41	D101	91	D137				
42	GND	92	GND	42	GND	92	GND				
43	D30	93	D66	43	D102	93	D138				
44	D31	94	D67	44	D103	94	D139				
45	D32	95	D68	45	D104	95	D140				
46	VDD	96	VDD	46	VDD	96	VDD				
47	D33	97	D69	47	D105	97	D141				
48	D34	98	D70	48	D106	98	D142				
49	D35	99	D71	49	D107	99	D143				
50	GND	100	GND	50	GND	100	GND				

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5 to V_{CC} + 0.5 (≤ 4.6 V (max))	V
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	7.5	W
Storage temperature	Tstg	–55 to +125	°C

Notes :
Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to VSS = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
	V_{SS}	0	0	0	V	2
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	0	—	70	˚C	

Notes :
1. All voltage referred to VSS .
2. The supply voltage with all VCC pins must be on the same level. The supply voltage with all VSS pins must be on the same level.

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Test conditions
Operating current*1, *2	I_{CC1}	—	2270	mA	t_{RC} = min
Standby current	I_{CC2}	—	250	mA	TTL interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IH} Dout = High-Z
		—	120	mA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	450	mA	t_{RC} = min
EDO page mode current*1, *3	I_{CC7}	—	2000	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{HPC} = t_{HPC} min
Input leakage current	I_{LI}	–5	180	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V
Output leakage current	I_{LO}	–5	180	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	V	Low Iout = 2 mA

Notes :
1. Icc depends on output load condition when the device is selected. Icc max is specified at the output open condition.
2. Address can be changed once or less while RAS = VIL.
3. Measured with one sequential address change per EDO cycle, tHPC.
4. VIH ≥ VCC – 0.2V, 0 V ≤ VIL ≤ 0.2 V.

CAPACITANCE (TA = 25°C, V CC = 3.3 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	—	252	pF	1
Input capacitance (Clocks)	C_{I2}	—	—	252	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	—	252	pF	1, 2

Notes :
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. /RAS, /UCAS AND /LCAS = VIH TO DISABLE DOUT.

AC Characteristics (Ta = 0 to +70°C, V = 3.3 V ± 0.3 V, V = 0 V)

Test Conditions
•Input rise and fall time: 2 ns
•Input pulse levels: VIL = 0 V, VIH = 3.0 V
•Input timing reference levels: 0.8 V, 2.0 V
•Output timing reference levels: 0.8 V, 2.0 V
•Output load: 1 TTL gate + CL (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	104	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	ns	26
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	ns	
Row address setup time	t_{ASR}	0	—	ns	
Row address hold time	t_{RAH}	10	—	ns	
Column address setup time	t_{ASC}	0	—	ns	26
Column address hold time	t_{CAH}	10	—	ns	26
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	45	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	12	30	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	ns	26
$\overline{OE}$ to Din delay time	t_{OED}	15	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	ns	7

Read Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	15	ns	9, 10, 17
Access time from address	t_{AA}	—	30	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	15	ns	9
Read command setup time	t_{RCS}	0	—	ns	26
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	ns	12, 26
Read command hold time from $\overline{RAS}$	t_{RCHR}	60	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	18	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	ns	
Output data hold time	t_{OH}	3	—	ns	21
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	ns	13, 21
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	ns	21
Output buffer turn-off to $\overline{RAS}$	t_{OFR}	—	15	ns	13, 21
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	15	ns	13
$\overline{WE}$ to Din delay time	t_{WED}	15	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	15	—	ns	

Write Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	ns	14, 26
Write command hold time	t_{WCH}	10	—	ns	26
Write command pulse width	t_{WP}	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	ns	26
Data-in setup time	t_{DS}	0	—	ns	15, 26
Data-in hold time	t_{DH}	10	—	ns	15, 26

Read-Modify-Write Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	140	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	79	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	49	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	ns	

Refresh Cycle

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	ns	26
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	ns	26
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	ns	26

EDO Page Mode Cycle

Parameter	Symbol	Min	Max	Unit	Notes
EDO page mode cycle time	t_{HPC}	25	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	ns	9, 17, 26
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	ns	9, 22
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	ns	
Write pulse width during $\overline{CAS}$ precharge	t_{WPE}	10	—	ns	
$\overline{OE}$ precharge time	t_{OEP}	10	—	ns	

EDO Page Mode Read-Modify-Write Cycle

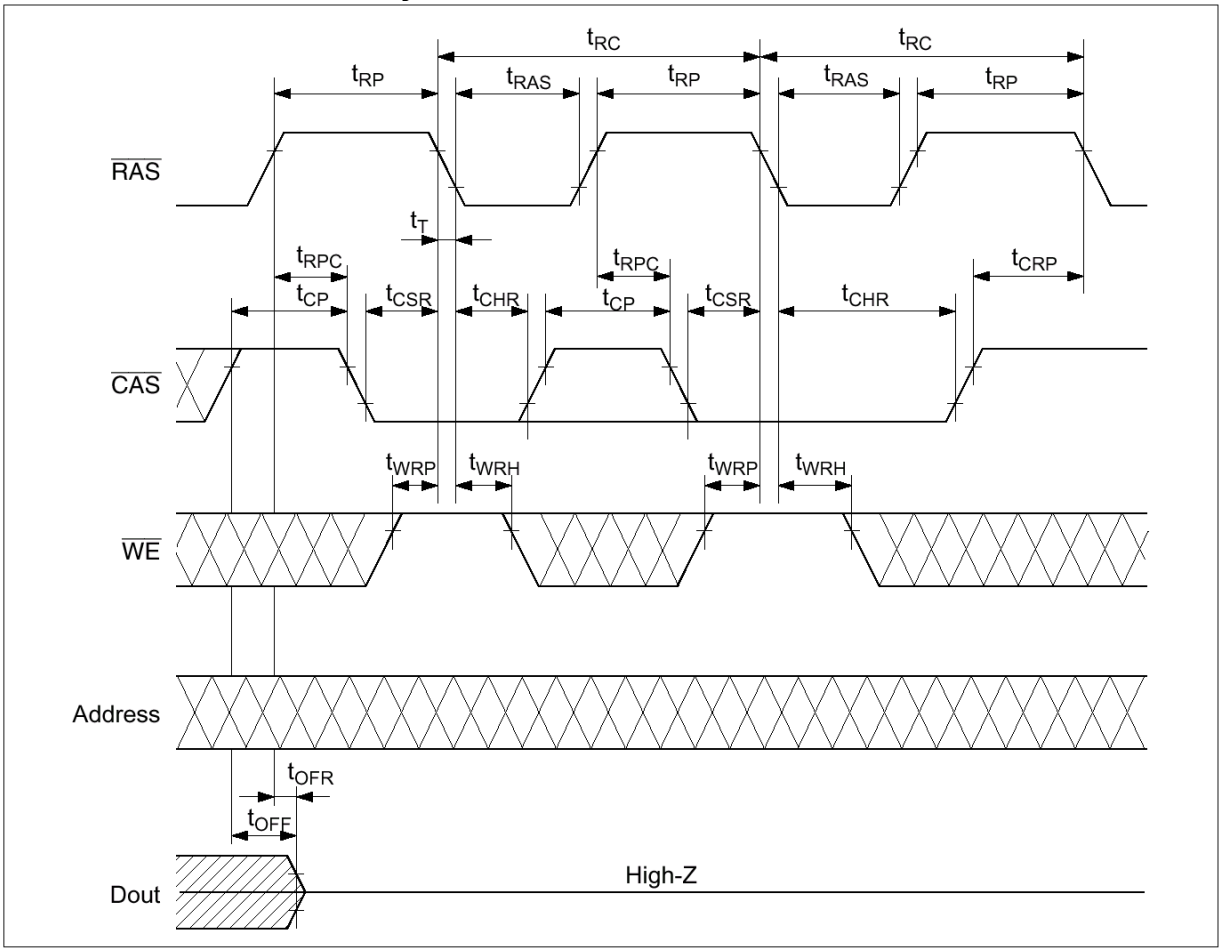
Parameter	Symbol	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	t_{HPRWC}	68	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	54	—	ns	14, 26

Notes:

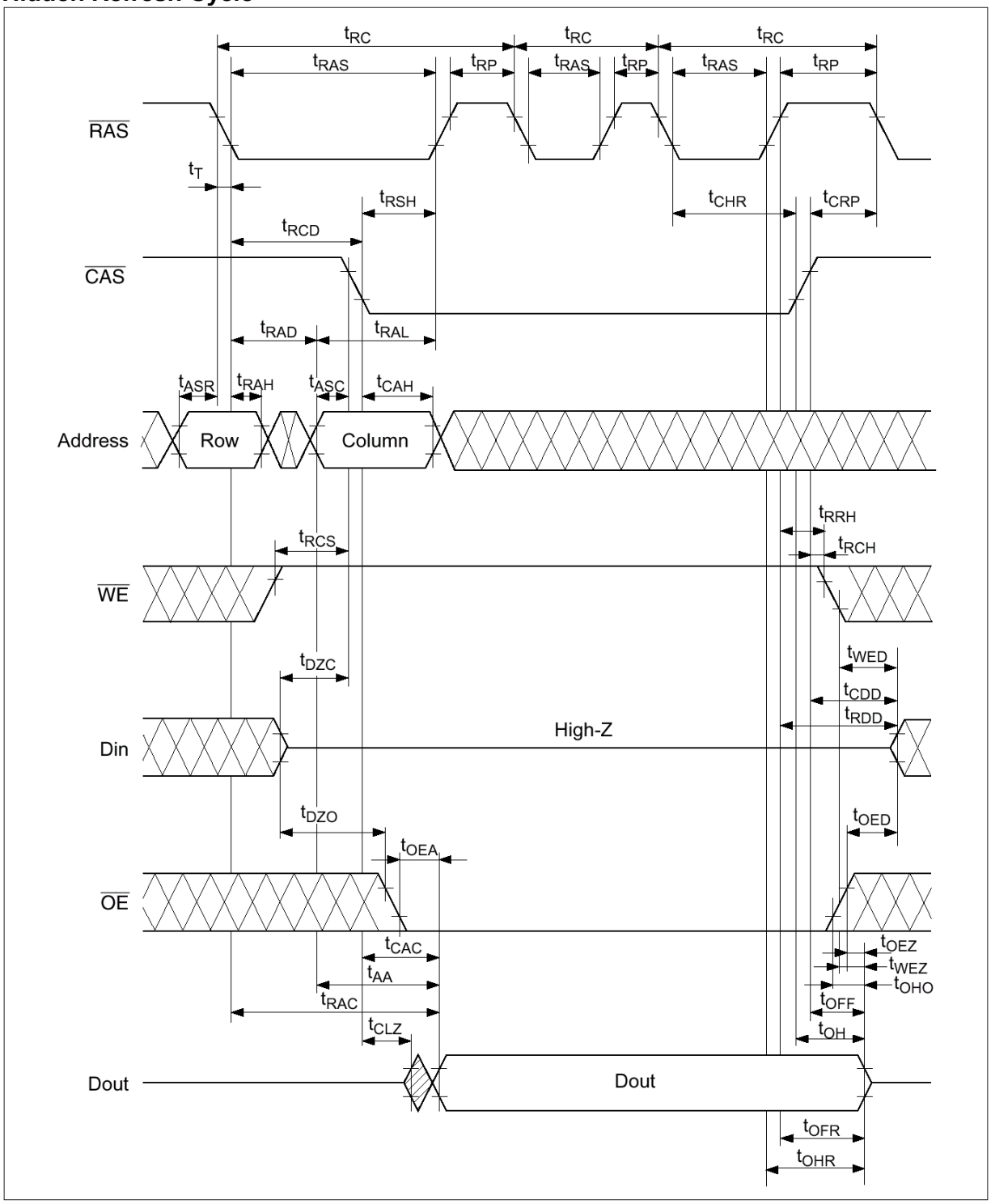
1. AC measurements assume tT = 2 ns.
2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing /RAS-only refresh or /CAS -before-/RAS refresh).
3. Operation with the tRCD (max) limit insures that tRAC (max) can be met, tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, than the access time is controlled exclusively by tCAC .
4. Operation with the tRAD (max) limit insures that tRAC (max) can be met, tRAD (max) is specified as a reference point only; if tRAD is greater than the specified tRAD (max) limit, then access time is controlled exclusively by tAA .
5. Either tOED or tCDD must be satisfied.
6. Either tDZO or tDZC must be satisfied.
7. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH (min) and VIL (max).
8. Assumes that tRCD ≤ tRCD (max) and tRAD ≤ tRAD (max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that tRCD ≥ tRCD (max) and tRCD + tCAC (max) ≥ tRAD + tAA (max).
11. Assumes that tRAD ≥ tRAD (max) and tRCD + tCAC (max) ≥ tRAD + tAA (max).
12. Either tRCH or tRRH must be satisfied for a read cycles.
13. tOFF (max), tOEZ (max), tWEZ (max) and tOFR (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. tWCS , tRWD , tCWD , tAWD and tCPW are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if tWCS ≥ tWCS (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tRWD ≥ tRWD (min), tCWD ≥ tCWD (min), and tAWD ≥ tAWD (min), or tCWD ≥ tCWD (min), tAWD ≥ tAWD (min) and tCPW ≥ tCPW (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. tDS and tDH are referred to /UCAS and /LCAS leading edge in early write cycles and to /WE leading edge in delayed write or read-modify-write cycles.
16. tRASP defines /RAS pulse width in EDO page mode cycles.
17. Access time is determined by the longest among tAA , tCAC and tCPA .
18. In delayed write or read-modify-write cycles, /OE must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large Vcc /Vss line noise, which causes to degrade VIH min/VIL max level.
20. tHPC (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode /RAS cycle (EDO page mode mix cycle (1), (2)), minimum value of /CAS cycle (tCAS + tCP + 2 tT) becomes greater than the specified tHPC (min) value. The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of /RAS and /CAS . Hold time and turn off time are specified by the timing specifications of later rising edge of /RAS and /CAS between tOHR and tOH and between tOFR and tOFF .
22. tDOH defines the time at which the output level go cross. VOL = 0.8 V, VOH = 2.0 V of output timing reference level.
23. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64 ms period on the condition a and b below.
    a. Enter self refresh mode within 15.6 μs after either burst refresh or distributed refresh at qual interval to all refresh addresses are completed.
    b. Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6μs after exiting from self refresh mode.
24. In case of entering from /RAS -only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 23.
25. At tRASS > 100 μs, self refresh mode is activated, and not activated at tRASS < 10 μs. It is undefined within the range of 10 μs ≤ tRASS ≤ 100 μs. For tRASS ≥ 10 μs, it is necessary to satisfy tRPS .
26. tASC , tCAH , tRCS , tWCS , tWCH , tCSR , tRPC , tCRP , tCHR , tRCH , tCPA , tCPW , tCWL , tDH , tDS , tCHS and tCP are determined by each of /UCAS /LACS independently.
27. XXX : H or L (H: VIH (min) ≤ VIN ≤ VIH (max), L: VIL (min) ≤ VIN ≤ VIL (max))
    /////// : Invalid Dout
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied VIH or VIL .

TIMING DIAGRAMS

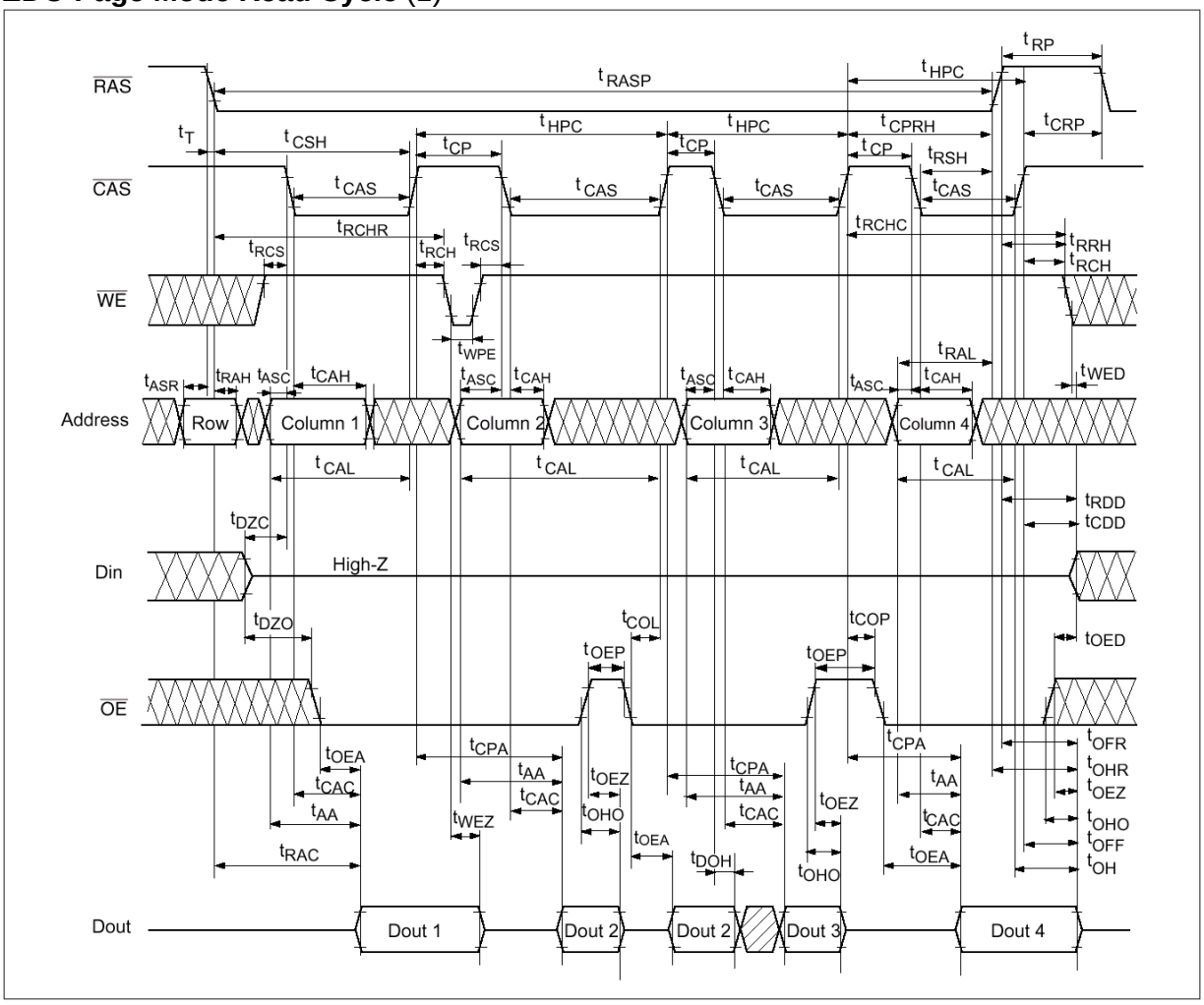
CAS -Before-RAS Refresh Cycle



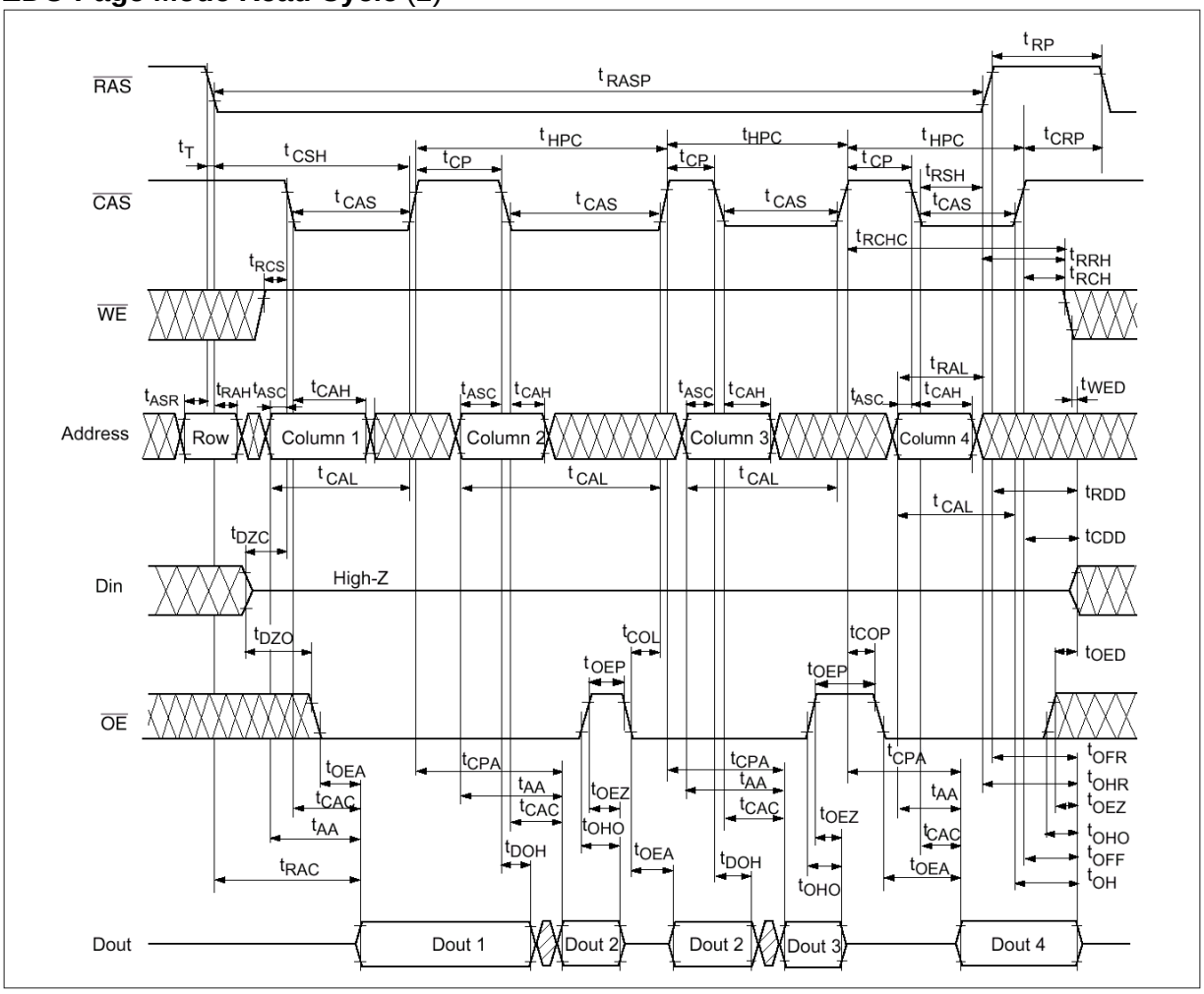
Hidden Refresh Cycle



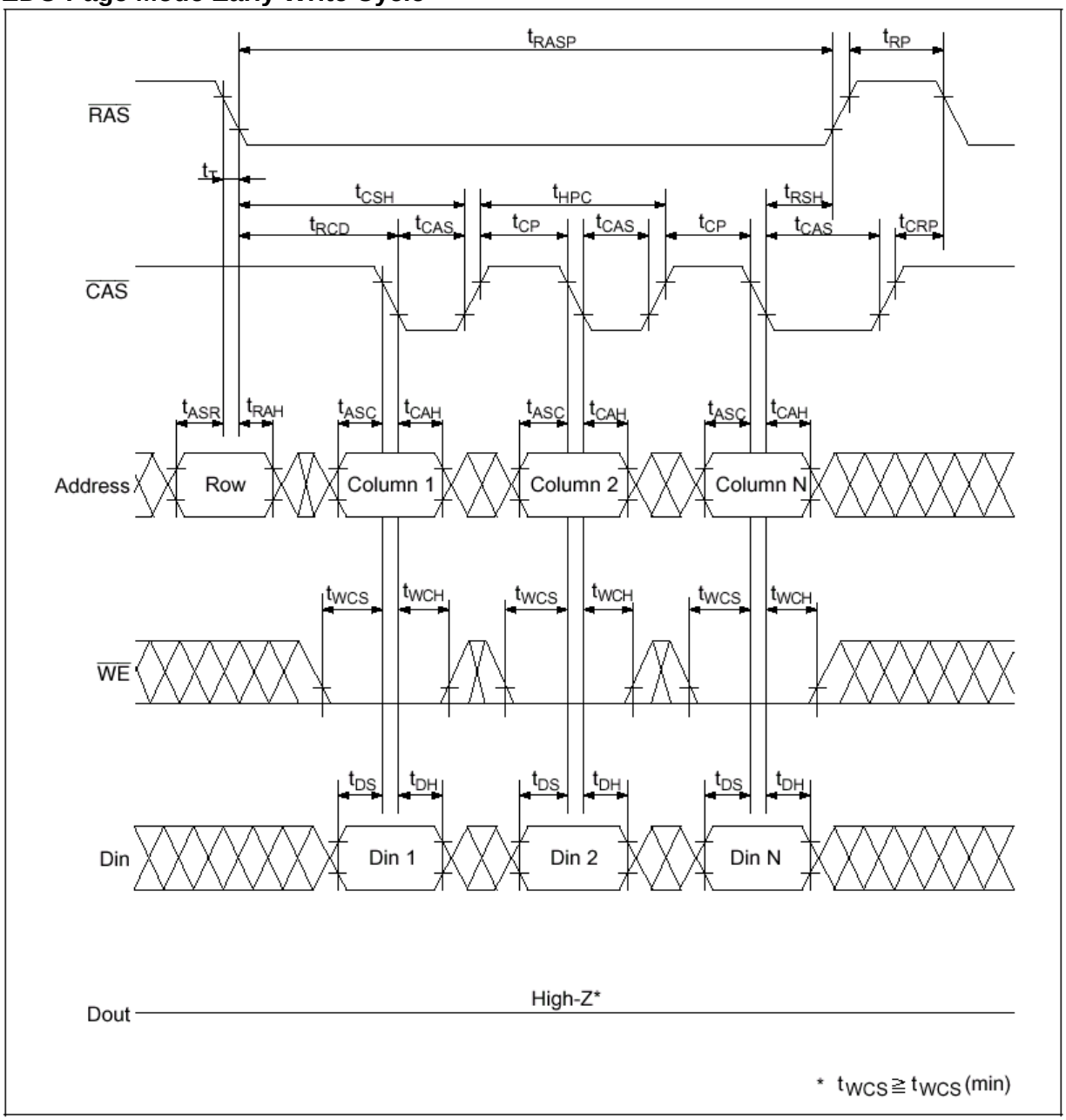
EDO Page Mode Read Cycle (1)



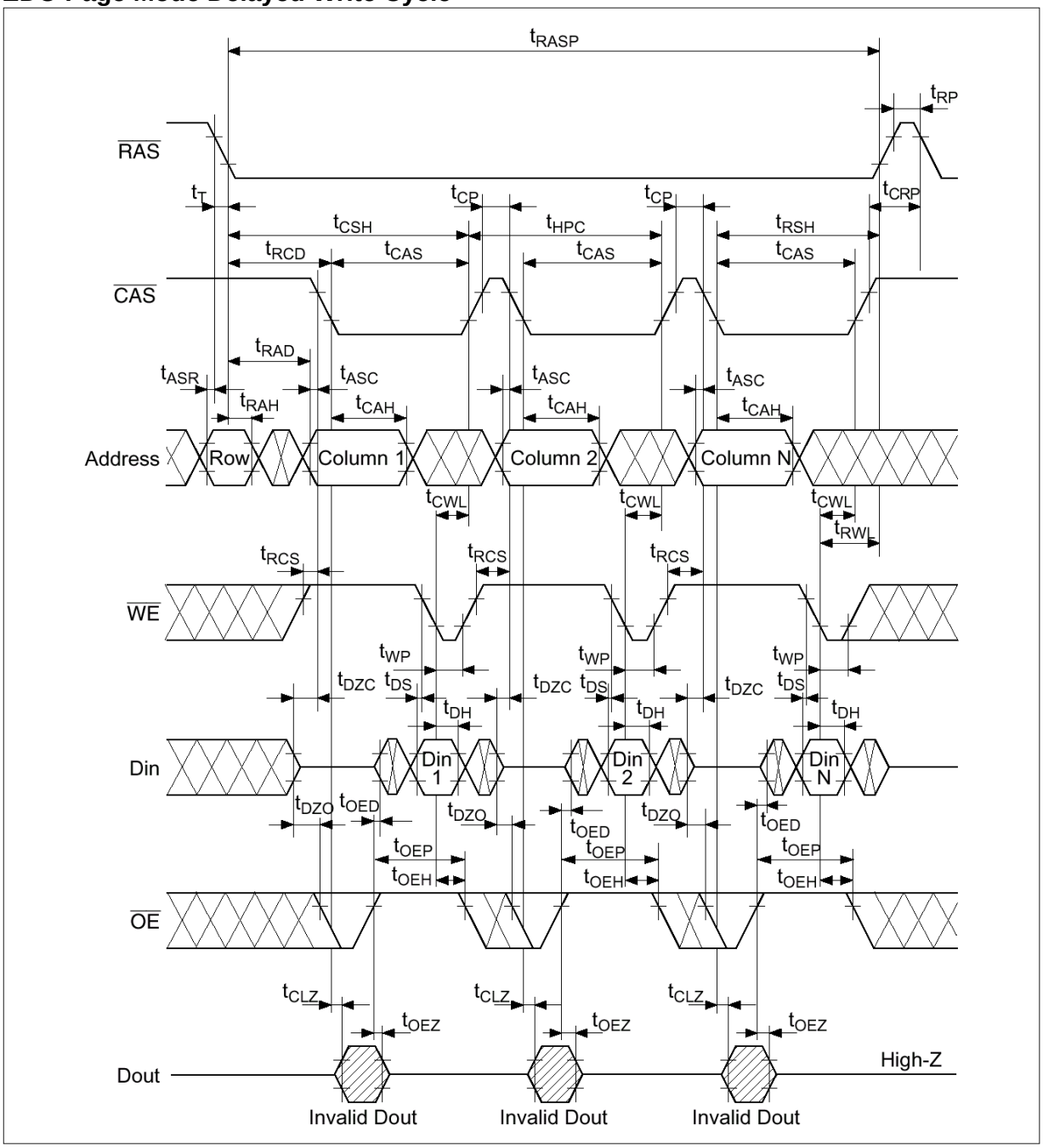
EDO Page Mode Read Cycle (2)



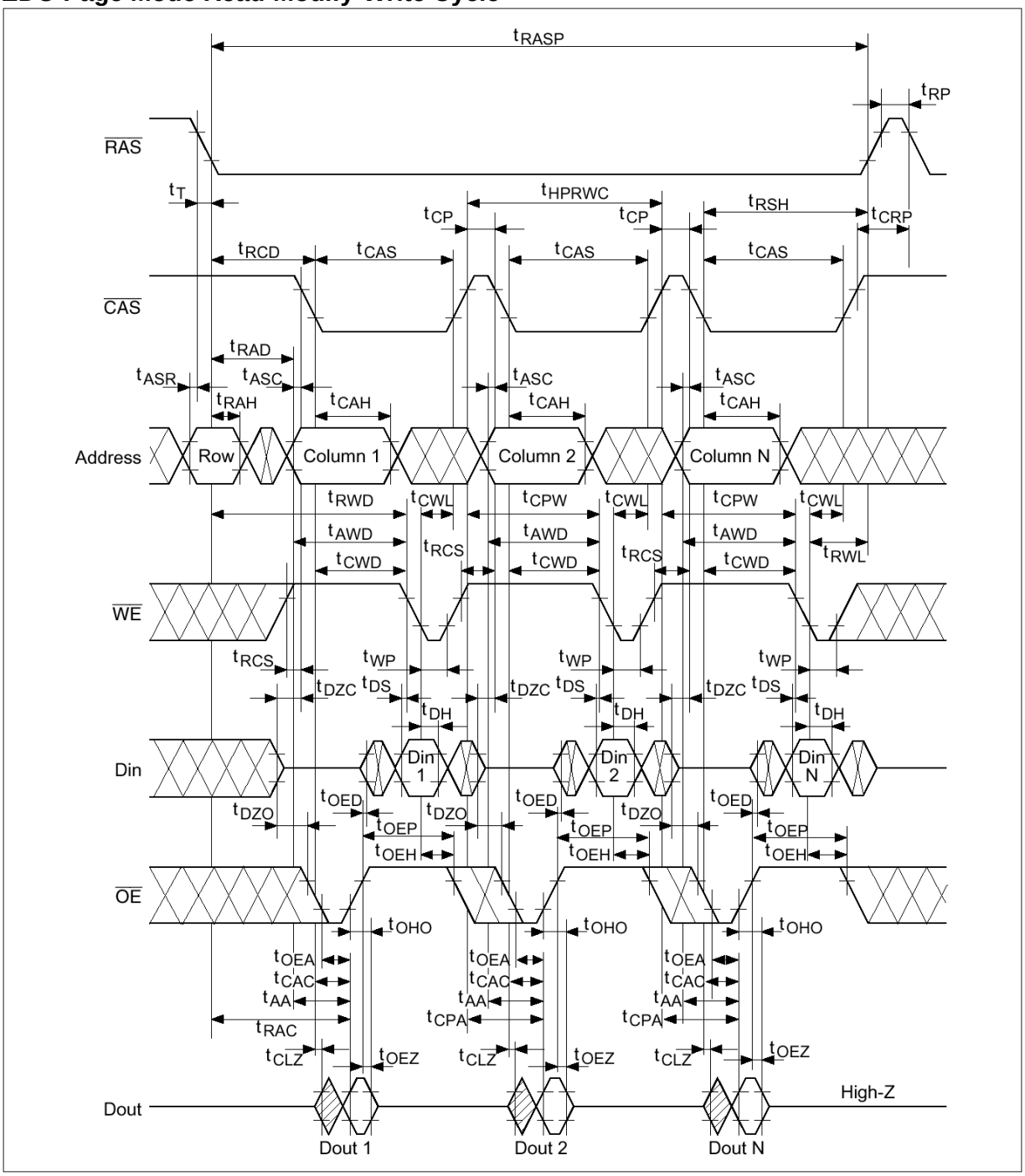
EDO Page Mode Early Write Cycle



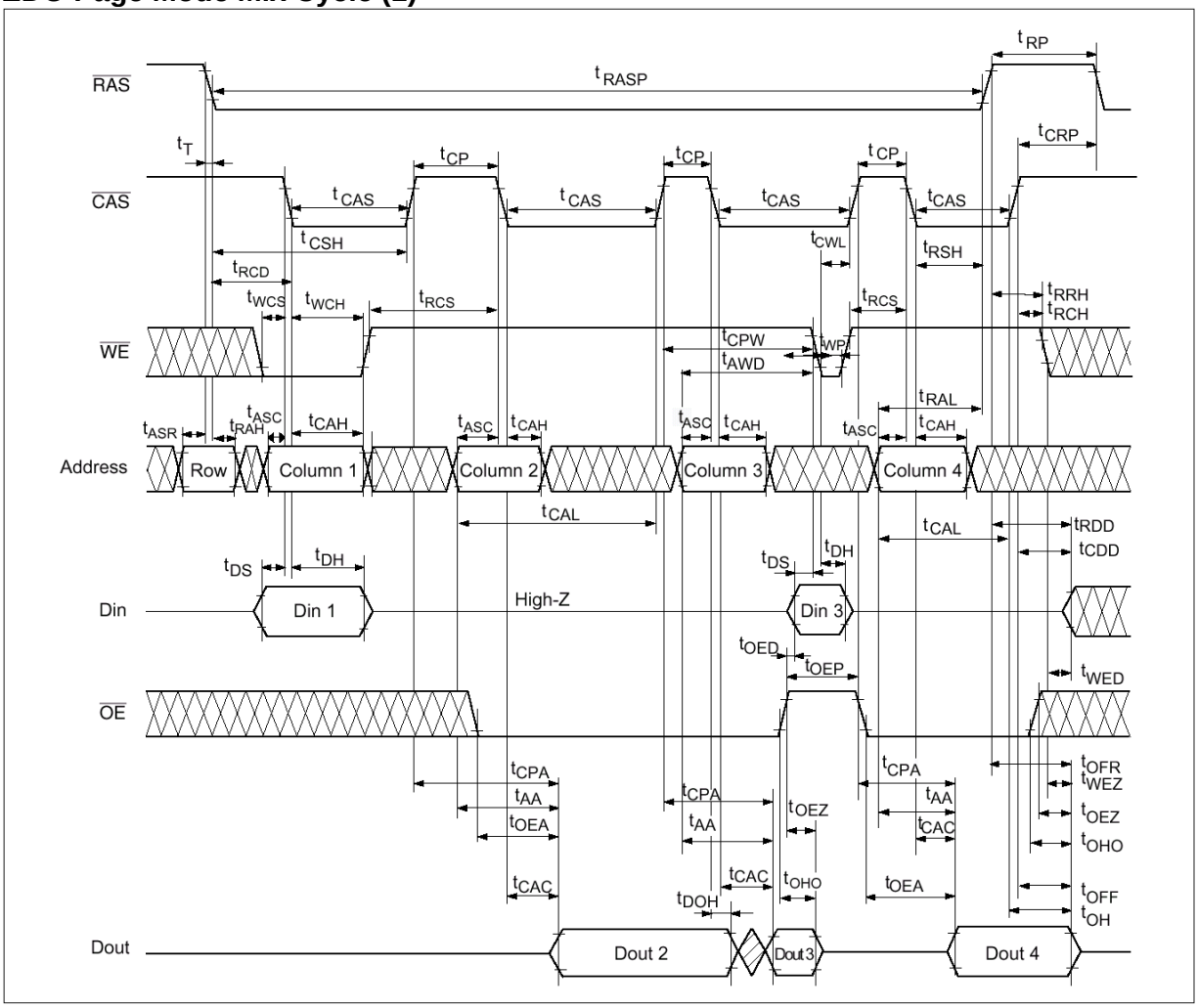
EDO Page Mode Delayed Write Cycle*[18]



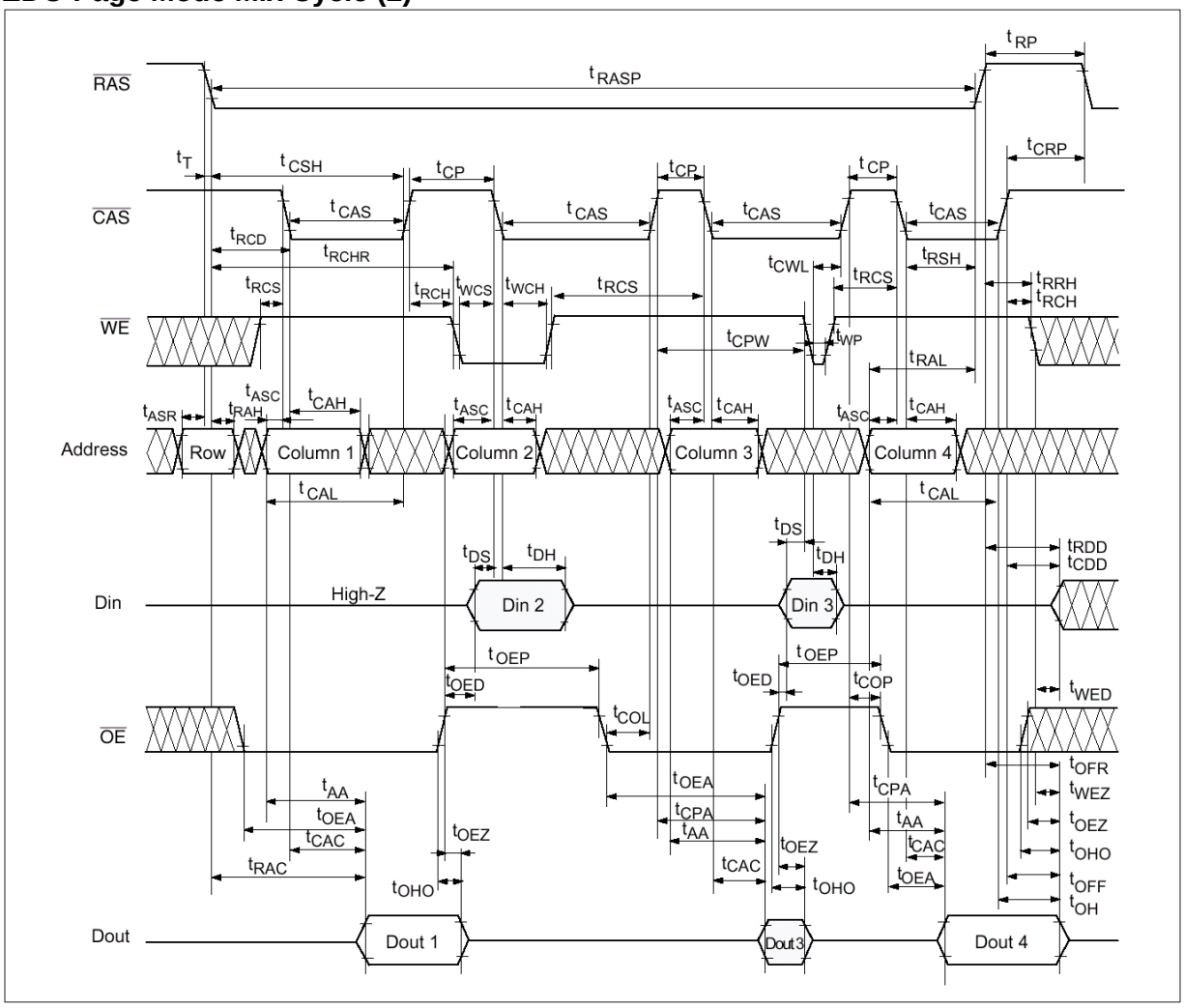
EDO Page Mode Read-Modify-Write Cycle*[18]



EDO Page Mode Mix Cycle (1) * [20]



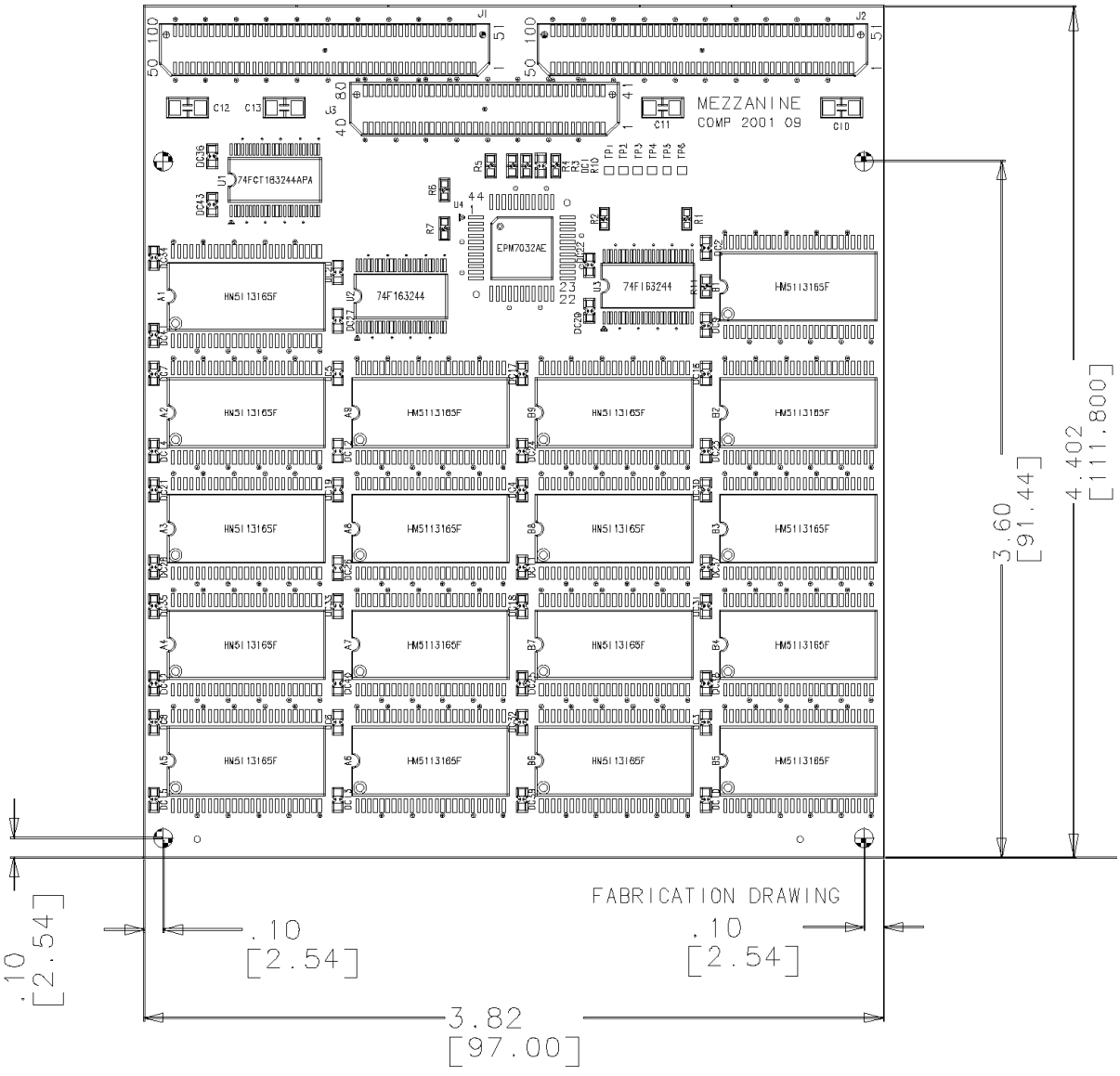
EDO Page Mode Mix Cycle (2)*[20]



PACKAGING INFORMATION

Unit : Mil

[Milimeter]



ORDERING INFORMATION

Part Number	Density	Org.	Package	Mode	Ref	Vcc	SPEED
HCPMEM-512	512MByte	32MX 144bit	Mezzanine	EDO	4K	3.3V	60ns