LXT380/1

Frequently Asked Questions

January 2001

Order Number: 249181-001

As of January 15, 2001, this document replaces the Level One document known as *LXT380/LXT381FAQs*.

Frequently Asked Questions

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1.0 Questions and Answers

1.1 Microprocessor Interface

Q1. In Motorola Mode, can I connect $\overline{CS}$ and $\overline{DS}$ together ?

Yes. Our timing specifications allow you to connect these signals together. There is no delay specified between $\overline{CS}$ and $\overline{DS}$.

Q2. I'm using the LXT380 in the non-multiplexed Motorola mode. What should I do with the address strobe signal (AS) ?

In non multiplexed Motorola mode there is no need for an address strobe signal. Therefore should be pulled High.

Q3. In non-multiplexed Intel mode what do I do with the ALE signal?

In non multiplexed Intel mode there is no need for an address latch enable signal. Therefore ALE should be pulled High.

Q4. What is the maximum bus speed the LXT380 can operate at?

The designer should refer to the LXT380 data sheet for timing specifications. Comparing the minimum signal widths with the corresponding microprocessor bus signals will determine if the devices can be connected directly. For extremely fast microprocessors, the LXT380 supports wait-state generation through the $\overline{ACK}$ / RDY (Motorola/Intel) pin.

Q5. How to handle an Interrupt in the Interrupt Service Routine ?

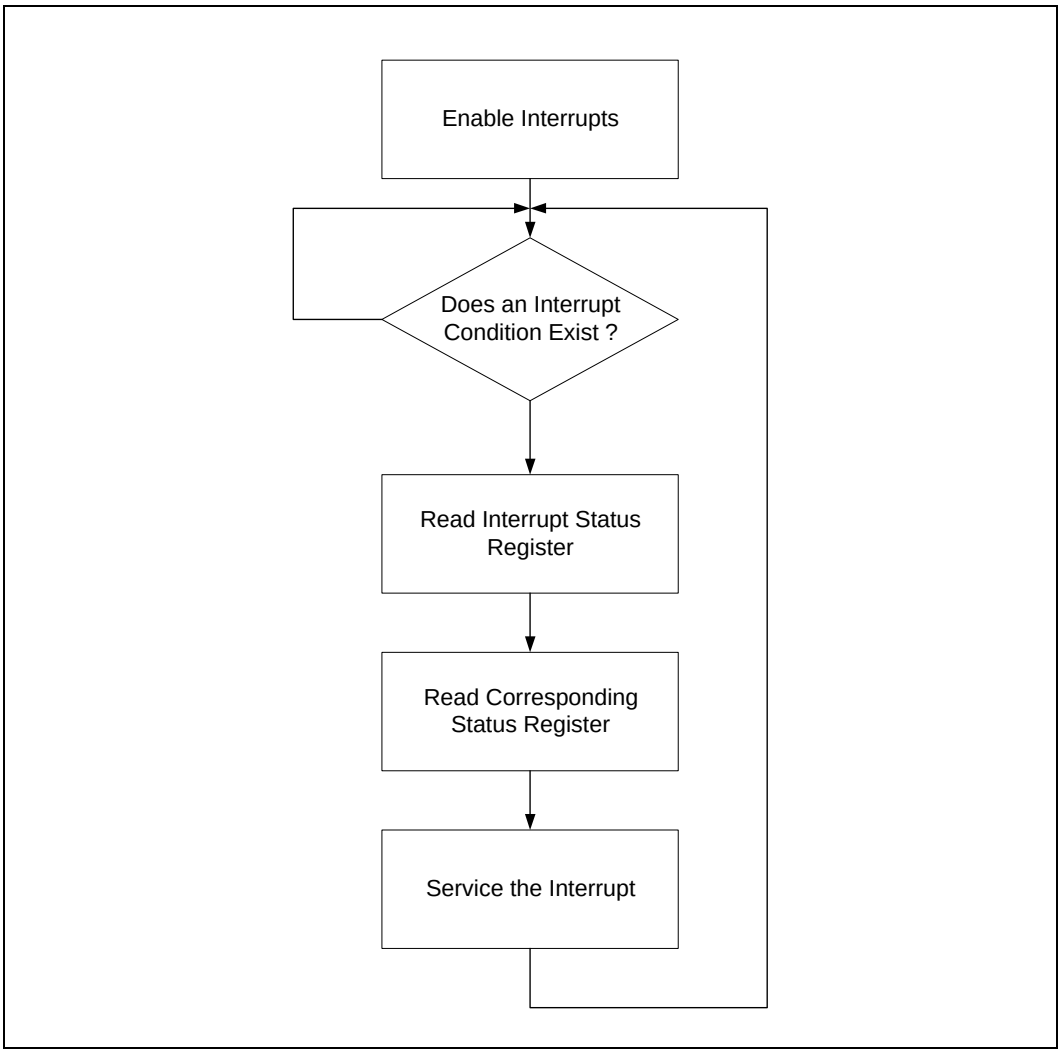
In the LXT380 there are three kinds of registers associated with interrupt handling: interrupt enable registers, interrupt status registers and status registers.

Writing a "1" into an interrupt enable register will enable the corresponding interrupt for the respective channel. For example, if LIE = FFh (LOS Interrupt Register) then loss of signal interrupts will be enabled for all eight channels.

The interrupt status registers signal that an interrupt was caused by a change in status in the corresponding channel. For example, if an interrupt is triggered by a loss of signal in channel 0, the associated interrupt service routine will start by reading the interrupt status registers in order to identify the cause for the interrupt. In this example you should read LIS = 01h (LOS Interrupt Status Register).

After reading the interrupt status register the software will read the associated status register to monitor the current status and take appropriate action. If in the example above, the loss of signal condition is still valid at the time the register is read then LOS = 01h (LOS Status Monitor Register). By reading the status register the interrupt condition will be cleared.

The following picture illustrates the interrupt handling process:



1.2 Line Interface

Q6. Can I use the same transformer (1:2) for the transmit and receive side?

Yes. The receiver sensitivity of the LXT380/1 is high enough to accommodate the loss introduced by a 2:1 step-down transformer. Our lab tests indicate that this configuration will reduce the maximum cable sensitivity by approximately 2dB @ 1.024MHz. This means a maximum cable attenuation of 10dB which is well above the required 6dB minimum for ITU-T G.703 compliance.

Note that the receive terminating resistors (RR in the data sheet) should be scaled appropriately to 9.31ohm and 15.0 ohm for coaxial cable and twisted pair cable respectively.

Q7. What transformers should I use with the LXT380/1?

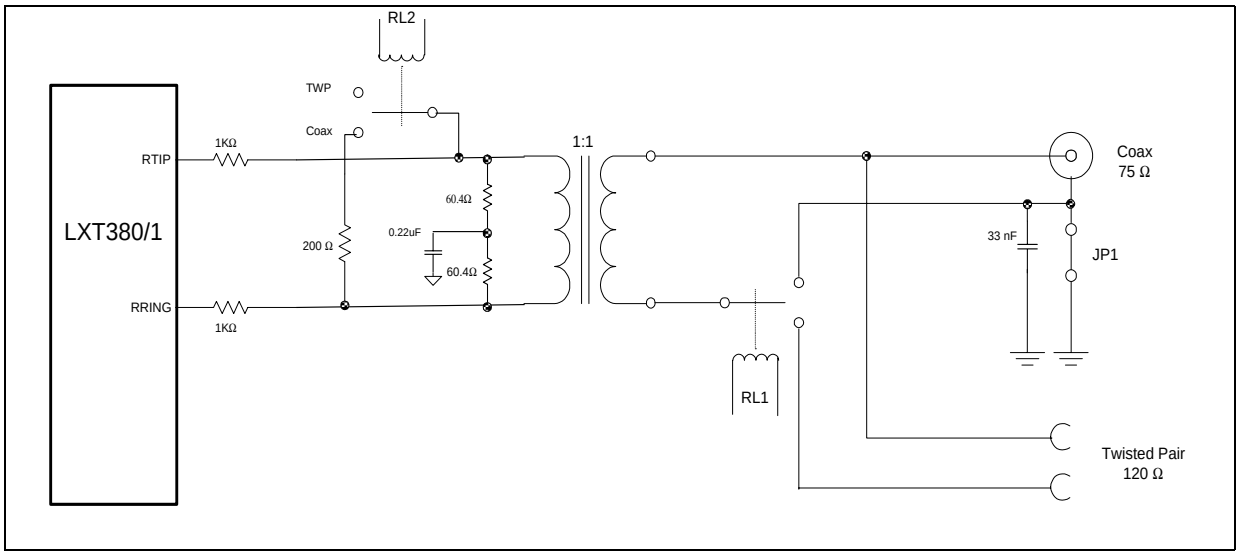
Transformer specifications for the LXT380/1 are listed in the data sheet (LXT380 see Table 40 and LXT381 see Table 10). Any transformer that meets these specifications can be used with the LXT380/1. The following table contains examples of transformers recommended by Intel:

Manufacturer	Part Number	Channels	Turns Ratio	SMD	Temperature Range
Halo Electronics	TG49 - LVL1NX	4Tx, 4Rx	1CT:2 Tx 2CT:1 Rx	Yes	EXT Temp
	TG49 - 1505NX	4Tx, 4Rx	1CT:2 Tx 2CT:1 Rx	Yes	EXT Temp
	TG48 - 1205N1	1Tx, 1Rx	1CT:2CT Tx 1:1 Rx	Yes	STD Temp
	TG29 - 1205NX	4Tx, 4Rx	1:2 Tx 2CT:1 Rx	Yes	STD Temp
	TG26 - 1205N1	1Tx, 1Rx	1CT:2CT Tx 2CT:1CT Rx	Yes	STD Temp
	TD26 - 1505D	1Tx, 1Rx	1:2CT Tx 1:2CT Rx	No	STD Temp
Pulse Engineering	T1124 / T1114	4Tx, 4Rx	1CT:2 TX 2CT:1 Rx	Yes	T1124 - STD Temp T1114 - EXT Temp
	T1066 / T1106	4Tx, 4Rx	1:2 Tx 1:2CT Rx	Yes	T1066 - STD Temp T1106 - EXT Temp
	T1068 / T1168	4Tx, 4Rx	1:2CT Tx 1:1CT Rx	Yes	T1068 - STD Temp T1168 - EXT Temp
	T1065 / T1105	4Tx, 4Rx	1:2CT Tx 1:2CT Rx	Yes	T1065 - STD Temp T1105 - EXT Temp
	PE - 68678	1Tx, 1Rx	1CT:1CT Rx 1CT:2CT Tx	Yes	STD Temp
	PE - 68877	1Tx, 1Rx	1CT:1CT Rx 1CT:2CT Tx	Yes	EXT Temp
	PE - 68841	1Tx, 1Rx	1CT:2CT Rx 1CT:2CT Tx	Yes	EXT Temp
	PE - 68861	1Tx, 1Rx	1CT:2CT Rx 1CT:2CT Tx	Yes	STD Temp
Bell Fuse	S553-6500-55	4Tx, 4Rx	1CT:2 Tx 2CT:1 Rx	Yes	EXT Temp
	S553-6500-37	4Tx, 4Rx	1CT:2 Tx 2CT:1 Rx	Yes	EXT Temp
	S553-6500-10	1Tx, 1Rx	1CT:2CT Tx 1CT:2CT Rx	Yes	STD Temp
PCA Electronics	EPA3557S	4Tx, 4Rx	1CT:2 Tx 2CT:1 Rx	Yes	STD Temp

Q8. How can I support E1 75/120 ohm operation in the same design?

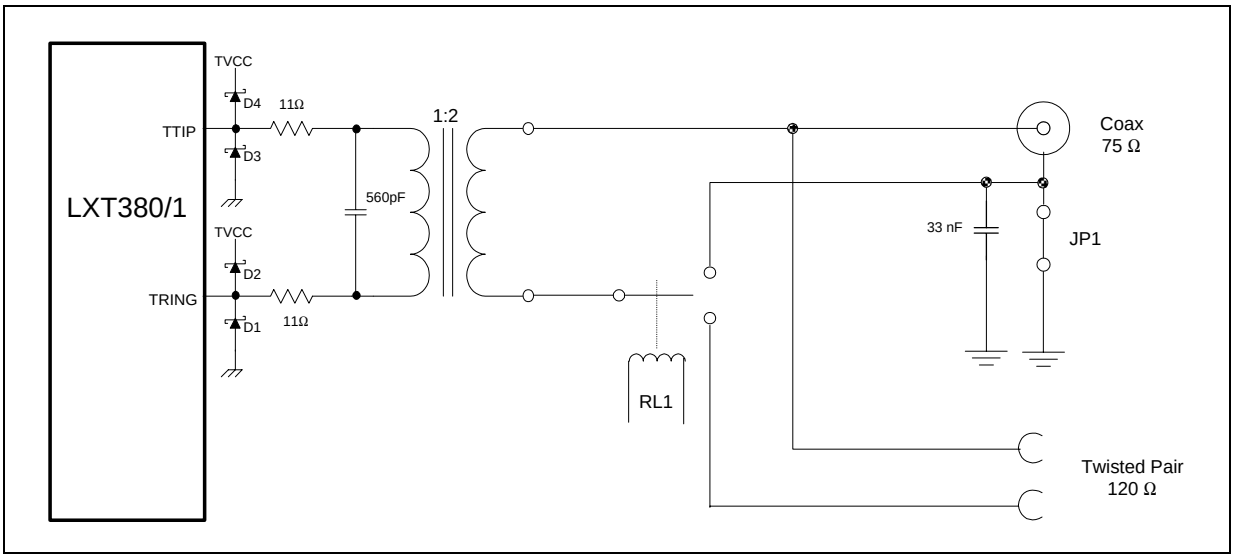
The following figure suggests a configuration for the receive side. The relay RL2 selects the appropriate terminating impedance (75 or 120 ohm). Relay RL1 is needed to isolate the balanced interface from the earth connection of the coaxial interface. If the connection through JP1 is made, connecting both signals together would ground (unbalance) one of the balanced output signals. The connection to earth through JP1 is provided in accordance to G.703. This connection should only be removed when earth currents interfere with normal operation.

Figure 1. Receive Interface



The following figure suggests a configuration for the transmit side. Since the LXT380/1 uses the same resistor/transformer combination for both 75 ohm and 120 ohm the design is simplified. The connection to earth through JP1 is recommended for G.703 compliance.

Figure 2. Transmit Interface



Q9. Does the LXT380/1 meet G.703 Annex B protection requirements?

Yes, when used with the recommended transmit and receive interface described in the data sheet. The recommended interface includes protection elements that ensure G.703 Annex B compliance at a minimum cost. Refer to Application Note 106 for more details.

Q10. I'm only using 7 channels in my design. What should I do to the TIP and RING signals in the unused channel?

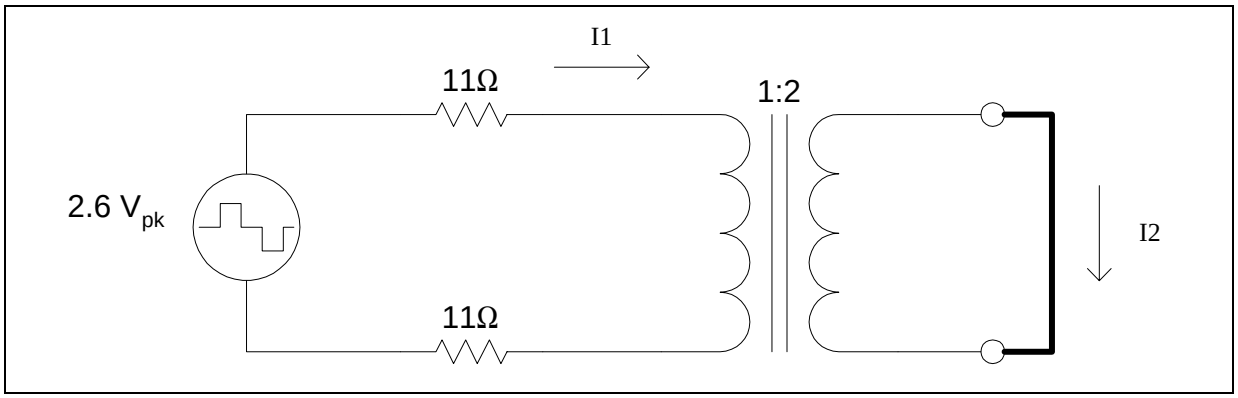
The unused TTIP and TRING pins should be left open. The unused RTIP and RRING pins should be connected together through a capacitor or 1kW resistor to avoid noise coupling into the device. Do not connect RTIP/RRING to ground since these signals have a 2.0 V biasing voltage.

Q11. How should I adjust the 560 pF capacitor in the transmit interface?

The main purpose of the transmit 560 pF capacitor is to slightly increase the high frequency transmit return loss. Typical applications already have a substantial amount of parasitic capacitance. Sources of parasitic capacitance are the protection elements, common mode chokes, long PCB traces and connectors. Too much capacitance might cause some slight ringing in the output pulse. In these cases, the designer is advised to reduce the capacitor value. However, for most designs, a 560pF capacitor provides good results.

Q12. Does the LXT380/1 meet BS5450 50 mArms output short-circuit current limitation?

Yes. The following figure represents a simplified Thevenin equivalent for the LXT380/1 transmit interface with a short-circuit at the output:



I1 can be approximated as:

I1pk = 2.6 / (2x11) = 118 mA pk

The worst-case short-circuit current occurs when an all ones is being transmitted. For an E1 all ones signal, the rms current can be calculated as:

I1rms = I1pk / ÷2 = 84 mA rms

I2rms = I1rms / 2 = 42 mA rms < 50 mA rms

Therefore, the worst case short-circuit current will be always less than 50 mA rms. Note, for simplicity, these calculations ignore the effect of the transformer winding resistance and driver output impedance. The actual short circuit current should be even lower than calculated.

Q13. How do I tri-state the LXT380/1 output drivers?

The output driver tri-state capability is useful in designing protection systems without external relays. For details on implementing redundancy applications without relays please refer to Application Note AN119.

The LXT380/1 offers two distinct methods for tri-stating the output drivers.

Hold the corresponding channel's TCLK Low for at least 8ms. This method allows driver tri-stating on a per-channel basis.

Set the OE pin Low to tri-state all the output drivers. The OE pin in the LXT380/1 allows fast switching between redundant and working boards without having to individually tri-state every output driver.

Q14. What are the layout recommendations for the analog interface?

Here's a list of general guidelines for the analog T1/E1 interfaces:

- Place decoupling capacitors very close to the corresponding TVCC/VCC pins.
- Avoid crossing transmit and receive signals to minimize cross-talk.
- Avoid routing digital signals near analog signals (TIP/RING) and receiver inputs.
- Provide ample power and ground planes.

- Route differential pairs like RTIP/RRING and TTIP/TRING close together. Make sure the trace length for differential signals is about the same.
- Don't extend the ground plane beyond the line side of the transmit and receive transformers. Ground plane noise could be coupled into the line signals increasing RF emissions.
- Minimize trace lengths connecting the LIU to transformers and connectors.
- When using surge protection elements in the line side of the transformer such as TVS, place them as close as possible to the disturbance source, i.e., the connector.

1.3 Digital (Framer) Interface

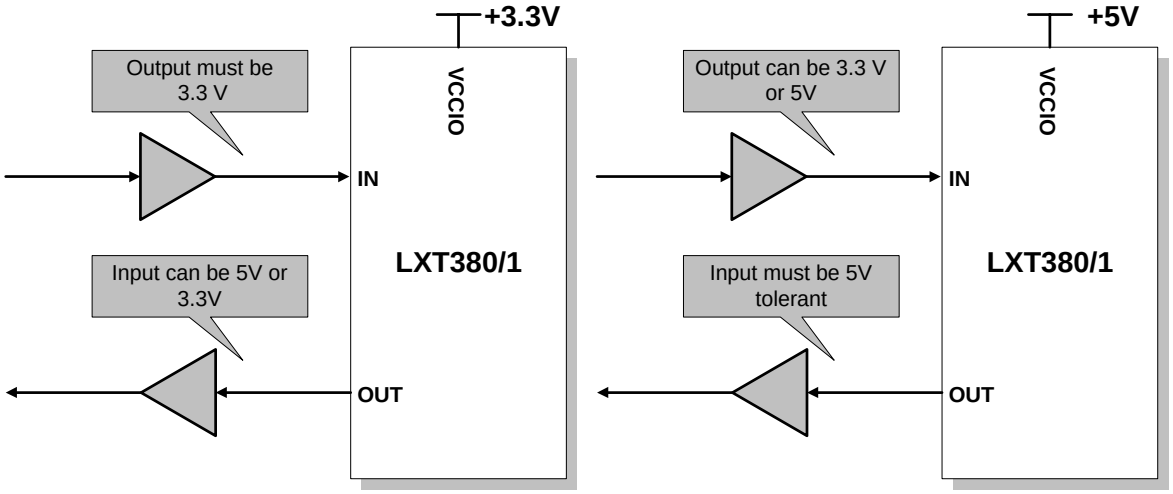
Q15. How do RPOS/RNEG behave upon loss of signal (LOS) ?

RPOS and RNEG will output the data content as seen at the line input. If LOS is caused by a total signal failure (all zeros), RPOS/RNEG will be Low all the time. However, if there are occasional 1's, they will be seen at RPOS/RNEG. This allows the framer or mapper connected to the LXT380 to perform LOS detection and LOS reset based on the RPOS/RNEG output.

Q16. How do I interface the LXT380/1 with 5V logic?

The following figure contrasts the 3.3V and 5.0V I/O configurations. 5V I/O capability is accomplished by connecting the 5V power supply to the VCCIO pins. Note that the power to the internal logic (VCC pins) and output drivers (TVCC pins) must still come from a 3.3V supply.

The outputs from the LXT380/1 will be 5V when VCCIO pins = 5V. Therefore, the devices that interface with the LXT380/1 must be 5V tolerant. Naturally, 5V devices have 5V tolerant inputs.



Q17. What is the difference between Unipolar and Bipolar mode operation?

Bipolar and unipolar modes are two different ways for an LIU to interface to a framer or back end ASIC. The following is from the receive perspective. The transmit perspective is similar.

The T1 or E1 data (zeros and ones) is coded as alternate positive and negative pulses for signaling logic 1's on the line. Zeros are coded as a zero voltage.

In bipolar mode, two data lines, (RPOS and RNEG) plus a clock line (RCLK) connect the LIU to the framer. A logic "1" on RPOS tells the framer that a positive pulse was detected on the line. A logic "1" on RNEG tells the framer that a negative pulse was detected on the line. In bipolar mode, it's the framer's responsibility to decode the sequence of positive and negative pulses into a sequence of logic zeros and ones. This is done by the AMI or B8ZS/HDB3 decoders inside the framer.

In unipolar mode, only one data line (RDATA) plus a clock (RCLK) connect the LIU to the framer. The sequence of positive and negative pulses is decoded inside the LIU. The resulting sequence of zeros and ones is output on TDATA. In unipolar mode, the AMI or B8ZS/HDB3 decoders are automatically enabled inside the LIU.

Typically, the LIU also provides a BPV (bipolar violation) output when in unipolar mode. This output indicates the reception of positive / negative pulse sequences that do not respect the selected encoding scheme (AMI, B8ZS/HDB3). Noise or cross talk on the line may trigger such violations of the encoding scheme. Some framers provide a BPV input that will drive internal BPV counters for performance monitoring purposes.

In bipolar mode, the BPVs are detected inside the framer based on the positive/negative pulse sequence in RPOS/RNEG.

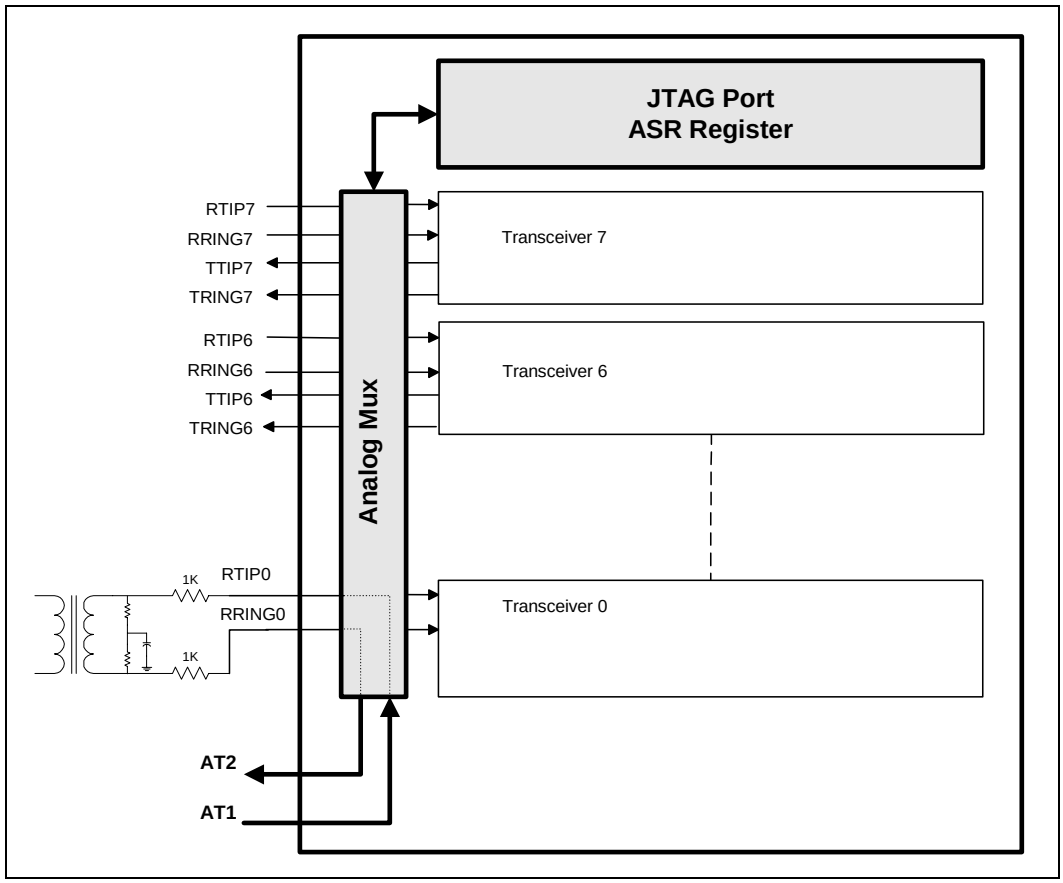
1.4 JTAG Port

Q18. Where can I get the BSDL files for the JTAG interface ?

The BSDL files for the LXT380 can be found on Intel's website at www.developer.intel.com/design/network.

Q19. How can I use the Analog JTAG port to test my metallic Tx/Rx interfaces ?

The analog JTAG functionality is illustrated in the following diagram:



The AT1 and AT2 pins are the analog test port input and output respectively. A voltage can be forced into any of the TTIP or RTIP pins. The voltage at the corresponding TRING or RRING pin is output at AT2. The selection is made by setting the ASR register in the JTAG interface.

If the connections across the primary transformer windings are good, there should be a total impedance of approximately 2 k ohm (DC) in the receive path (2 x 1 k ohm) and approximately 22 ohm (2 x 11 ohm) across the transmit path. If the impedance is much higher than the expected value, there may be an open circuit in the path (possibly caused by a bad component or soldering problem). As you can see, this feature allows testing the analog interface connections. This is something that is not possible with conventional (digital) JTAG interfaces.

1.5 General Questions

Q20. What are the main differences between the LXT381 and the LXT380?
The LXT381 features can be seen as a subset of the LXT380. The main differences are:

- The LXT381 is a data recovery only device.
- The LXT381 is controlled by hardware only.

- The LXT381 does not support G.772 monitoring.

The LXT381 provides the essential analog front-end features. It is intended for applications where the back-end ASIC implements most of the digital features such as clock recovery alarm processing.

The LXT380, with its rich set of features, is ideal for interfacing with standard framers or mappers requiring external clock recovery.

Q21. What is the maximum jitter allowed on MCLK?

MCLK is used internally as a reference for the clock recovery DPLLs. We strongly recommend a jitter free, independent MCLK clock from a crystal oscillator. Any jitter present at MCLK will be added to the RCLK output almost transparently. The designer should decide the maximum output jitter that can be tolerated at the output which is based on the specifications the equipment is to comply with.

Q22. Where can I get the IBIS models for the LXT380/1 ?

The IBIS models for the LXT380 can be found on Intel's website at www.developer.intel.com/design/network.

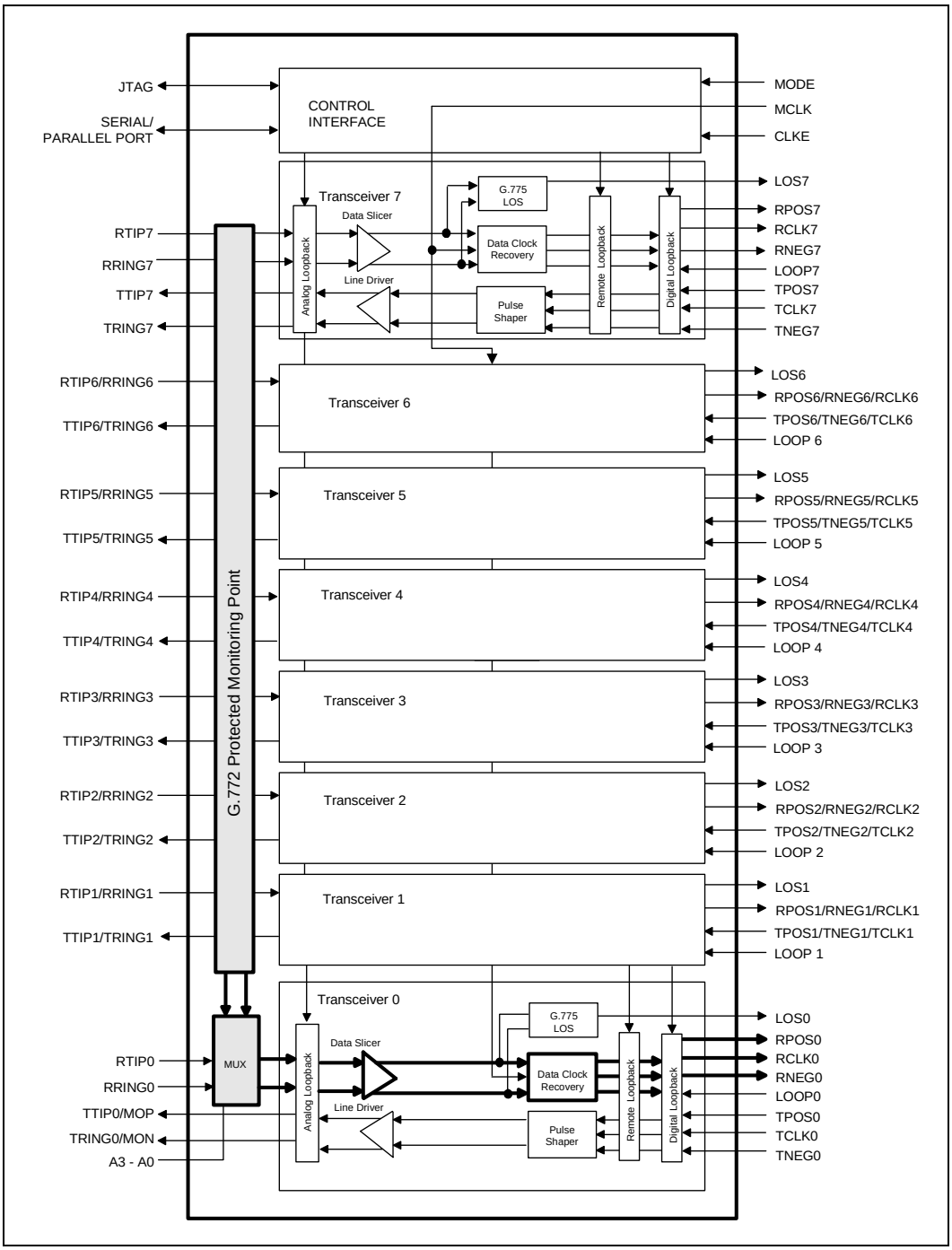
Q23. How much power is dissipated in the LXT380/1 package?

The maximum power dissipated in the package can be found under "Absolute Maximum Ratings", Table 26 and is equal to 850 mW. Do not use the maximum power supply current and power supply voltage values to derive the power dissipated in the package. A good percentage of the power consumed by the LIU is delivered to the E1 line. This power is dissipated outside the LIU package.

Q24. How does the G.772 monitoring work?

The LXT380 can be configured as an octal line interface unit with all channels working as regular transceivers. In applications using only seven channels, the eighth channel can be configured to monitor any of the remaining channel's inputs or outputs.

The monitoring is non-intrusive per ITU-T G.772. The following figure illustrates this concept.



The monitored line signal (input or output) goes through channel 0 clock and data recovery. The signal can be observed digitally at the RCLK/RPOS/RNEG outputs. This feature can also be used to create timing interfaces derived from an E1 signal. Please refer to Application Note 249128: “Timing Interface Using the LXT380".

In addition, channel 0 can be configured for Remote Loopback while in monitoring mode. This will output the same data as the signal being monitored at the channel 0 output (TTIP/ TRING). The output signal can then be connected to standard test equipment with an E1 electrical interface for monitoring purposes (non -intrusive monitoring).