

---

# R8A20211BG/R8A20210BG (MARIE\_Blade)

## Network Address Search Engine (9 M/18 M-bit Full Ternary CAM)

REJ03H0001-0100

Rev.1.00

Feb 21, 2005

---

### Description

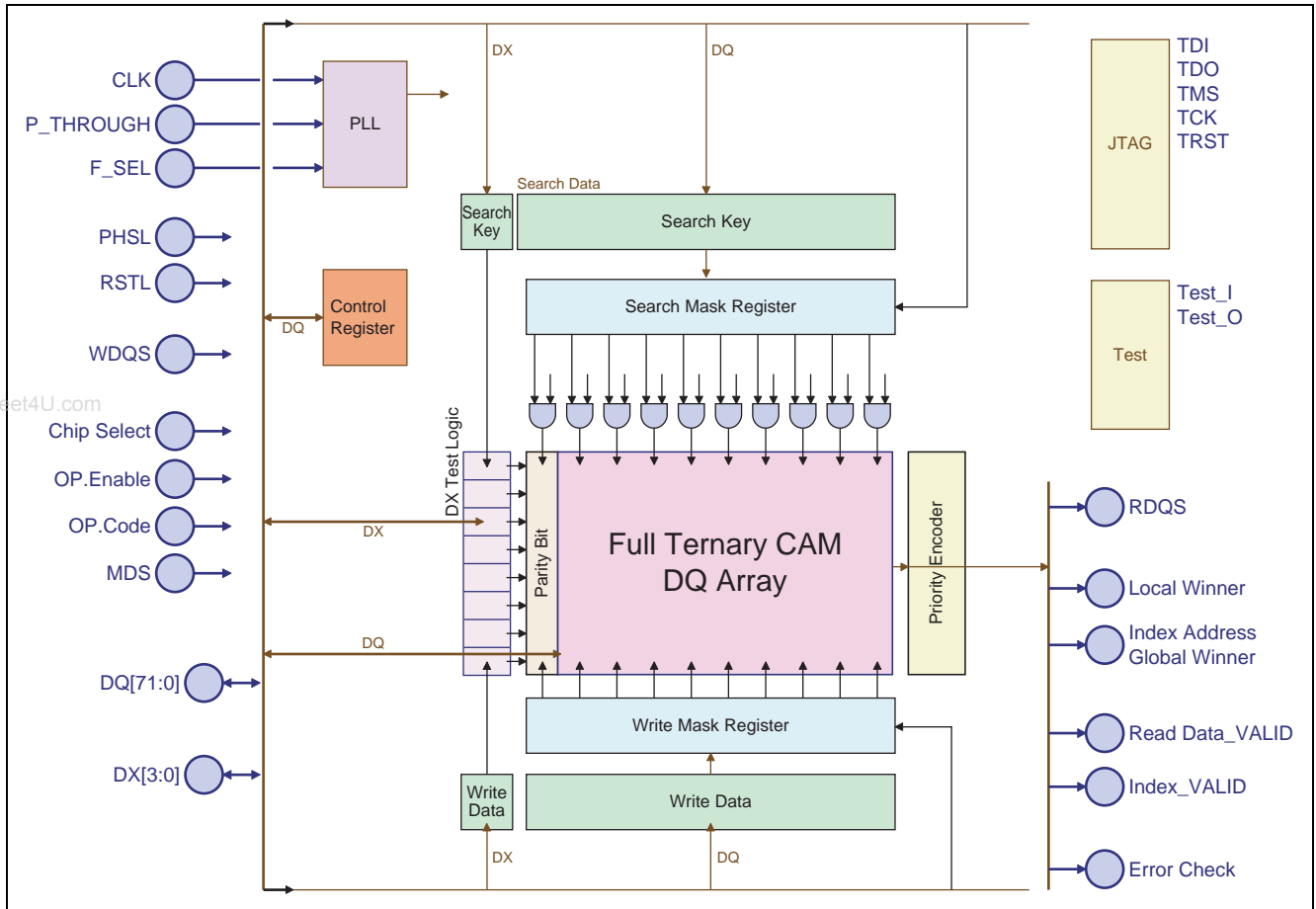
Renesas delivers MARIE\_Blade that is a ternary CAM search engine targeted for network packet classifying. The full-custom CAM memory realizes large capacity, high density and low power consumption.

MARIE\_Blade can realize up to 133 Msps in 72-bit/144-bit normal mode (parallel search 266 Msps), 66.5 Msps in 288-bit mode (parallel search 133 Msps) and 33 Msps in 576-bit mode (parallel search 66.5 Msps). The Hierarchical search reduces power consumption; The DX test logic, an extended bit, performs a DX test logic search first (primary search), and the DQ pin performs a DQ array search (secondary search). The parity bit in the DQ array can check for errors as an additional function.

### Features

- 9 M/18 M-bit full ternary CAM
- CLK operating frequency 266 MHz Max
- Maximum search rate at normal mode: 133 Msps [72-bit/144-bit lookup size]
- Maximum search rate at parallel mode: 266 Msps [72-bit/144-bit lookup size]
- Maximum search rate at normal mode: 66.5 Msps [288-bit lookup size]
- Maximum search rate at parallel mode: 133 Msps [288-bit lookup size]
- Maximum search rate at parallel mode: 33 Msps [576-bit lookup size]
- Maximum search rate at normal mode: 66.5 Msps [576-bit lookup size]
- Priority encoder
- Hierarchical search
- Parity bit (even parity) check
- IEEE 1149.1 test port
- 1.2 V core power supply
- 1.2 V power supply for search (1.0 V power supply for power saving)
- SSTL-2 interface/2.5 V I/O power supply

Block Diagram



## Functional Description

### 1. High Density and Low Power Consumption

Renesas MARIE\_Blade is a network search engine with the high-density TCAM memory cell. The minimized memory cell allows MARIE\_Blade to realize not only high performance but also small dimension and low power consumption.

### 2. SSTL-2 Interface

SSTL2 class-1/2 can be selected depending on system board specifications.

Exception: the external Vref pin provides the input reference voltage.

### 3. Programmable Array

Type of array architecture does not determine a lookup size, but the basic unit of entry address for Write TCAM is 72-bit wide. Each lookup size, 72-bit/144-bit/288-bit/576-bit, for secondary search is specified when a command is loaded: Lookup result provided by the Index Address also depends on the lookup size used.

<Entry Address> example of 18 M-bit

- 0, 1, 2, 3, 4, 5, ... 262143: 72-bit search
- 0, 2, 4, 6, 8, ... 262142: 144-bit search
- 0, 4, 8, 12, ... 262140: 288-bit search
- 0, 8, 16, 24, ... 262136: 576-bit search

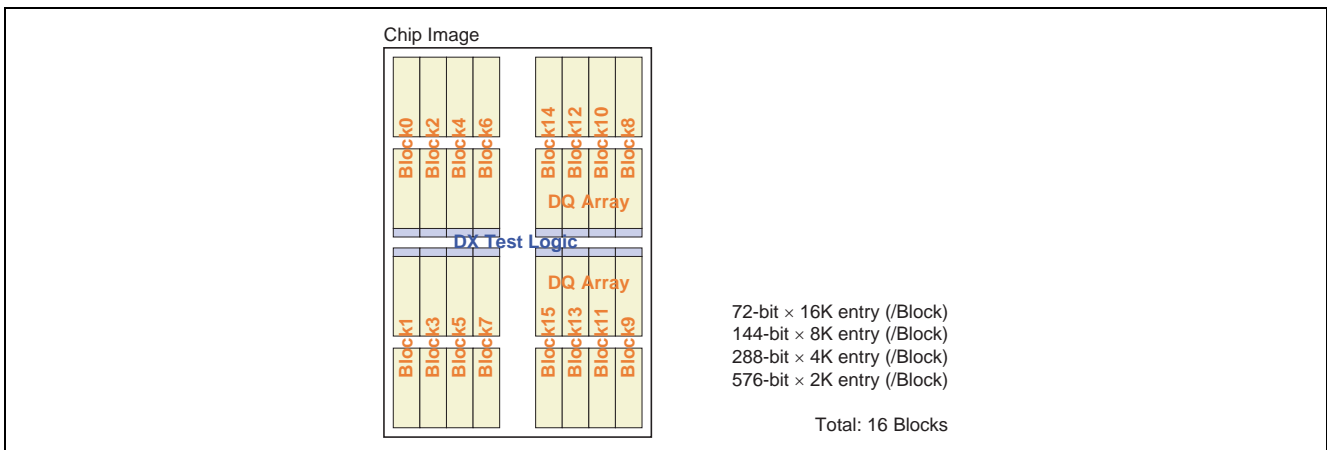


Figure 1 Block Structure

### 4. Bank Structure

The MARIE\_Blade CAM array is comprised of two banks, which enables to perform a search in parallel. The number of block in each bank is programmable and determined by the bankset register setting. The whole 16 blocks are divided to any sizes. Refer to the example on the figure 2.

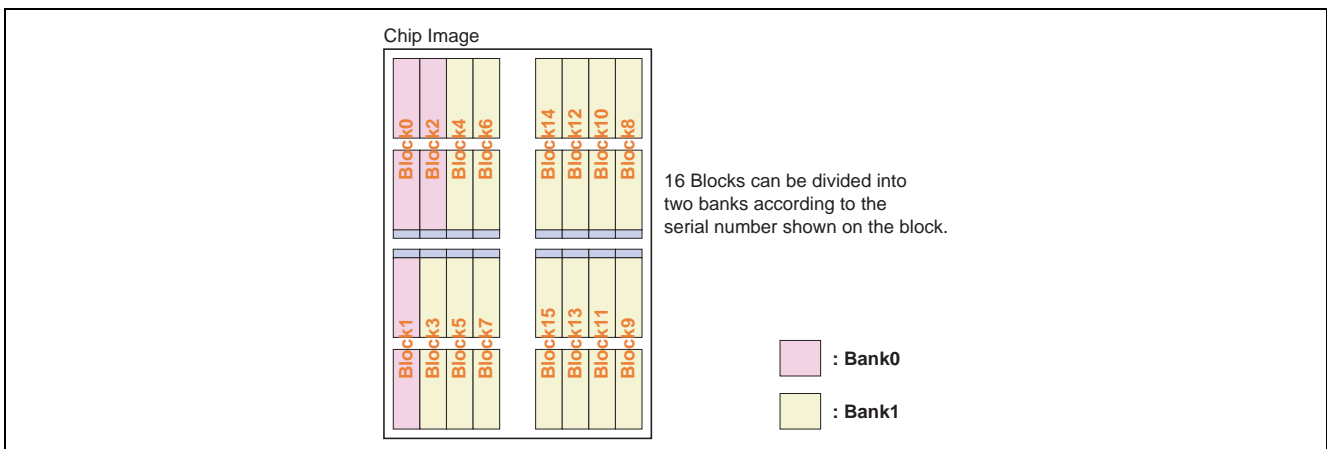


Figure 2 Bank Structure Example

5. Greedy Operation

MARIE\_Blade offers the Greedy operation to write to the DQ array. In the Greedy operation, Block 0-7 (figure 2) are defined as Mat A, and Block 8-15 are defined as Mat B. The Greedy writes to an entry in each Mat at a time (total two entries). The DQ pin [17:0] carries an address for access, but its value [17] selecting either MAT A or MAT B is ignored in this case.

6. Hierarchical Search

MARIE\_Blade has two types of search: the DX test logic search and the DQ array search. The DX Test Logic consists of 4-bit entry, and DQ array, 72-bit entry. MARIE\_Blade searches the DX Test Logic (primary search) first, and then searches only the DQ array having a hit address of primary search (secondary search). Therefore the Hierarchical Search can reduce power consumption.

Each block in the DX Test Logic has a single kind of data. Note: MARIE\_Blade is not partitioned by configuration (72-bit/144-bit/288-bit/576-bit). If the user does not utilize the DX Test Logic search, MARIE\_Blade searches the entire DQ array.

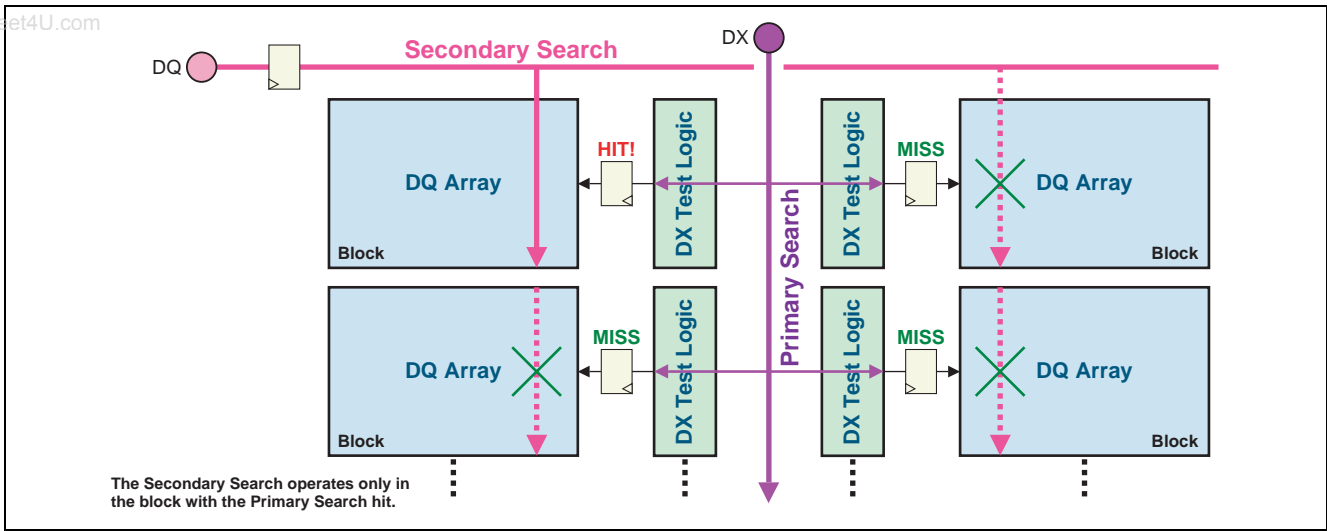


Figure 3 Hierarchical Search

7. Global Mask Search Register

The Global Mask Search Register (GMSR) controls bits that participate in the secondary search. The GMSR mask consists of the same bit width as that of corresponding CAM DQ, and it masks per bit. The GMSR is valid only during the secondary search. Note that the operation of other registers is restricted during the parallel mode.

Please refer to another section for details.

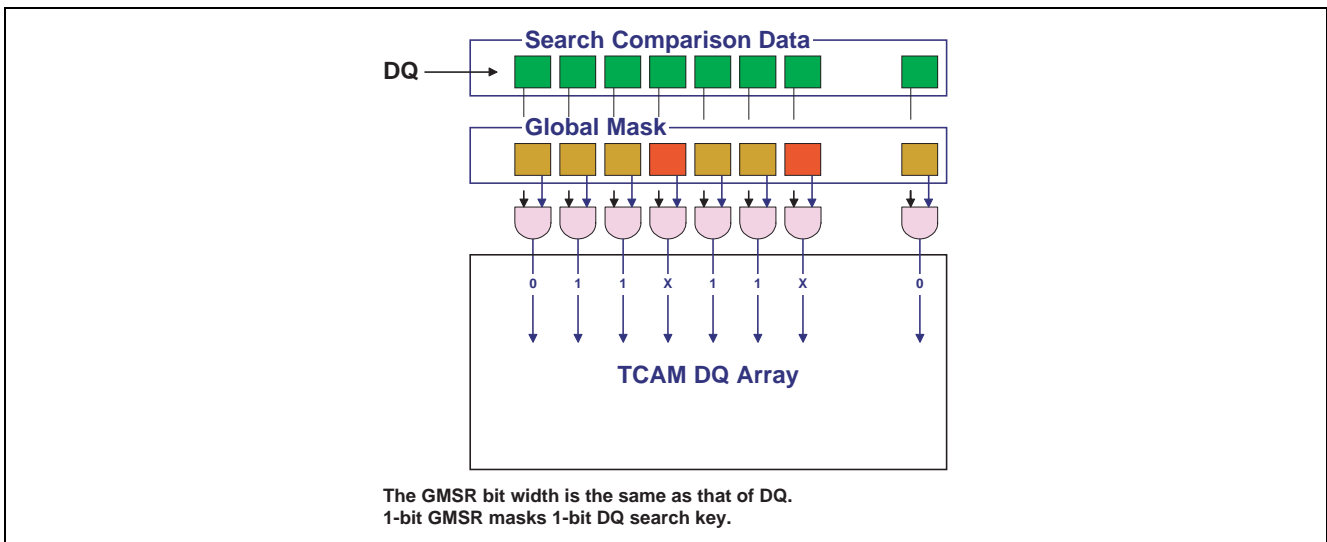


Figure 4 Global Mask Search

8. Write Mask Register

The Write Mask Register (WMR) controls bits that participate in the Write TCAM operation. The WMR mask has the same bit width as that of corresponding CAM DQ array.

Also, this register is valid only during Write TCAM. When writing to the 9 M Mats simultaneously (Greedy Operation), MARIE\_Blade uses the mask register that is shared between MAT A and Mat B (Greedy Write).

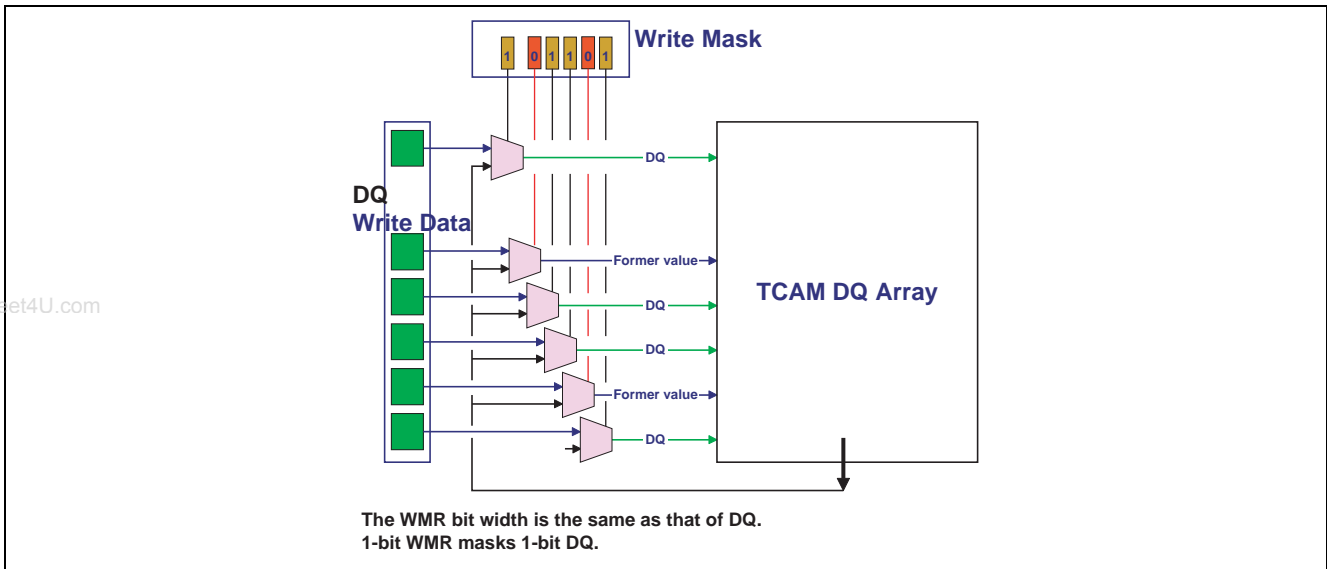


Figure 5 Masked Write TCAM

9. Address Source and Data Source

A couple of different sources can be selected to write addresses and/or data into the DQ array. Two possible sources for the address input are the DQ input pin and the Address Source Register (ASR). Three possible sources for data input are the DQ input pin, the Data Source Register (DSR), or the Load Data Register (LDR).

— Address Source Register (ASR)

There are two sources to input entry addresses to the DQ array: The DQ pin and ASR. An entry address with a hit is stored in the ASR so that the DQ pin can trace hit history with this ASR.

In addition, ASR is capable of detecting empty entries as Pseudo Learn.

— Data Source Register (DSR)

The DQ input pin, DSR or LDR can be used as a data source.

DSR stores data of search miss. Pseudo Learn and Write TCAM to the array can be realized by specifying the DSR having search miss data (data source).

— Load Data Register (LDR)

Load Data Register (LDR) is used as the write data source in order to operate Move. See the figure 6.

The Load Data command loads the DQ data into the LDR first, and then operates the Write TCAM with this LDR (source register). Please refer to another section for details.

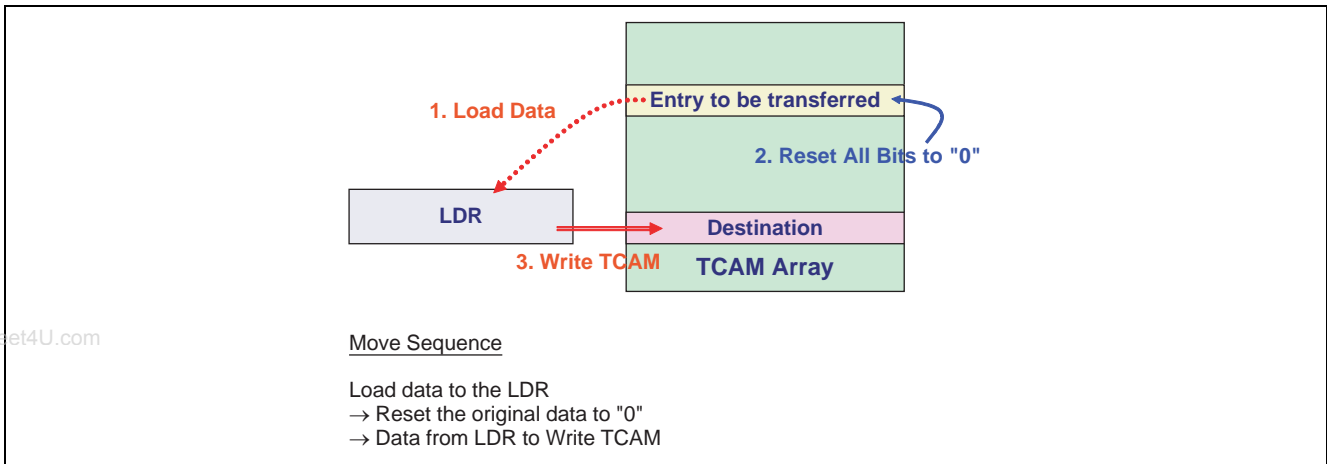


Figure 6 Move

10. Pseudo Learn

MARIE\_Blade does not support an ordinary Learn function required by LAN switch for example. However, with a combination of DSR and ASR, Pseudo Learn can take the place of Learn. A search key resulting in a miss is stored into the DSR. Then Pseudo Learn can be achieved by operating Write TCAM with the DSR. Furthermore, search for empty entries can be added into this process. In this case, the data to be input must contain an entry flag bit. There is an example of 72-bit Normal Search. The user must select MSB [71] DQ data as the empty entry flag bit, and set it to be [even, odd] = [0, 1] respectively (1 bit consists of even and odd). If there is any empty entry indicating [1, 0], it means all data are occupied. In other words, all data in the TCAM must be [0, 1] after reset, and bit-1 [71] must be always [even, odd]= [1,0] during the Write TCAM.

After setting a rule likewise, the procedure follows...

- (1) When a search miss occurs, store the search miss key into the DSR
- (2) Stop searching when the DSR is full of search miss keys
- (3) Search only the DQ MSB with GMSR  
(Search key, DQ [71] = 0, detects empty entries)
- (4) Store the hit address of (3)
- (5) Do the Write TCAM with (1) DSR data and (4) ASR address

The Write Delete Entry command can facilitate to reset empty entry bits. This command resets all bits in the assigned entry to be [even, odd] = [0,1].

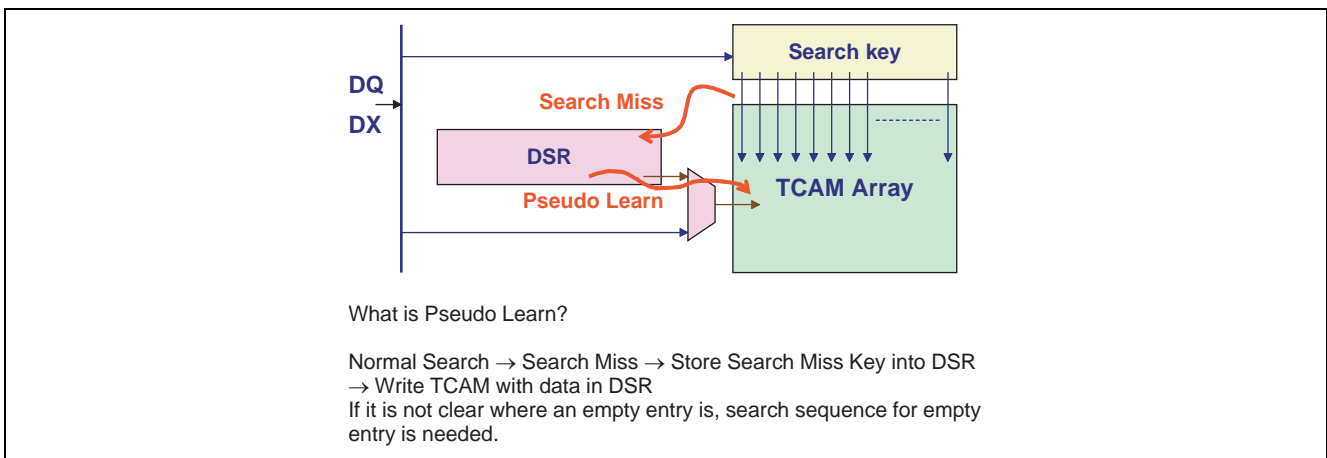


Figure 7 Pseudo Learn

11. Parity Bit Check

MARIE\_Blade provides an error check function using parity bits. Soft error can be detected with upper 2 bits in each DQ entry (72-bit lookup) as the parity bit. If Status Set Register (ST) is set to allow the error check, Parity Bit Check is automatically operated during Read TCAM.

Once any error is found, the error flag goes high and retrieved data is input. Go through the following steps to provide the parity bit for 72-bit entry.

>> DQ [70] ... Set even bits in DQ [69:0] to be even parity

>> DQ [71] ... Set odd bits in DQ [69:0] to be even parity

Note that MARIE\_Blade supports neither Error Check & Correct nor Parity Bit Generation.

## Pin Description

- Common: 13 pins

Pin Name	Symbol	I/O	Function
Clock input	CLK	I	CAM Clock. All input signals except OP and DQ reference to rising edge of CLK. Activates all output signals except IND, LW and GW in order to control.
Phase L	PHSL	I	Asserted in half operating frequency range. This signal and CLK generate internal CAM_CLK providing Cycle-A and Cycle-B. Please refer to another section for details.
PLL through	P_THROUGH	I	Bypasses the PLL circuit. Refer to the Block Diagram. Setting "L" operates PLL.
Frequency select	F_SEL	I	Specifies PLL Lock Range depending on CLK operation frequency. Refer to the Table 1.
WDQS [4:0]	WDQS	I	Source Synchronous Clock for input signals from OP and DQ.
RDQS	RDQS	O-Tri	Source Synchronous Clock for output signals from IND, LW and GW.
Reset L	RSTL	I	Hardware reset for MARIE-Blade.

- Network Processor/ASIC Interface: 110 pins

Pin Name	Symbol	I/O	Function
Chip select	C_SEL	I	Enables only chips with High. This signal must be asserted during two cycles, Cycle-A and Cycle-B.
Operation enable	OP_ENA	I	Indicates that commands from OP are valid. This signal must be set during two cycles, Cycle-A and Cycle-B.
Mode select	MDS	I	Selects Normal or Parallel for search, and Normal or Greedy for write.
Op.code [6:0]	OP[6:0]	I	OP [6:0] controls command codes. Should be asserted at Cycle-A
DX [3:0]	DX[3:0]	I/O-Tri	<b>Extended Data</b> Primary search key is input/output when DX Test Logic Read/Write/Search command is loaded.
DQ/address [71:0]	DQ[71:0]	I/O-Tri	<b>Data Pin</b> Multiplexed pin between address and data, which functions during DQ array Read/Write/Search command.
Index address [17:0]	IND[17:0]	O-Tri	Input address into externally located SRAMs. Entry address carried by this pin is search hit address. If ASR is used as write address source, IND retrieves write address from it.
Local winner flag	LW	O	Goes high when search results in hit.
Global winner flag [1:0]	GW	O-Tri	Directly outputs prioritized device ID set by ST [9:8] when search results in hit.
Read data valid	RD_VD	O	Qualifies read data when DQ/DX output.
Index valid	IND_VD	O	Qualifies read data when IND outputs regardless of search result.
Error check flag	EC_F	O	Goes high when Parity Bit Check finds any errors. Enable only during a Read TCAM, whose setting allows error check.



- JTAG Interface: 5 pins

Pin Name	Symbol	I/O	Function
Test mode select	TMS	I	Gives input command for TAP controller.
Test data input	TDI	I	Serial input of registers placed between TDI and TDO.
Test data output	TDO	O	Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller.
Test clock	TCK	I	Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from the falling edge of TCK.
JTAG reset	TRST	I	JTAG reset can be used to reset TAP controller.

Note: JTAG specification is referenced to IEEE 1149.1.

- Power and Ground

Pin Name	Symbol	Pins	Function
Vectored	V_CORE	50	1.2 V for core and peripheral circuitry
Voltage for search	V_MAT	41	Power to match line 1.2 V to 1.0 V
I/O buffer supply voltage	VCCQ	24	Supply voltage for I/O buffer = 2.5 V
Input reference voltage	V_REF	8	50% of VCCQ
Ground	GND	104	0 V Ground level
Supply voltage for PLL	VPLL	1	2.5 V
Ground for PLL	GPLL	1	0 V Ground level for PLL

Follow the table below to input F\_SEL depending on the CLK operation frequency range

**Table 1 F\_SEL Input Value for CLK Operation Frequency Range**

Input CLK (MHz)	F_SEL [2]	F_SEL [1]	F_SEL [0]
250 to 350	0	1	1
150 to 225	0	1	0
125 to 175	0	0	1
75 to 112.5	0	0	0

## Pin Layout

## 1. Signal

Ball Name	Pin Name	Ball Name	Pin Name	Ball Name	Pin Name	Ball Name	Pin Name
A2	DQ [71]	G1	DQ [56]	N2	OP_ENA	Y1	DQ [39]
A23	DQ [34]	G3	DQ [55]	N24	TEST_I [0]	Y2	DQ [40]
A24	DQ [35]	G4	DQ [54]	P1	OP [0]	Y4	DQ [41]
B1	DQ [70]	G22	IND [17]	P2	OP [1]	Y22	DQ [4]
B2	DQ [69]	G23	DQ [18]	P3	OP [2]	Y24	DQ [3]
B3	DQ [68]	G25	DQ [19]	P4	OP [3]	Y25	DQ [2]
B4	DQ [67]	H1	RD_VD	P24	TEST_I [1]	AA2	DQ [42]
B22	DQ [30]	H2	P_THROUGH	P25	LW	AA4	DQ [43]
B23	DQ [31]	H3	F_SEL [2]	R1	OP [4]	AA22	DQ [6]
B24	DQ [32]	H23	IND [14]	R3	OP [5]	AA24	DQ [5]
B25	DQ [33]	H24	IND [15]	R24	TEST_I [2]	AB1	DQ [44]
C1	DQ [66]	H25	IND [16]	R25	IND_VD	AB2	DQ [45]
C3	DQ [65]	J2	F_SEL [1]	T1	OP [6]	AB3	WDQS [2]
C4	DQ [64]	J3	F_SEL [0]	T2	TMS	AB23	WDQS [0]
C22	DQ [27]	J23	IND [12]	T23	EC_F	AB24	DQ [8]
C23	DQ [28]	J24	IND [13]	T24	IND [1]	AB25	DQ [7]
C25	DQ [29]	K1	DX [3]	T25	IND [0]	AC1	DQ [46]
D1	DQ [63]	K2	DX [2]	U2	TCK	AC3	DQ [47]
D2	DQ [62]	K4	DX [1]	U3	TRST	AC4	DQ [48]
D3	WDQS [3]	K22	RDQS	U23	IND [3]	AC22	DQ [11]
D23	WDQS [1]	K23	IND [9]	U24	IND [2]	AC23	DQ [10]
D24	DQ [25]	K24	IND [10]	V1	TDI	AC25	DQ [9]
D25	DQ [26]	K25	IND [11]	V2	TDO	AD1	DQ [49]
E2	DQ [61]	L1	DX [0]	V3	DQ [36]	AD2	DQ [50]
E4	DQ [60]	L23	PHSL	V22	IND [7]	AD3	DQ [51]
E22	DQ [23]	L25	GW [1]	V23	IND [6]	AD4	DQ [52]
E24	DQ [24]	M1	MDS	V24	IND [5]	AD22	DQ [15]
F1	DQ [59]	M2	C_SEL	V25	IND [4]	AD23	DQ [14]
F2	DQ [58]	M3	WDQS [4]	W1	DQ [37]	AD24	DQ [13]
F4	DQ [57]	M4	RSTL	W3	DQ [38]	AD25	DQ [12]
F22	DQ [20]	M22	CLK	W22	DQ [1]	AE2	DQ [53]
F24	DQ [21]	M24	TEST_O	W23	DQ [0]	AE23	DQ [17]
F25	DQ [22]	M25	GW [0]	W25	IND [8]	AE24	DQ [16]

2. Power/Ground

• VCCQ

Ball Name	Pin Name
A1	VCCQ
A25	VCCQ
C2	VCCQ
C24	VCCQ
E1	VCCQ
E25	VCCQ

Ball Name	Pin Name
G2	VCCQ
G24	VCCQ
J1	VCCQ
J25	VCCQ
L2	VCCQ
N1	VCCQ

Ball Name	Pin Name
N25	VCCQ
R2	VCCQ
U1	VCCQ
U25	VCCQ
W2	VCCQ
W24	VCCQ

Ball Name	Pin Name
AA1	VCCQ
AA25	VCCQ
AC2	VCCQ
AC24	VCCQ
AE1	VCCQ
AE25	VCCQ

• V\_CORE

Ball Name	Pin Name
A3	V_CORE
A5	V_CORE
A6	V_CORE
A7	V_CORE
A8	V_CORE
A9	V_CORE
A10	V_CORE
A11	V_CORE
A12	V_CORE
A13	V_CORE
A14	V_CORE
A15	V_CORE
A16	V_CORE

Ball Name	Pin Name
A17	V_CORE
A18	V_CORE
A19	V_CORE
A20	V_CORE
A21	V_CORE
D4	V_CORE
D22	V_CORE
E3	V_CORE
E23	V_CORE
F3	V_CORE
F23	V_CORE
K3	V_CORE
T3	V_CORE

Ball Name	Pin Name
Y3	V_CORE
Y23	V_CORE
AA3	V_CORE
AA23	V_CORE
AB4	V_CORE
AB22	V_CORE
AE3	V_CORE
AE5	V_CORE
AE6	V_CORE
AE7	V_CORE
AE8	V_CORE
AE9	V_CORE
AE10	V_CORE

Ball Name	Pin Name
AE11	V_CORE
AE12	V_CORE
AE13	V_CORE
AE14	V_CORE
AE15	V_CORE
AE16	V_CORE
AE17	V_CORE
AE18	V_CORE
AE19	V_CORE
AE20	V_CORE
AE21	V_CORE

• V\_MAT

Ball Name	Pin Name
D5	V_MAT
D6	V_MAT
D7	V_MAT
D8	V_MAT
D9	V_MAT
D10	V_MAT
D11	V_MAT
D12	V_MAT
D13	V_MAT
D14	V_MAT
D15	V_MAT

Ball Name	Pin Name
D16	V_MAT
D17	V_MAT
D18	V_MAT
D19	V_MAT
D20	V_MAT
D21	V_MAT
H4	V_MAT
H22	V_MAT
J4	V_MAT
J22	V_MAT
U4	V_MAT

Ball Name	Pin Name
U22	V_MAT
V4	V_MAT
AB5	V_MAT
AB6	V_MAT
AB7	V_MAT
AB8	V_MAT
AB9	V_MAT
AB10	V_MAT
AB11	V_MAT
AB12	V_MAT
AB13	V_MAT

Ball Name	Pin Name
AB14	V_MAT
AB15	V_MAT
AB16	V_MAT
AB17	V_MAT
AB18	V_MAT
AB19	V_MAT
AB20	V_MAT
AB21	V_MAT

• VREF

Ball Name	Pin Name
A4	VREF
A22	VREF

Ball Name	Pin Name
L4	VREF
N22	VREF

Ball Name	Pin Name
R4	VREF
R23	VREF

Ball Name	Pin Name
AE4	VREF
AE22	VREF

• GND

Ball Name	Pin Name
B5	GND
B6	GND
B7	GND
B8	GND
B9	GND
B10	GND
B11	GND
B12	GND
B13	GND
B14	GND
B15	GND
B16	GND
B17	GND
B18	GND
B19	GND
B20	GND
B21	GND
C5	GND
C6	GND
C7	GND
C8	GND
C9	GND
C10	GND
C11	GND
C12	GND
C13	GND

Ball Name	Pin Name
C14	GND
C15	GND
C16	GND
C17	GND
C18	GND
C19	GND
C20	GND
C21	GND
L3	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L22	GND
L24	GND
M11	GND
M12	GND
M13	GND
M14	GND
M15	GND
M23	GND
N3	GND
N4	GND
N11	GND
N12	GND

Ball Name	Pin Name
N13	GND
N14	GND
N15	GND
N23	GND
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND
P23	GND
R11	GND
R12	GND
R13	GND
R14	GND
R15	GND
T4	GND
T22	GND
W4	GND
AC5	GND
AC6	GND
AC7	GND
AC8	GND
AC9	GND
AC10	GND
AC11	GND
AC12	GND

Ball Name	Pin Name
AC13	GND
AC14	GND
AC15	GND
AC16	GND
AC17	GND
AC18	GND
AC19	GND
AC20	GND
AC21	GND
AD5	GND
AD6	GND
AD7	GND
AD8	GND
AD9	GND
AD10	GND
AD11	GND
AD12	GND
AD13	GND
AD14	GND
AD15	GND
AD16	GND
AD17	GND
AD18	GND
AD19	GND
AD20	GND
AD21	GND

• VPLL/GPLL

Ball Name	Pin Name
P22	VPLL

Ball Name	Pin Name
R22	GPLL

Pin Arrangement

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25		
A	VCCQ	DQ[71]	V <sub>CORE</sub>	VREF	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	VREF	DQ[34]	DQ[35]	VCCQ	A	
B	DQ[70]	DQ[69]	DQ[68]	DQ[67]	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ[30]	DQ[31]	DQ[32]	DQ[33]	B
C	DQ[66]	VCCQ	DQ[65]	DQ[64]	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ[27]	DQ[28]	VCCQ	DQ[29]	C	
D	DQ[63]	DQ[62]	WDQS[3]	V <sub>CORE</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>CORE</sub>	WDQS[1]	DQ[25]	DQ[26]	D	
E	VCCQ	DQ[61]	V <sub>CORE</sub>	DQ[60]																		DQ[23]	V <sub>CORE</sub>	DQ[24]	VCCQ	E	
F	DQ[59]	DQ[58]	V <sub>CORE</sub>	DQ[57]																		DQ[20]	V <sub>CORE</sub>	DQ[21]	DQ[22]	F	
G	DQ[56]	VCCQ	DQ[55]	DQ[54]																		DQ[17]	DQ[18]	VCCQ	DQ[19]	G	
H	RD_VD	P_THROUGH	F_SEL[2]	V <sub>MAT</sub>																		V <sub>MAT</sub>	IND[14]	IND[15]	IND[16]	H	
J	VCCQ	F_SEL1	F_SEL[0]	V <sub>MAT</sub>																		V <sub>MAT</sub>	IND[12]	IND[13]	VCCQ	J	
K	DX[3]	DX[2]	V <sub>CORE</sub>	DX[1]																		RDQS	IND[9]	IND[10]	IND[11]	K	
L	DX[0]	VCCQ	GND	VREF							GND	GND	GND	GND	GND							GND	PHSL	GND	GW[1]	L	
M	MDS	C_SEL	WDQS[4]	RSTL							GND	GND	GND	GND	GND							CLK	GND	TEST_O	GW[0]	M	
N	VCCQ	OP_ENA	GND	GND							GND	GND	GND	GND	GND							VREF	GND	TEST_I[0]	VCCQ	N	
P	OP[0]	OP[1]	OP[2]	OP[3]							GND	GND	GND	GND	GND							VPLL	GND	TEST_I[1]	LW	P	
R	OP[4]	VCCQ	OP[5]	VREF							GND	GND	GND	GND	GND							GPLL	VREF	TEST_I[2]	IND_VD	R	
T	OP[6]	TMS	V <sub>CORE</sub>	GND																		GND	EC_F	IND[1]	IND[0]	T	
U	VCCQ	TCK	TRST	V <sub>MAT</sub>																		V <sub>MAT</sub>	IND[3]	IND[2]	VCCQ	U	
V	TDI	TDO	DQ[36]	V <sub>MAT</sub>																		IND[7]	IND[6]	IND[5]	IND[4]	V	
W	DQ[37]	VCCQ	DQ[38]	GND																		DQ[1]	DQ[0]	VCCQ	IND[8]	W	
Y	DQ[39]	DQ[40]	V <sub>CORE</sub>	DQ[41]																		DQ[4]	V <sub>CORE</sub>	DQ[3]	DQ[2]	Y	
AA	VCCQ	DQ[42]	V <sub>CORE</sub>	DQ[43]																		DQ[6]	V <sub>CORE</sub>	DQ[5]	VCCQ	AA	
AB	DQ[44]	DQ[45]	WDQS[2]	V <sub>CORE</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>MAT</sub>	V <sub>CORE</sub>	WDQS[0]	DQ[8]	DQ[7]	AB
AC	DQ[46]	VCCQ	DQ[47]	DQ[48]	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ[11]	DQ[10]	VCCQ	DQ[9]	AC	
AD	DQ[49]	DQ[50]	DQ[51]	DQ[52]	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ[15]	DQ[14]	DQ[13]	DQ[12]	AD	
AE	VCCQ	DQ[53]	V <sub>CORE</sub>	VREF	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	V <sub>CORE</sub>	VREF	DQ[17]	DQ[16]	VCCQ	AE	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25		

(Top view)

Package Dimensions

