S5N8950

G.dmt ADSL Transceiver for CO and CPE

Preliminary Information Rev.1.2

Nov. 2000.

1 General Description

The **S5N8950** is an optimized chip of ADSL transceiver supporting G.992.1, G.992.2 and T1.413, and provides a total chipset solution with AFE chip (***S5N8951***) for both CO and CPE applications. The **S5N8950** consists of the ATM framer, DMT modem, and DSP core. It supports various interfaces of UTOPIA level 2 for ATM data and serial interface for Non-ATM data, and host controller compatible with Motorola and Intel. It is fully compatible with G.Lite and G.dmt standards to satisfy interoperability with compatible other chipsets. For CO/CPE application, evaluation tool kit shall be provided.

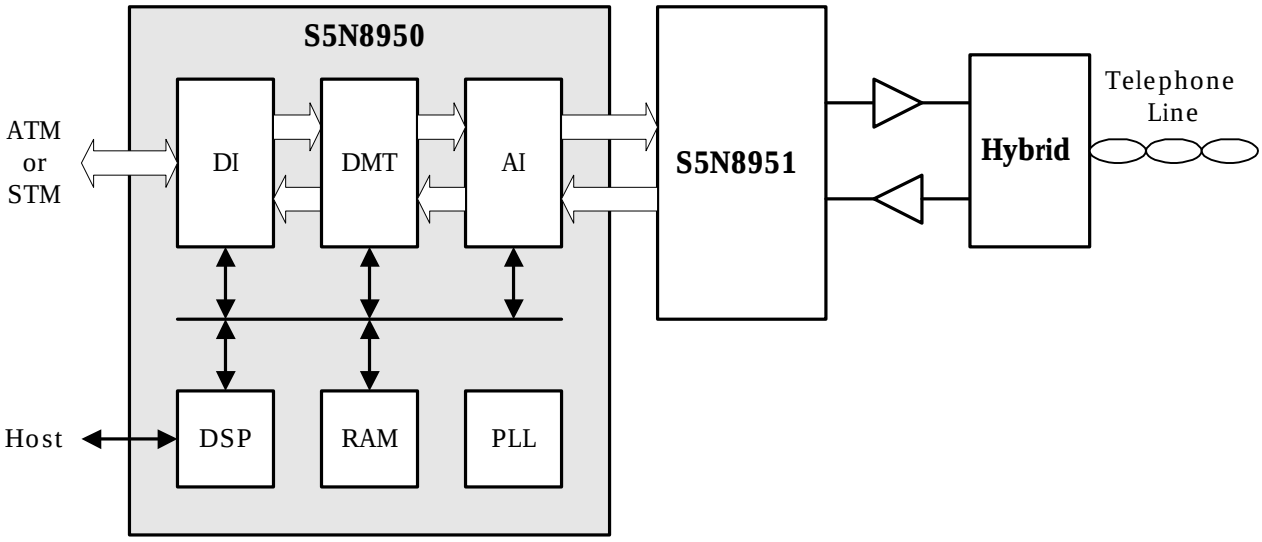

Figure 1: ADSL Transceiver configuration for S5N8950.

2 Main Features

- Power and performance optimized single port DMT.
- Supports ITU-T G.992.1 (G.dmt) , G.992.2 (G.Lite) and T1.413 standards.
- STM serial interface and ATM UTOPIA level 1 and level 2 interface.
- Supports both the FDM-based and EC-based DMT line coding.
- Analog and digital PLL modes.
- Adaptive frequency and time domain equalizing.
- Provides over 10 Mbps downstream data rate and over 640 Kbps upstream data rate
- Flexible host interface for Motorola and Intel Controller
- Reed-Solomon Forward Error Correction with Interleaving.
- 3-D trellis coding and Viterbi algorithm.
- Supports all of the framing modes.
- Supports Rate Adaptive Mode.
- 12-Bit ADC and DAC with Over-sampling
- Downloadable coefficients of rate-conversion filter banks.
- Low power consumption (less than 0.5 Watt).
- Power management
- Self-diagnostics
- 0.18 um 1.8 V CMOS technology.
- 3.3 V external interface.
- Operation Temperature : -40 C to 85 C
- Low Cost & Compact Package (160 QFP)

3 External Pin Description

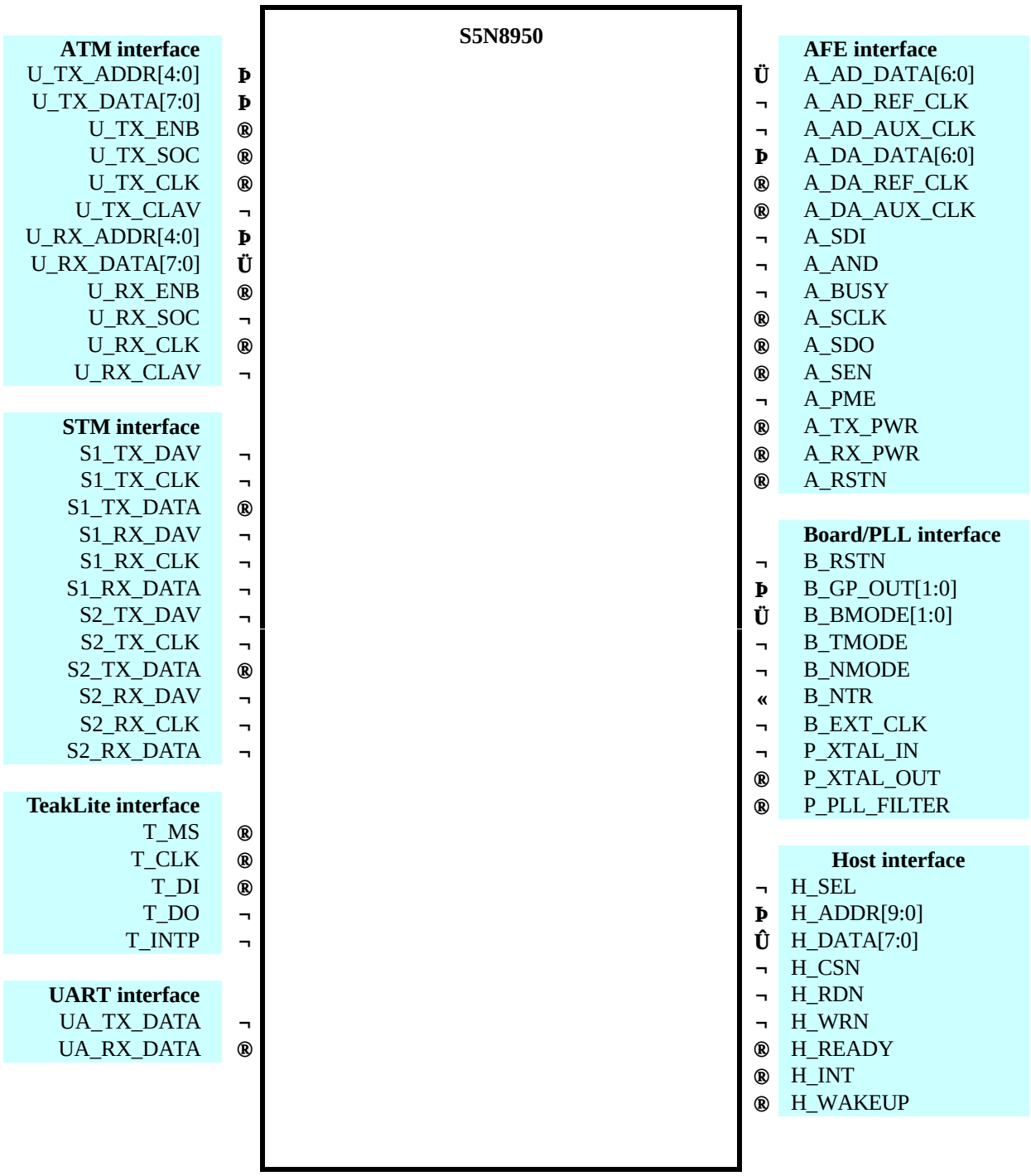

Figure 2: Pin diagram

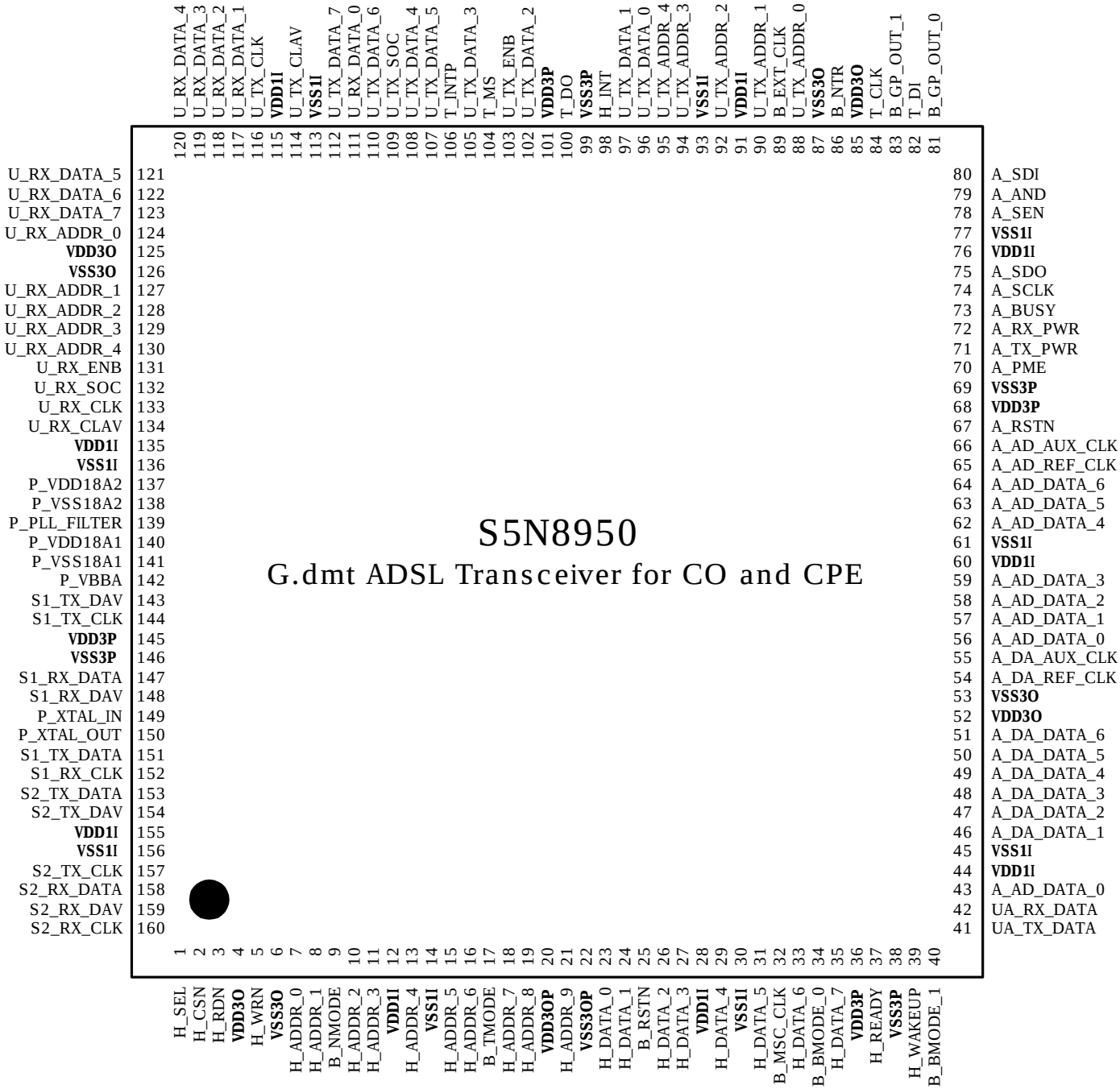

Figure 3: Pin configuration

Interface Type	Mnemonic	Type	Driver	Function
ATM interface				
	U_TX_ADDR[4:0]	I	PHTICD	Utopia Tx Address
	U_TX_DATA[7:0]	I	PHTICD	Utopia Tx Data
	U_TX_ENB	I	PHTICD	Utopia Tx Enable
	U_TX_SOC	I	PHTICD	Utopia Tx Start of Cell
	U_TX_CLK	I	PHTICD	Utopia Tx Clock. 25 MHz
	U_TX_CLAV	OZ	PHTOT4	Utopia Tx Cell Available
	U_RX_ADDR[4:0]	I	PHTICD	Utopia Rx Address[4:0]
	U_RX_DATA[7:0]	OZ	PHTOT4	Utopia Rx Data[7:0]
	U_RX_ENB	I	PHTICD	Utopia Rx Enable
	U_RX_SOC	OZ	PHTOT4	Utopia Rx Start of Cell
	U_RX_CLK	I	PHTICD	Utopia Rx Clock. 25 MHz
	U_RX_CLAV	OZ	PHTOT4	Utopia Rx Cell Available
STM interface				
	S1_TX_DAV	O	PHOB4	Serial Tx data valid signal in the 1-st STM
	S1_TX_CLK	O	PHOB4	Serial Tx clock in the 1-st STM
	S1_TX_DATA	I	PHTICD	Serial Tx data in the 1-st STM
	S1_RX_DAV	O	PHOB4	Serial Rx data valid signal in the 1-st STM
	S1_RX_CLK	O	PHOB4	Serial Rx clock in the 1-st STM
	S1_RX_DATA	O	PHOB4	Serial Rx data in the 1-st STM
	S2_TX_DAV	O	PHOB4	Serial Tx data valid signal in the 2-nd STM
	S2_TX_CLK	O	PHOB4	Serial Tx clock in the 2-nd STM
	S2_TX_DATA	I	PHTICD	Serial Tx data in the 2-nd STM
	S2_RX_DAV	O	PHOB4	Serial Rx data valid in the 2-nd STM
	S2_RX_CLK	O	PHOB4	Serial Rx clock in the 2-nd STM
	S2_RX_DATA	O	PHOB4	Serial Rx data in the 2-nd STM
Host Interface				
	H_SEL	I	PHTICD	Host type : [0]=Motorola / [1]= Intel
	H_ADDR[9:0]	I	PHTICD	Host address bus
	H_DATA[7:0]	B	PHTBCDT6SM	Host data bus
	H_CSN	I	PHTICD	Chip selection
	H_RDN	I	PHTICD	Motorola: Not used. / Intel: Read enable (active low)
	H_WRN	I	PHTICD	Motorola: [0]=write enable / [1]=read enable / Intel: Write Enable (active low)
	H_READY	OZ	PHTOT4	Motorola: Host CPU DTACK (active low) / Intel: Host CPU Ready (active high)
	H_INT	O	PHOB4	Motorola: Interrupt IRQ (active low) / Intel: Interrupt INT (active high)
	H_WAKEUP	O	PHOB4	Host Wakeup

AFE interface				
	A_AD_DATA[6:0]	I	PHICD	ADC data for 2 phase.
	A_AD_REF_CLK	I	PHICD	ADC data reference clock for DMT b2b test
	A_AD_AUX_CLK	I	PHICD	ADC data strobe clock for DMT b2b test
	A_DA_DATA[6:0]	O	PHOB2	DAC data for 2 phase
	A_DA_REF_CLK	O	PHOB2	DAC data reference clock
	A_DA_AUX_CLK	O	PHOB2	DAC data strobe clock
	A_SDI	I	PHICU	AFE serial input data
	A_AND	I	PHICD	Audible noise detection (active high)
	A_BUSY	I	PHICD	AFE busy (active high)
	A_SCLK	O	PHOB2	AFE serial clock
	A_SDO	O	PHOB2	AFE serial output data
	A_SEN	O	PHOB2	AFE serial enable (active low)
	A_PME	O	PHICD	AFE power management enable
	A_TX_PWR	O	PHOB2	TX line driver power enable (active high)
	A_RX_PWR	O	PHOB2	RX line driver power enable (active high)
	A_RSTN	O	PHOB2	AFE reset (active low)

Board / PLL interface				
	B_RSTN	I	PHIS	System reset (active low)
	B_GP_OUT[1:0]	O	PHOB2	General purpose output
	B_BMODE[1:0]	I	PHIC	TeakLite boot mode selection [0] = simple reset [1] = boot from Host CPU (normal mode) [2] = boot from JTAG (emulation mode) [3] = self-booting (test mode)
	B_TMODE	I	PHIC	Test Mode Enable (DSP view, Scan Test, Memory BIST, PLL Test) [0] Normal, [1] Test Mode
	B_NMODE	I	PHIC	NAND tree test mode [0] Normal, [1] NAND tree test mode
	B_NTR	B	PHTBCT4	ATM Network Timing Reference
	B_EXT_CLK	I	PHIC	external clock
	B_MSC_CLK	I	PHIC	misc. clock for BIRA test
	P_XTAL_IN	I	PHSOSCM26	XTAL input for clock.
	P_XTAL_OUT	O		XTAL output for clock.
	P_PLL_FILTER	O	POAR50_ABB	Internal PLL pump out connected to filter.

TeakLite Interface				
	T_MS	I	PHTICD	TeakLite JTAG test mode select
	T_CLK	I	PHTICD	TeakLite JTAG test clock
	T_DI	I	PHTICD	TeakLite JTAG test input data
	T_DO	OZ	PHTOT4	TeakLite JTAG test output data
	T_INTP	O	PHOB4	TeakLite TJAM interrupt to host

UART interface				
	UA_TX_DATA	O	PHOB4	UART Rx data
	UA_RX_DATA	I	PHTICD	UART Rx data

Power interface				
	P_VDD18A2	I	VDD1T_ABB	Digital power supply
	P_VSS18A2	I	VSS1T_ABB	Digital ground
	P_VDD18A1	I	VDD1T_ADD	Analog power supply
	P_VSS18A1	I	VSS1T_ABB	Analog ground
	P_VBBA	I	VBB1_ABB	bulk ground
	P_VDD1I	I	VDD1I	1.8 V internal power.
	P_VSS1I	I	VSS1I	1.8 V internal ground
	P_VDD3O	I	VDD3O	3.3 V output-driver power
	P_VSS3O	I	VSS3O	3.3 V output-driver ground
	P_VDD3P	I	VDD3P	3.3 V pre-driver power
	P_VSS3P	I	VSS3P	3.3 V pre-driver ground
	P_VDD3OP	I	VDD3OP	3.3 V output driver and pre-driver power
	P_VSS3OP	I	VSS3OP	3.3 V output driver and pre-driver ground

Table 1: Pin configuration

Pad	I/O	Description
PHTIC	I	5V tolerant for 3.3 V interface LVCMOS level input buffer
PHTICD	I	5V tolerant for 3.3 V interface LVCMOS level input buffer with pull-down register.
PHTOT4	OZ	5V tolerant for 3.3 V interface tri-state output buffer driving 4 mA
PHOB4	O	3.3 V LVCMOS normal output buffer driving 4 mA
PHOB2	O	3.3 V LVCMOS normal output buffer driving 2 mA
PHIC	I	3.3 V interface LVCMOS level input buffer
PHICD	I	3.3 V interface LVCMOS level input buffer with pull-down register.
PHICU	I	3.3 V interface LVCMOS level input buffer with pull-up resister
PHICD	I	3.3 V interface LVCMOS level input buffer with pull-down resister
PHIS	I	3.3 V interface LVCMOS Schmitt-trigger level input buffer
PHTBCT4	B	3.3 V interface 5 V tolerant LVCMOS level tri-state bi-directional buffer driving 4 mA
PHTBCT6SM	B	3.3 V interface 5 V tolerant LVCMOS level tri-state bi-directional buffer driving 6 mA medium slew rate control
PHTBCDT6SM	B	3.3 V interface 5 V tolerant LVCMOS level tri-state bi-directional buffer driving 6 mA medium slew rate control with pull-down register.
POAR50_ABB	O	Analog normal output pad for 1.8 V interface with resister 50 Ohm and separated bulk bias
PHSOSCM26	I/O	Oscillator cell with enable and feedback resistor.
VDD1T_ABB	I	Power, 1.8 V total with separate bulk bias
VSS1T_ABB	I	Ground, 1.8 V total with separate bulk bias
VBB1_ABB	I	Ground, 1.8 V bulk bias
VDD1I	I	VDD for 1.8 V internal power
VSS1I	I	VSS for 1.8 V internal power
VDD3O	I	VDD for 3.3 V output driver power
VSS3O	I	VSS for 3.3 V output driver power
VDD3P	I	VDD for 3.3 V pre- driver power
VSS3P	I	VSS for 3.3 V pre- driver power
VDD3OP	I	VDD for 3.3 V output driver and pre- driver power
VSS3OP	I	VSS for 3.3 V output driver and pre- driver power

Table 2: Pad description

4 Functional Description

The G.dmt ADSL transceiver consists of two main chips; G.dmt ADSL transceiver chip (S5N8950) and Analog Front End chip (S5N8951). The AFE provides an analog interface with line driver and hybrid components to connect the PSTN. The G.dmt ADSL transceiver provides all the digital functional as depicted in Figure 4.

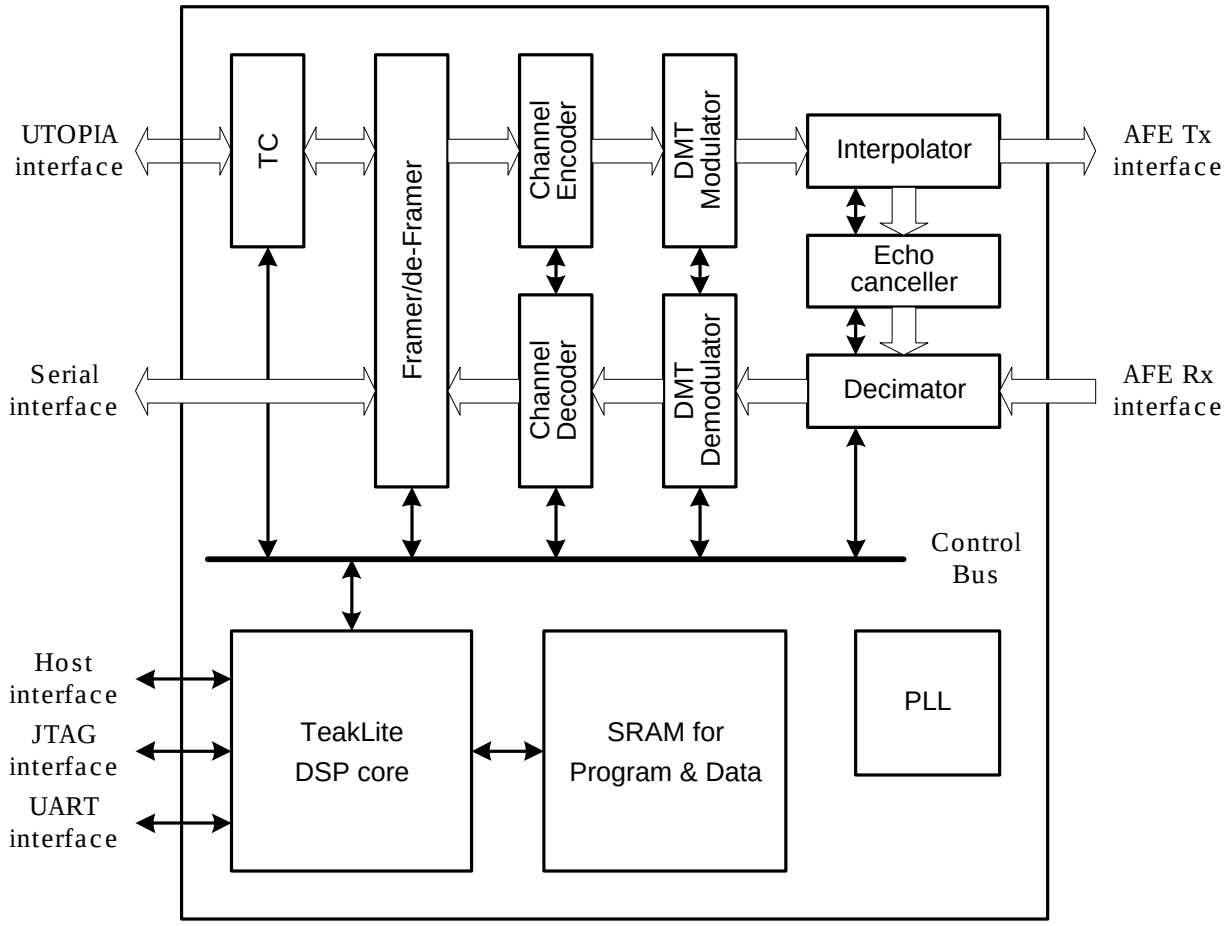

Figure 4: Block diagram

The input bit stream is divided into bit slices and they are fed into the QAM, which are allocated to 256 sub-channels according to the bit loading table. The bit slices are then converted to frequency-domain complex samples by the QAM encoder. The 256 complex samples are changed to 512 time-domain samples by IFFT. The Tx filter performs band separation and interpolation functions.

The received signals are attenuated and distorted in terms of both phase and amplitude. PLL fixes the phase errors within 4 samples using the 276 kHz pilot tone transmitted from the CO side. The ones over 4

samples are fixed by the sync recovery algorithm using a known synchronization symbol. The TEQ is a filter that adaptively alters the channel so that the impulse response is reduced to the length of the cyclic prefix which will be removed prior to FFT. The FEQ is a one tap complex adaptive filter for each sub-channel, which adjusts the gains and phases of the received signals. The equalizers are adaptively updated due to the transmission channel environment.

In FDM-based DMT modulation, the frequency band, 0 to 1.104 MHz, is divided into 256 equi-spaced sub-channels, of which 26 KHz (#6) to 134 KHz (#31) is allocated for the upstream, and 142 KHz (#33) to 1.100 MHz (#255) for the downstream. The Nyquist rate, therefore, should be 2.208 MHz (276kHz).

DMT inherently transmits an optimized time-variable spectrum. This spectrum is adjusted according to the desired data rate and the transmission characteristics (transfer function and noise spectrum) on each and every sub-channel. For this, CO and CPE transmit 128.4 KHz wide tone downstream and upstream respectively to each other during initialization. They measure the quality of each of these received tones and then decided whether a tone has sufficient quality to be used for further transmission and, if so, how much data this tone should carry relative to the other tones that are used. They inform the bit lo9ading result to each other.

5 I/O Timing Description

5.1 AFE Data Interface Timing Information

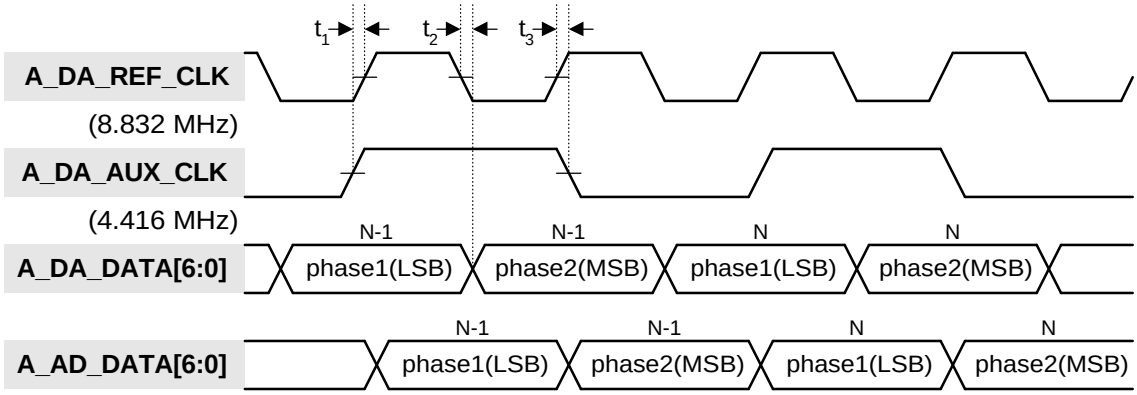

Table 3: AFE data interface timing diagram.

Parameter	Description	Min	Max	Unit
t_1	A_DA_AUX_CLK setup to A_DA_REF_CLK ↑		10	§ À
t_2	DATA delay after A_DA_REF_CLK ↓		10	§ À
t_3	A_DA_AUX_CLK hold to A_DA_REF_CLK ↑		10	§ À

Table 4: AFE data interface timing table.

5.2 AFE Control Interface Timing Information

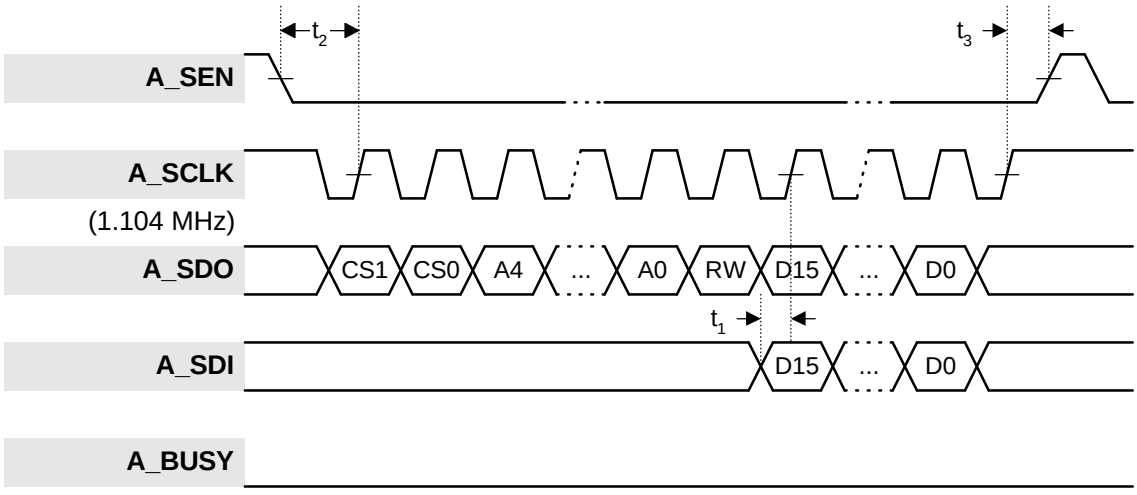

Figure 5: AFE control interface timing diagram.

Parameter	Description	Min	Max	Unit
t_1	A_SDI setup to A_SCLK ↑	30		§ À
t_2	A_SEN ↓ before A_SCLK ↑	30		§ À
t_3	A_SEN ↓ from A_SCLK ↑	15		§ À

Table 5: AFE control interface timing table.

5.3 Motorola Read Cycle Timing Information

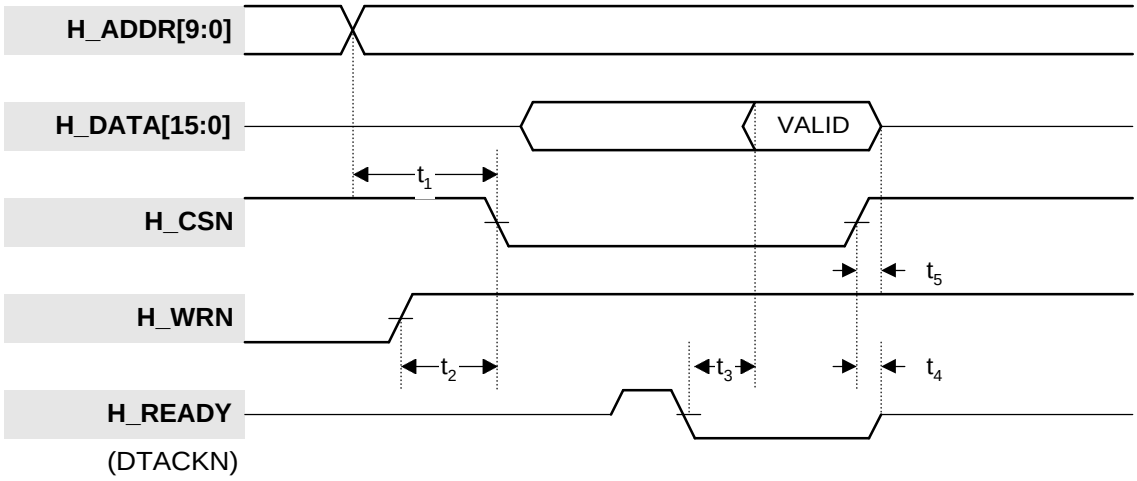

Figure 6: Motorola read cycle timing diagram.

Parameter	Description	Min	Max	Unit
t_1	H_ADDR setup to H_CSN ↓	0		§ À
t_2	H_WRN ↑ before H_CSN ↓	0		§ À
t_3	H_DATA valid from H_READY ↓		10	§ À
t_4	H_READY hi-Z from H_CSN ↑	1	5	§ À
t_5	H_DATA hold after H_CSN ↑		5	§ À

Table 6: Motorola read cycle timing table.

5.4 Motorola Write Cycle Timing Information

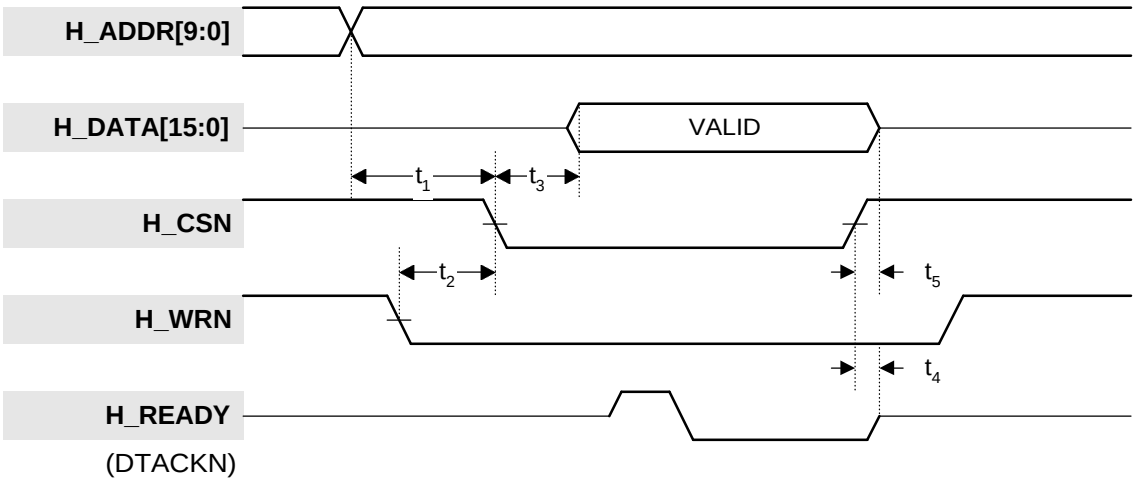

Figure 7: Motorola write cycle timing diagram.

Parameter	Description	Min	Max	Unit
t_1	H_ADDR setup to H_CSN ↓	0		§ À
t_2	H_WRN ↓ before H_CSN ↓	0		§ À
t_3	H_DATA valid from H_READY ↓		50	§ À
t_4	H_READY hi-Z from H_CSN ↑	1	5	§ À
t_5	H_DATA hold after H_CSN ↑	5		§ À

Table 7: Motorola write cycle timing table.

5.5 Intel Read Cycle Timing Information

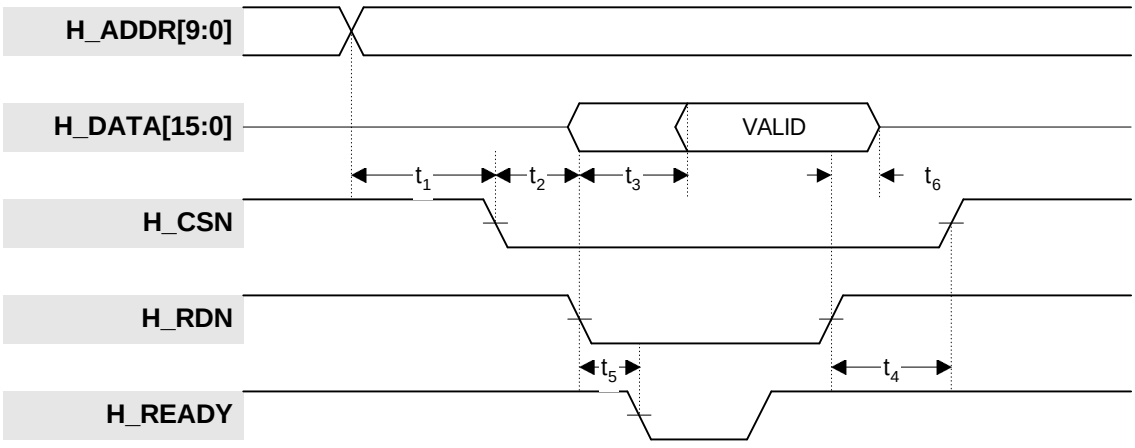

Figure 8: Intel read cycle timing diagram.

Parameter	Description	Min	Max	Unit
t_1	H_ADDR setup to H_CSN ↓	0		§ À
t_2	H_CSN ↓ before H_RDN ↓	0		§ À
t_3	H_DATA valid from H_RDN ↓		170	§ À
t_4	H_CSN ↑ from H_RDN ↑	0		§ À
t_5	H_READY ↓ from H_RDN ↓	0	20	§ À
t_6	H_DATA hold after H_RDN ↑		5	§ À

Table 8: Intel read cycle timing table.

5.6 Intel Write Cycle Timing Information

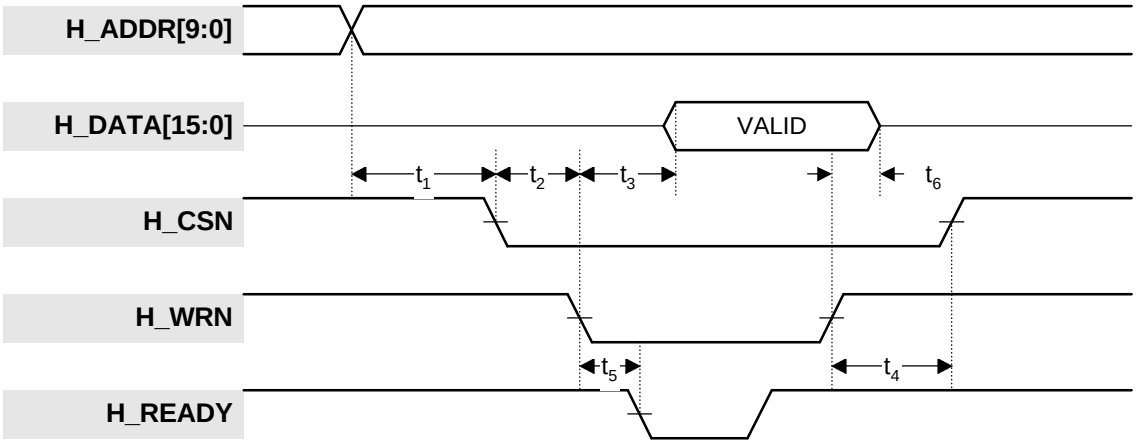

Figure 9: Intel write cycle timing diagram.

Parameter	Description	Min	Max	Unit
t_1	H_ADDR setup to H_CSN ↓	0		§ À
t_2	H_CSN ↓ before H_WRN ↓	0		§ À
t_3	H_DATA valid from H_WRN ↓		50	§ À
t_4	H_CSN ↑ from H_WRN ↑	0		§ À
t_5	H_READY ↓ from H_WRN ↓	0	20	§ À
t_6	H_DATA hold after H_WRN ↑	5		§ À

Table 9: Intel write cycle timing table.

5.7 Byte Mode Non-ATM Interface Timing Information.

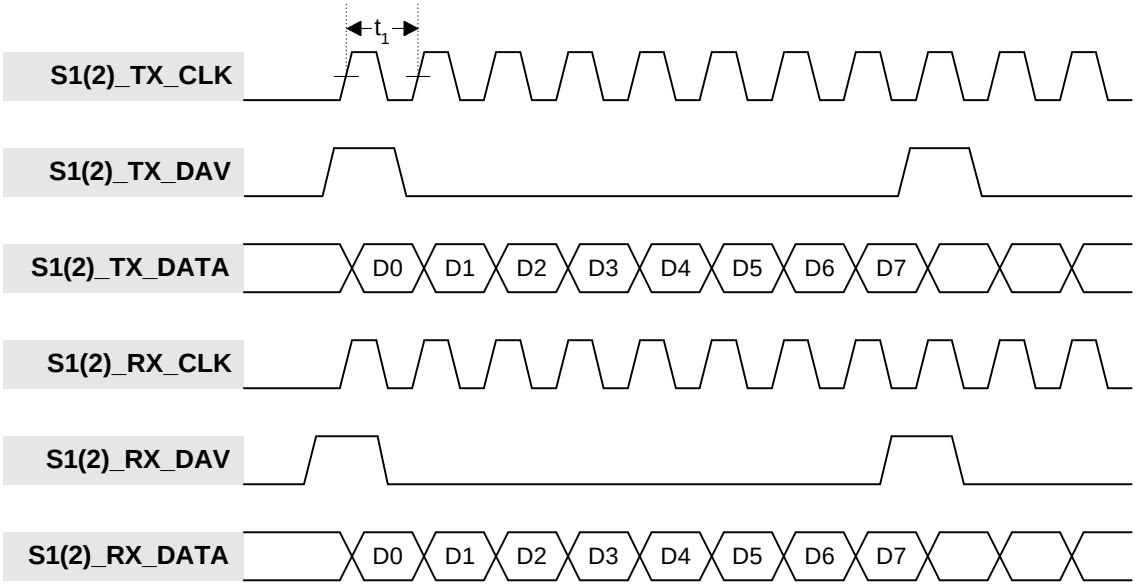

Figure 10: Byte mode non-ATM interface timing diagram.

Parameter	**Description**	**Min**	**Max**	**Unit**
t_1	S1(2)_TX_CLK frequency	1	25	MHz

Table 10: Byte mode non-ATM interface timing table.

5.8 Envelope Mode non-ATM Interface Timing Information

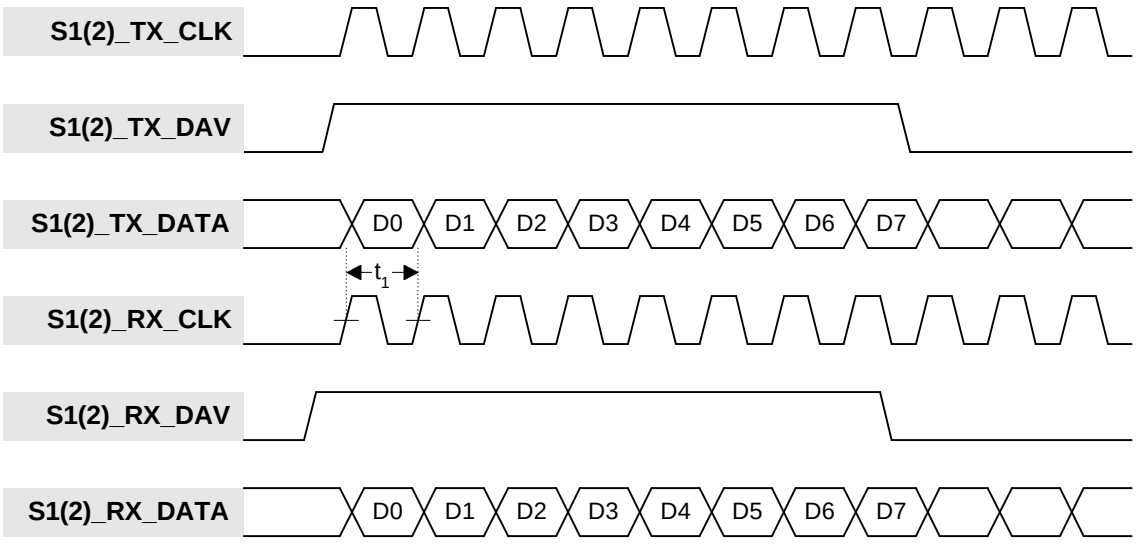

Figure 11: Envelope mode non-ATM interface timing diagram.

Parameter	Description	Min	Max	Unit
t_1	S1(2)_RX_CLK frequency	1	25	MHz

Table 11: Envelope mode non-ATM interface timing table.

5.9 UTOPIA-2 ATM Interface Timing Information

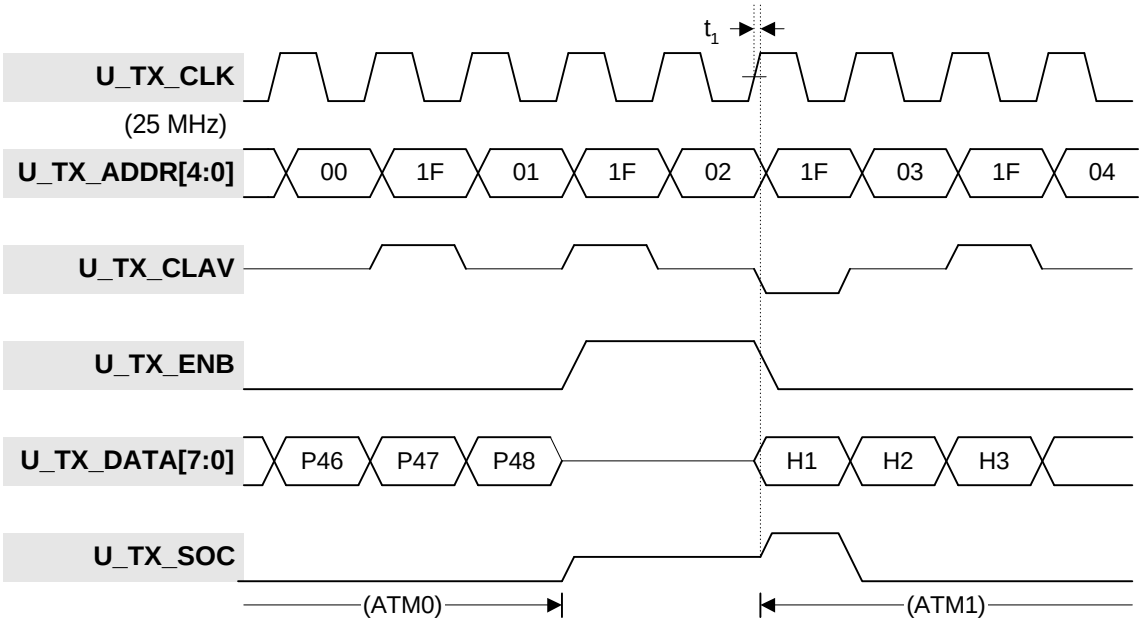

Figure 12: UTOPIA-2 ATM interface timing diagram.

Parameter	Description	Min	Max	Unit
t_1	Signal Hold after U_TX_CLK ↑	5	10	§ À

Table 12: UTOPIA-2 ATM interface timing table.

5.10 UTOPIA-2 ATM Interface Timing Information

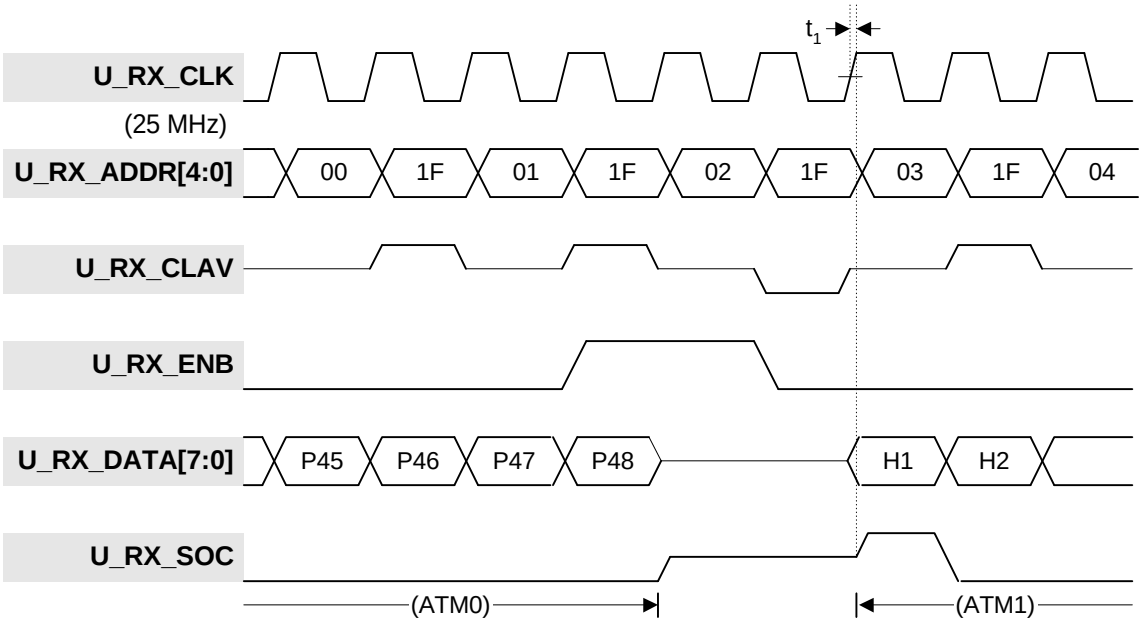

Figure 13: UTOPIA-2 ATM interface timing diagram.

Parameter	Description	Min	Max	Unit
t_1	Signal Hold after U_RX_CLK ↑	5	10	§ À

Table 13: UTOPIA-2 ATM interface timing table.

6 Electrical Characteristics

Symbol	**Parameter**	**Rating**	**Unit**
I_{LATCH}	Latch-up Current	± 200	mA
T_{STG}	Storage Temperature	£ 65 ~ 150	°C

Table 14: Absolute Maximum Ratings

Symbol	**Parameter**	**Rating**		**Unit**
V_{DD}	DC Input Voltage	1.8 V I/O	1.65 ~ 1.95	V
		3.3 V I/O	3.0 ~ 3.6	
		5V-tolerant I/O	3.0 ~ 3.6	
	Analog Core DC Supply Voltage	1.8 V Core	1.8±5%	
T_A	Operating Temperature (Ambient)		-40 to 85	°C

Table 15: Recommended Operating Conditions

Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
P_D	Power Dissipation		716		§ Ñ

Table 16: Power Dissipation

Symbol	**Parameters**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	Input High Voltage	2.0			V
V_{IL}	Input Low Voltage			0.8	
V_{OH}	Output High Voltage	2.4			
V_{OL}	Output Low Voltage			0.4	
VT	Switching Threshold		1.4		
VT^+	Schmitt Trigger, Positive-going Threshold			2.0	
VT^-	Schmitt Trigger, Negative-going Threshold	0.8			
I_{IH}	Input High Current ($V_{IN}=V_{DD}$)	-10(10)	(33)	10(60)	µA
I_{IL}	Input Low Current ($V_{IN}=V_{SS}$)	-10(-60)	(-33)	10(-10)	
I_{OZ}	Tri-state Output Leakage Current	-10		10	
I_{DD}	Quiescent Supply Current			100	
C_{IN}	Input Capacitance			4	pF
C_{OUT}	Output Capacitance			4	

NOTE: ( ) – Input buffer with pull-down

Table 17: DC Characteristics