25AA040/25LC040/25C040

4K SPI™ Bus Serial EEPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
25AA040	1.8-5.5V	1 MHz	C,I
25LC040	2.5-5.5V	2 MHz	C,I
25C040	4.5-5.5V	3 MHz	C,I,E

FEATURES

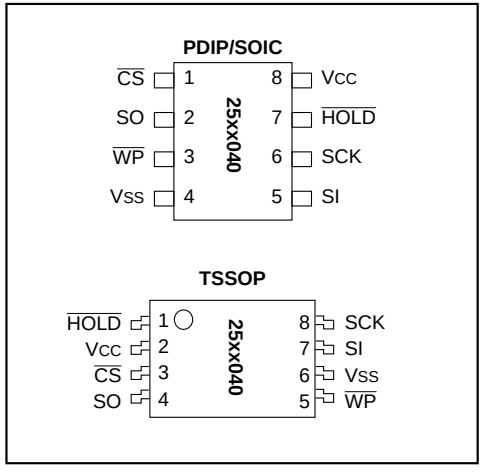
- Low power CMOS technology
  - Write current: 3 mA typical
  - Read current: 500 μA typical
  - Standby current: 500 nA typical
- 512 x 8 bit organization
- 16 byte page
- Write cycle time: 5ms max.
- Self-timed ERASE and WRITE cycles
- Block write protection
  - Protect none, 1/4, 1/2, or all of array
- Built-in write protection
  - Power on/off data protection circuitry
  - Write enable latch
  - Write protect pin
- Sequential read
- High reliability
  - Endurance: 1M cycles (guaranteed)
  - Data retention: > 200 years
  - ESD protection: > 4000 V
- 8-pin PDIP, SOIC, and TSSOP packages
- Temperature ranges supported:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E) (25C040): -40°C to +125°C

DESCRIPTION

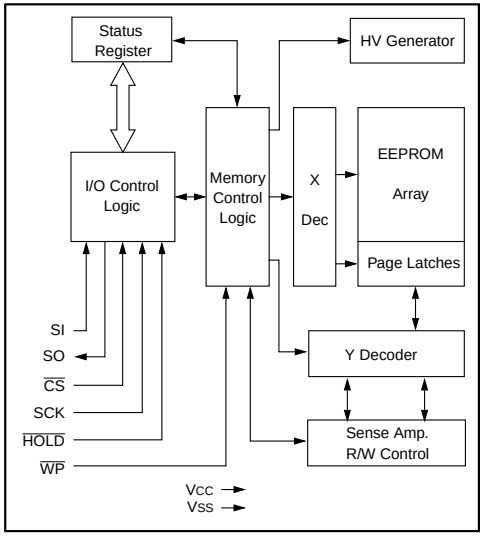
The Microchip Technology Inc. 25AA040/25LC040/25C040 (25xx040*) is a 4K bit serial Electrically Erasable PROM. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of chip select, allowing the host to service higher priority interrupts. Also, write operations to the device can be disabled via the write protect pin ($\overline{WP}$).

PACKAGE TYPES



BLOCK DIAGRAM



*25xx040 is used in this document as a generic part number for the 25AA040/25LC040/25C040 devices.
SPI is a trademark of Motorola.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

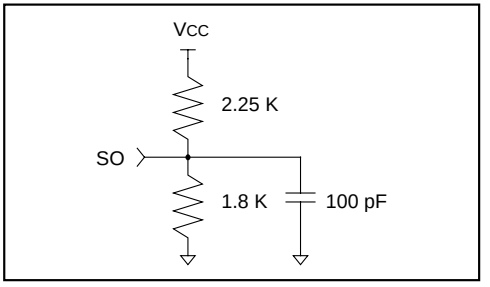
Vcc 7.0V
All inputs and outputs w.r.t. Vss..... -0.6V to Vcc+1.0V
Storage temperature ..... -65˚C to 150˚C
Ambient temperature under bias..... -65˚C to 125˚C
Soldering temperature of leads (10 seconds) ..... +300˚C
ESD protection on all pins.....4kV

***Notice:** Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Pin
VSS	Ground
VCC	Supply Voltage
$\overline{HOLD}$	Hold Input

FIGURE 1-2: AC TEST CIRCUIT



1.2 AC Test Conditions

AC Waveform:
VLO = 0.2V
VHI = VCC - 0.2V (Note 1)
VHI = 4.0V (Note 2)
Timing Measurement Reference Level
Input 0.5 VCC
Output 0.5 VCC

Note 1: For VCC ≤ 4.0V
2: For VCC > 4.0V

TABLE 1-3: DC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): TAMB = 0°C to +70°C VCC = 1.8V to 5.5V Industrial (I): TAMB = -40°C to +85°C VCC = 1.8V to 5.5V Automotive (E): TAMB = -40°C to +125°C VCC = 4.5V to 5.5V (25C040 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
High level input voltage	VIH1	2.0	VCC+1	V	VCC ≥ 2.7V (Note)
	VIH2	0.7 VCC	VCC+1	V	VCC< 2.7V (Note)
Low level input voltage	VIL1	-0.3	0.8	V	VCC ≥ 2.7V (Note)
	VIL2	-0.3	0.3 VCC	V	VCC < 2.7V (Note)
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA
	VOL	—	0.2	V	IOL = 1.0 mA, VCC < 2.5V
High level output voltage	VOH	VCC -0.5	—	V	IOH =-400 µA
Input leakage current	ILI	-10	10	µA	$\overline{CS}$ = VCC, VIN = VSS TO VCC
Output leakage current	ILO	-10	10	µA	$\overline{CS}$ = VCC, VOUT = VSS TO VCC
Internal Capacitance (all inputs and outputs)	CINT	—	7	pF	TAMB = 25˚C, CLK = 1.0 MHz, VCC = 5.0V (Note)
Operating Current	ICC Read	— —	1 500	mA µA	VCC = 5.5V; FCLK=3.0 MHz; SO = Open VCC = 2.5V; FCLK=2.0 MHz; SO = Open
	ICC Write	— —	5 3	mA mA	VCC= 5.5V VCC = 2.5V
Standby Current	ICCS	— —	5 2	µA µA	$\overline{CS}$ = Vcc = 5.5V, Inputs tied to VCC or VSS $\overline{CS}$ = Vcc = 2.5V, Inputs tied to VCC or VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-4: AC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): Industrial (I): Automotive (E):	Tamb = 0°C to +70°C Tamb = -40°C to +85°C Tamb = -40°C to +125°C		VCC = 1.8V to 5.5V VCC = 1.8V to 5.5V VCC = 4.5V to 5.5V (25C040 only)	
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
Clock Frequency	FCLK	— — —	3 2 1	MHz MHz MHz	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
$\overline{CS}$ Setup Time	TCSS	100 250 500	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
$\overline{CS}$ Hold Time	TCSH	150 250 475	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
$\overline{CS}$ Disable Time	TCSD	500	—	ns	
Data Setup Time	TSU	30 50 50	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
Data Hold Time	THD	50 100 100	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
CLK Rise Time	TR	—	2	µs	(Note 1)
CLK Fall Time	TF	—	2	µs	(Note 1)
Clock High Time	THI	150 250 475	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
Clock Low Time	TLO	150 250 475	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
Clock Delay Time	TCLD	50	—	ns	
Clock Enable Time	TCLE	50	—	ns	
Output Valid from Clock Low	TV	— — —	150 250 475	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
Output Hold Time	THO	0	—	ns	(Note 1)
Output Disable Time	TDIS	— — —	200 250 500	ns ns ns	VCC = 4.5V to 5.5V (Note 1) VCC = 2.5V to 4.5V (Note 1) VCC = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ Setup Time	THS	100 100 200	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
$\overline{HOLD}$ Hold Time	THH	100 100 200	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
$\overline{HOLD}$ Low to Output High-Z	THZ	100 150 200	— — —	ns ns ns	VCC = 4.5V to 5.5V (Note 1) VCC = 2.5V to 4.5V (Note 1) VCC = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ High to Output Valid	THV	100 150 200	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
Internal Write Cycle Time	TWC	—	5	ms	
Endurance	—	1M	—	E/W Cycles	(Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-5: HOLD TIMING

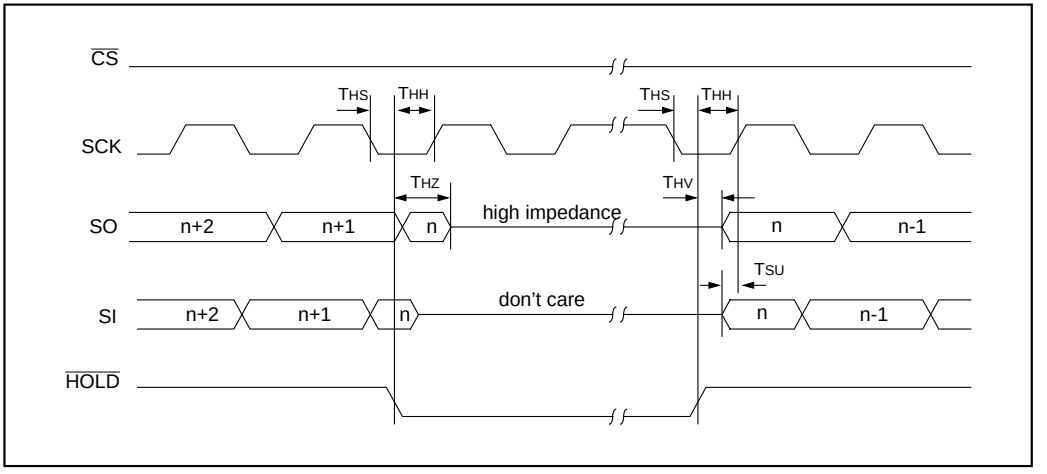


FIGURE 1-6: SERIAL INPUT TIMING

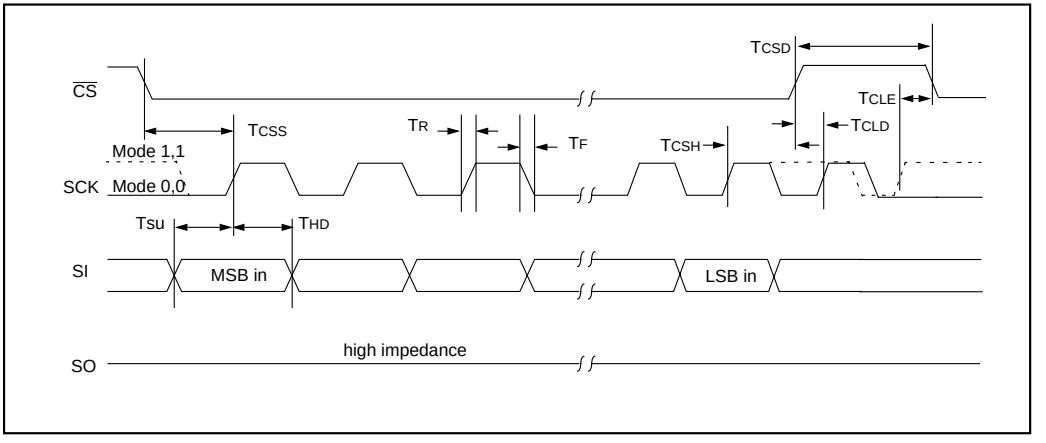
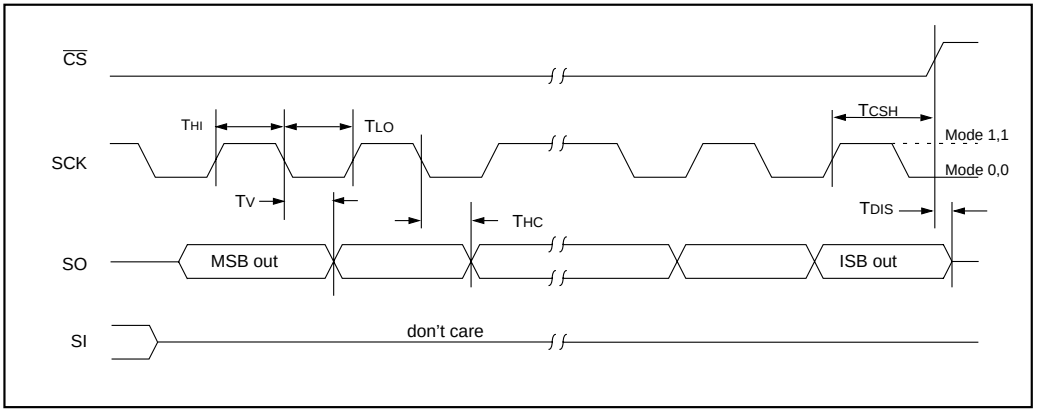


FIGURE 1-7: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go in standby mode as soon as the programming cycle is complete. As soon as the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus. A low to high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

2.3 Serial Output (SO)

The SO pin is used to transfer data out of the 25xx040. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.4 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25xx040. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.5 Write Protect ($\overline{WP}$)

This pin is a hardware write protect input pin. When $\overline{WP}$ is low, all writes to the array or status register are disabled, but any other operation functions normally. When $\overline{WP}$ is high, all functions, including non-volatile writes operate normally. $\overline{WP}$ going low at any time will reset the write enable latch and inhibit programming, except when an internal write has already begun. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write. See Table 3-7 for Write Protect Functionality Matrix.

2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25xx040 while in the middle of a serial sequence without having to re-transmit the entire sequence over at a later time. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high to low transition. The 25xx040 must remain selected during this sequence. The SI, SCK, and SO pins are in a high impedance state during the time the part is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 PRINCIPLES OF OPERATION

The 25xx040 is a 512 byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC16C6X/7X microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software.

The 25xx040 contains an 8-bit instruction register. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation. The $\overline{WP}$ pin must be held high to allow writing to the memory array.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. The most significant address bit (A8) is located in the instruction byte. All instructions, addresses, and data are transferred MSB first, LSB last.

Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25xx040 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

3.2 Read Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction with the A8 address bit is transmitted to the 25xx040 followed by the lower 8-bit address (A7 through A0). After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (01FFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-2).

3.3 Write Sequence

Prior to any attempt to write data to the 25xx040, the write enable latch must be set by issuing the WREN instruction (Figure 3-5). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25xx040. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a write instruction, followed by the address, and then the data to be written. Keep in mind that the most significant address bit (A8) is included in the instruction byte. Up to 16 bytes of data can be sent to the 25xx040 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with XXXX 0000 and ends with XXXX 1111. If the internal address counter reaches XXXX 1111 and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the least significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-3 and Figure 3-4 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the status register may be read to check the status of the WIP, WEL, BP1, and BP0 bits (Figure 3-8). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 $A_8$011	Read data from memory array beginning at selected address
WRITE	0000 $A_8$010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register

Note: A_8 is the 9^{th} address bit necessary to fully address 512 bytes.

FIGURE 3-2: READ SEQUENCE

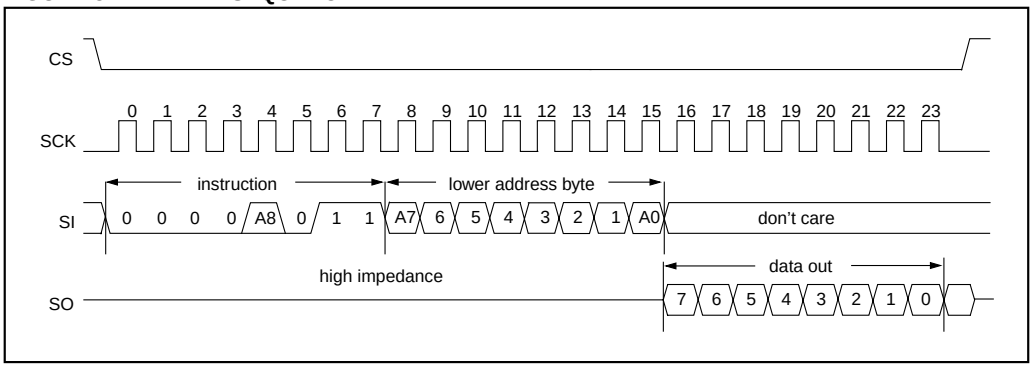


FIGURE 3-3: BYTE WRITE SEQUENCE

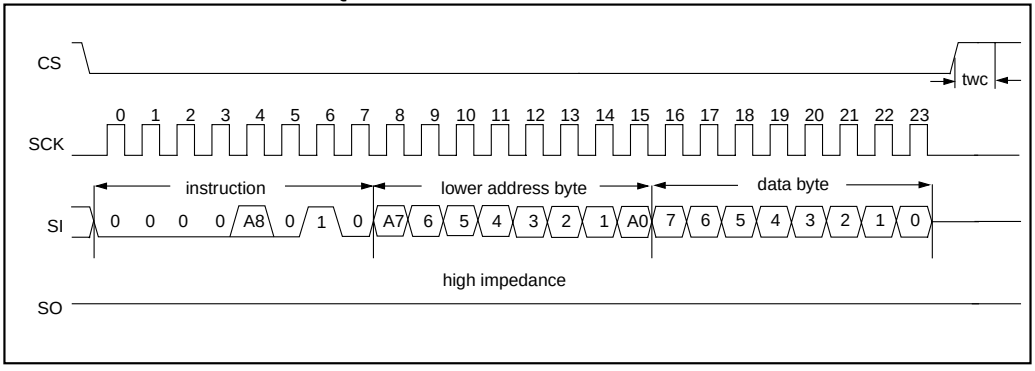
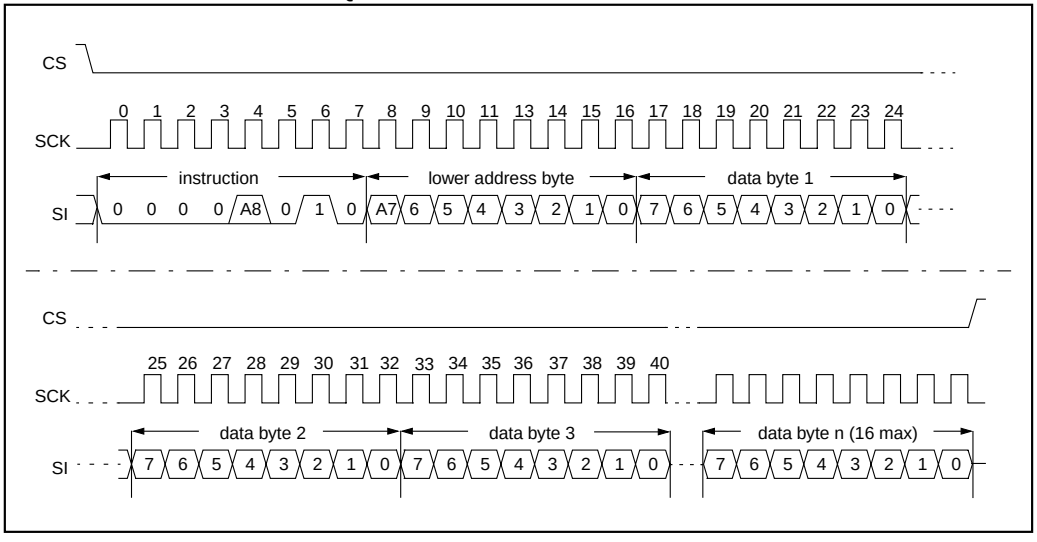


FIGURE 3-4: PAGE WRITE SEQUENCE



3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25xx040 contains a write enable latch. See Table 3-10 for the Write Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- $\overline{WP}$ line is low

FIGURE 3-5: WRITE ENABLE SEQUENCE

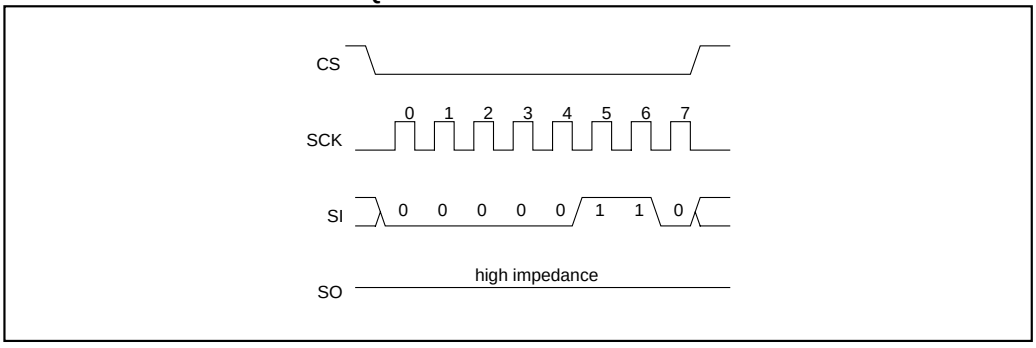
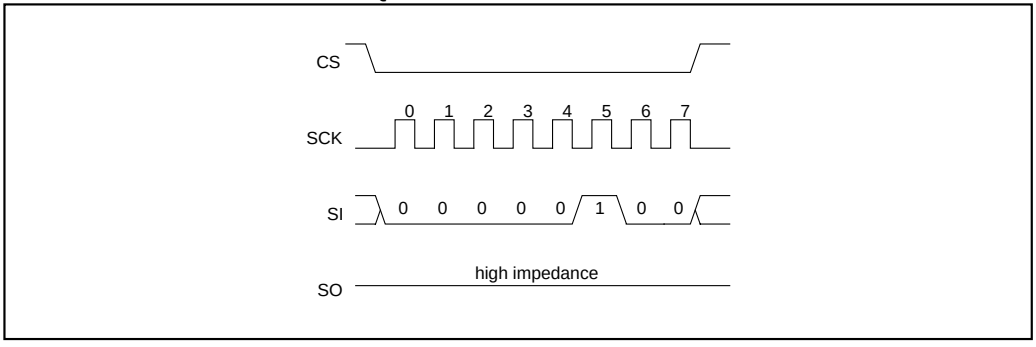


FIGURE 3-6: WRITE DISABLE SEQUENCE



3.5 Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the 25xx040 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress. This bit is read only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1' the latch allows writes to the array, when set to a '0' the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the status register. This bit is read only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write protected. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

See Figure 3-8 for RDSR timing sequence

3.6 Write Status Register(WRSR)

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the status register. The array is divided up into four segments. The user has the ability to write protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 3-7.

See Figure 3-9 for WRSR timing sequence

TABLE 3-7: ARRAY PROTECTION

BP1	BP0	Array Addresses Write Protected
0	0	none
0	1	upper 1/4 (0180h - 01FFh)
1	0	upper 1/2 (0100h - 01FFh)
1	1	all (0000h - 01FFh)

FIGURE 3-8: READ STATUS REGISTER SEQUENCE

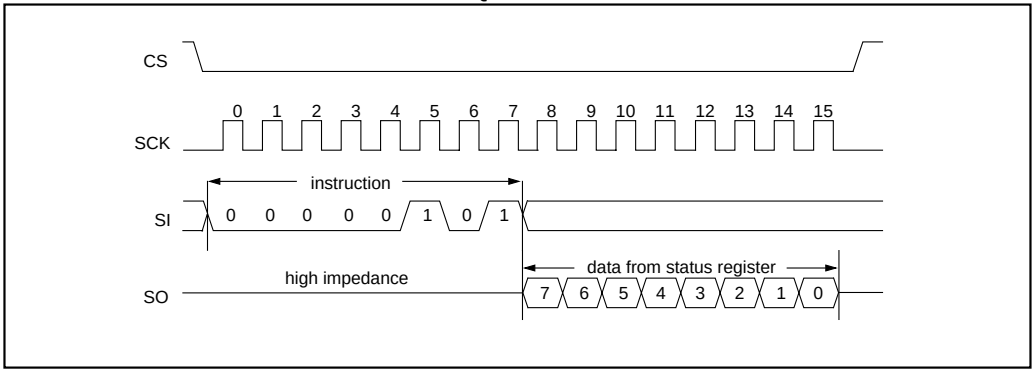
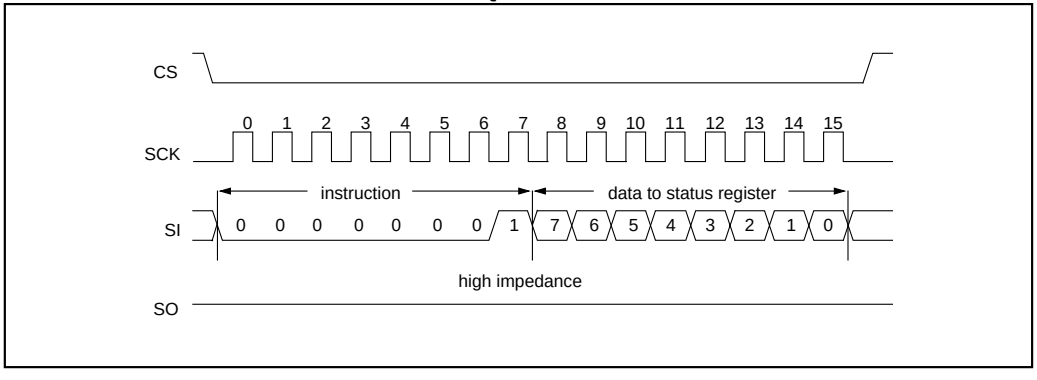


FIGURE 3-9: WRITE STATUS REGISTER SEQUENCE



3.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up.
- A write enable instruction must be issued to set the write enable latch.
- After a byte write, page write, or status register write, the write enable latch is reset.
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle.
- Access to the array during an internal write cycle is ignored and programming is continued.
- The write enable latch is reset when the $\overline{WP}$ pin is low.

3.8 Power On State

The 25xx040 powers on in the following state:

- The device is in low power standby mode ($\overline{CS}$ = 1).
- The write enable latch is reset.
- SO is in high impedance state.
- A low level on $\overline{CS}$ is required to enter active state.

.

TABLE 3-10: WRITE PROTECT FUNCTIONALITY MATRIX

WP	WEL	Protected Blocks	Unprotected Blocks	Status Register
Low	X	Protected	Protected	Protected
High	0	Protected	Protected	Protected
High	1	Protected	Writable	Writable

25AA040/25LC040/25C040 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

25xx040 — /P

Package:

P	= Plastic DIP (300 mil Body), 8-lead
SN	= Plastic SOIC (150 mil Body), 8-lead
ST	= TSSOP, 8-lead

Temperature Range:

Blank	= 0°C to +70°C
I	= –40°C to +85°C
E	= –40°C to +125°C

Devices:

25AA040	4096 bit 1.8V SPI Serial EEPROM
25AA040T	4096 bit 1.8V SPI Serial EEPROM Tape and Reel
25AA040X	4096 bit 1.8V SPI Serial EEPROM in alternate pinout (ST only)
25AA040XT	4096 bit 1.8V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
25LC040	4096 bit 2.5V SPI Serial EEPROM
25LC040T	4096 bit 2.5V SPI Serial EEPROM Tape and Reel
25LC040X	4096 bit 2.5V SPI Serial EEPROM in alternate pinout (ST only)
25LC040XT	4096 bit 2.5V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
25C040	4096 bit 5.0V SPI Serial EEPROM
25C040T	4096 bit 5.0V SPI Serial EEPROM Tape and Reel
25C040X	4096 bit 5.0V SPI Serial EEPROM in alternate pinout (ST only)
25C040XT	4096 bit 5.0V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

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