

Enhanced Current Mode PWM Controller

Description

The CS-51021/22/23/24 Fixed Frequency PWM Current Mode Controller provides all necessary features required for AC-DC or DC-DC primary side controller. In addition to basic functions needed for current mode operation, several features have been added minimizing the number of external components. In addition to the low startup current ($75\mu\text{A}$) and high frequency operation capability, the CS-51021/22/23/24 includes

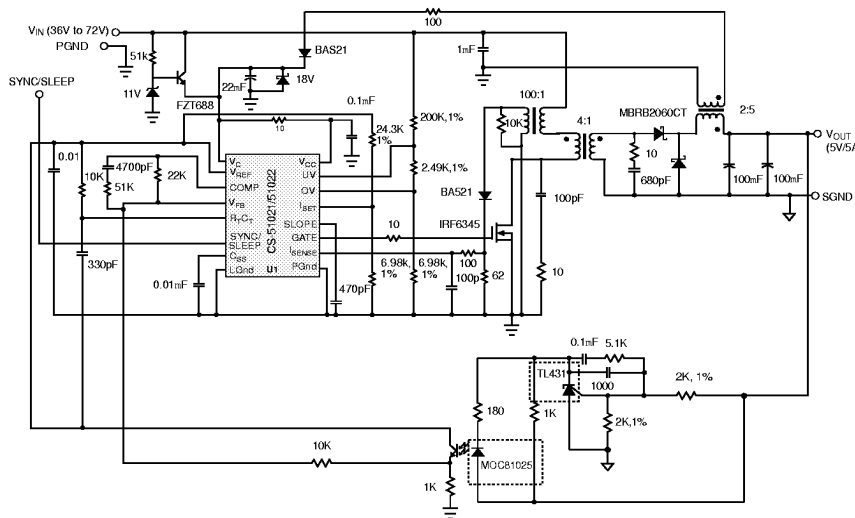
over/under voltage monitoring, externally programmable dual threshold overcurrent protection, current sense leading edge blanking, current slope compensation, bi-directional synchronization (CS-51021/CS-51023), an oscillator with accurate duty cycle control, a 5V reference, and a $100\mu\text{A}$ sleep current (CS-51022/CS-51024).

The CS-51021/22/23/24 is available in 16 pin PDIP and 16 pin SO narrow body packages.

Features

- **$75\mu\text{A}$ Max. Startup Current**
- **Fixed Frequency Current Mode Control**
- **1MHz Switching Frequency**
- **Under Voltage Protection Monitor**
- **Over Voltage Protection Monitor with Programmable Hysteresis**
- **Programmable Dual Threshold Overcurrent Protection with Delayed Restart**
- **Programmable Soft Start**
- **Accurate Maximum Duty Cycle Limit**
- **Programmable Slope Compensation**
- **Leading Edge Current Sense Blanking**
- **1A Sink/Source Gate Drive**
- **Bidirectional Synchronization (51021/23)**
- **50ns PWM Propagation Delay**
- **$100\mu\text{A}$ Max Sleep Current (51022/24)**

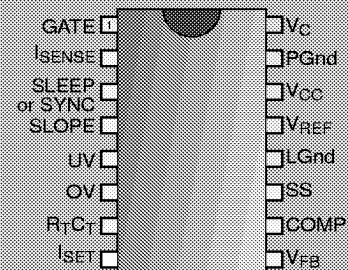
Typical Application Diagram



36-72V to 5V, 5A DC-DC Converter

Package Options

16 Lead PDIP & SO Narrow



Absolute Maximum Ratings

Power Supply Voltage, V_{CC}	-0.3V, 20V
Driver Supply Voltage, V_C	-0.3V, 20V
SYNC, SLEEP, $R_T C_T$, SOFT START, V_{FB} , SLOPE, I_{SENSE} , UV, OV, I_{SET} (Logic Pins).....	-0.25V to V_{REF}
Peak GATE Output Current.....	1A
Steady State Output Current.....	$\pm 0.2A$
Operating Junction Temperature, T_J	150°C
Operating Temperature Range, T_A	-40 to 85°C
Storage Temperature Range, T_S	-65 to 150°C
ESD (Human Body Model).....	2kV
Lead Temperature Soldering: Wave Solder (through hole styles only).....	10 sec. max, 260°C peak
Reflow (SMD styles only).....	60 sec. max above 183°C, 230°C peak

Electrical Characteristics: Unless otherwise stated, specifications apply for $-40^\circ\text{C} < T_A < 85^\circ\text{C}$, $-40^\circ\text{C} < T_J < 150^\circ\text{C}$, $3V < V_C < 20V$, $8.2V < V_{CC} < 20V$, $R_T = 12k\Omega$, $C_T = 390pF$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Under Voltage Lockout					
START Threshold (CS-51021/22)		7.95	8.25	8.8	V
START Threshold (CS-51023/24)		12.4	13	13.4	V
STOP Threshold		7.4	7.7	8.2	V
Hysteresis (CS-51021/22)		0.50	0.75	1.00	V
Hysteresis (CS-51023/24)		4	5	6	V
I_{CC} @ Startup (CS-51021/22)	$V_{CC} < UV_{START}$ Threshold		40	75	μA
I_{CC} @ Startup (CS-51023/24)	$V_{CC} < UV_{START}$ Threshold		45	75	μA
I_{CC} Operating (CS-51021/23)			7	9	mA
I_{CC} Operating (CS-51022/24)			6	8	mA
I_C Operating	Includes 1nF Load		7	12	mA
■ Voltage Reference					
Initial Accuracy	$T_A = 25^\circ\text{C}$, $I_{REF} = 2\text{mA}$, $V_{CC} = 14\text{V}$ (Note1)	4.95	5	5.05	V
Total Accuracy	$1\text{mA} < I_{REF} < 10\text{mA}$	4.9	5	5.15	V
Line Regulation	$8.2V < V_{CC} < 18V$, $I_{REF} = 2\text{mA}$		6	20	mV
Load Regulation	$1\text{mA} < I_{REF} < 10\text{mA}$		6	15	mV
NOISE Voltage	$10\text{Hz} < F < 10\text{KHz}$		50		μV
OP Life Shift	$T = 1000$ Hours (Note 1)		4	20	mV
FAULT Voltage	Force V_{REF}	$.92 \cdot V_{REF}$	$.95 \cdot V_{REF}$	$.97 \cdot V_{REF}$	V
OK Voltage	Force V_{REF}	$.94 \cdot V_{REF}$	$.96 \cdot V_{REF}$	$.98 \cdot V_{REF}$	V
OK Hysteresis	Force V_{REF}	50	100	150	mV
Current Limit	Force V_{REF}	-20	-55	-100	mA
■ Error Amplifier					
Initial Accuracy	$T_A = 25^\circ\text{C}$, $I_{REF} = 2\text{mA}$, $V_{CC} = 14V$, $V_{FB} = COMP$ (Note 1)	2.465	2.515	2.565	V
Reference Voltage	$V_{FB} = COMP$	2.440	2.515	2.590	V
V_{FB} Leakage Current	$V_{FB} = 0V$		-0.2	-2	μA
Open Loop Gain	$1.4V < COMP < 4V$ (Note 1)	60	90		dB
Unity Gain Bandwidth	(Note 1)	1.5	2.5		MHz
COMP Sink Current	$COMP = 1V$, $V_{FB} = 2.7V$	2	6		mA
COMP Source Current	$COMP = 1.5V$, $V_{FB} = 2.3V$	-0.2	-0.5		mA

Electrical Characteristics: $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$, $-40^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$, $3\text{V} < V_C < 20\text{V}$, $8.2\text{V} < V_{CC} < 20\text{V}$,
 $R_T = 12\text{k}\Omega$, $C_T = 390\text{pF}$, unless otherwise stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Error Amplifier continued					
COMP High Voltage	$V_{FB} = 2.3\text{V}$	4.35	4.8	5	V
COMP Low Voltage	$V_{FB} = 2.7\text{V}$	0.4	0.8	1.2	V
PS Ripple Rejection	FREQ = 120Hz (Note 1)	60	85		dB
SS Clamp, V_{COMP}	$V_{SS} = 2.5\text{V}$, $V_{FB} = 0\text{V}$, $I_{SET} = 2\text{V}$	2.4	2.5	2.6	V
$I_{LIM(SET)}$ Clamp	$V_{FB} = 2.3\text{V}$, $V_{ISET} = 1\text{V}$, $V_{SLOPE} = 2\text{V}$	0.95	1	1.15	V
■ Oscillator					
Accuracy	$R_T = 12\text{k}$, $C_T = 390\text{pF}$	230	255	280	kHz
Voltage Stability	Delta Frequency $8.2\text{V} < V_{CC} < 20\text{V}$		2	3	%
Temperature Stability	$T_{MIN} < T_A < T_{MAX}$ (Note1)		8		%
Min Charge & Discharge Time	(Note1)	0.333			μs
Duty Cycle Accuracy	$R_T = 12\text{k}$, $C_T = 390\text{pF}$	70	77	83	%
Peak Voltage	(Note1)		3		V
Valley Voltage	(Note1)		1.5		V
Valley Clamp Voltage	10k Resistor to ground on $R_T C_T$	1.2	1.4	1.6	V
Discharge Current		0.8	1	1.2	mA
Discharge Current	$T_A = 25^{\circ}\text{C}$ (Note 1)	0.925	1	1.075	mA
■ Synchronization (CS-51021/23)					
Input Threshold		1.0	1.5	2.7	V
Output Pulsewidth		160	260	360	ns
Output High Voltage	$I_{SYNC} = 100\mu\text{A}$	3.5	4.3	4.8	V
Input Resistance	Resistance to ground	35	70	140	k Ω
Drive Delay	SYNC to GATE RESET	90	120	150	ns
Output Drive Current	1k Load	1.25	2	2.75	mA
■ SLEEP (CS-51022/24)					
SLEEP Input Threshold	Active High	1.0	1.5	2.7	V
SLEEP Input Current	$V_{SLEEP} = 4\text{V}$	11	25	46	μA
I_{CC} @ SLEEP	$V_{CC} \leq 15\text{V}$		50	100	μA
■ GATE Driver					
HIGH Voltage	Measure V_C -GATE, $V_C = 10\text{V}$, 200mA Load		1.5	2	V
LOW Voltage	Measure GATE-PGnd, 200mA SINK		1.2	1.5	V
HIGH Voltage Clamp	$V_C = 20\text{V}$, 1nF	11	13.5	16	V
LOW Voltage Clamp	Measured at 10mA Output Current		0.6	0.8	V
Peak Current	$V_C = 20\text{V}$, 1nF (Note 1)		1		A
UVL Leakage	$V_C = 20\text{V}$, measured at 0V		-1	-50	μA
RISE Time	Load = 1nF, $1\text{V} < \text{GATE} < 9\text{V}$, $V_C = 20\text{V}$, $T_A = 25^{\circ}\text{C}$		60	100	ns
FALL Time	Load = 1nF, $9\text{V} > \text{GATE} > 1\text{V}$, $V_C = 20\text{V}$		15	40	ns

Electrical Characteristics: Unless otherwise stated, specifications apply for $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$, $-40^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$, $3\text{V} < V_C < 20\text{V}$, $8.2\text{V} < V_{CC} < 20\text{V}$, $R_T = 12\text{k}\Omega$, $C_T = 390\text{pF}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ SLOPE Compensation					
Charge Current	SLOPE = 0V	-63	-53	-43	μA
COMP Gain	Fraction of slope voltage added to I_{SENSE} (Note 1)	0.095	0.100	0.105	V/V
Discharge Voltage	SYNC = 0V		0.1	0.2	V
■ Current Sense					
OFFSET Voltage	Slope = $I_{\text{SENSE}} = 0\text{V}$	0.09	0.10	0.11	V
Blanking Time		10	55	100	ns
Blanking Disable Voltage	Adjust V_{FB}	1.8	2	2.2	V
Second Current Threshold Gain		1.21	1.33	1.45	V/V
I_{SENSE} Input Resistance		3	5	10	$\text{k}\Omega$
Minimum On Time	GATE High to Low	30	70	110	ns
Gain	Slope = $I_{\text{SET}} = 2\text{V}$	0.78	0.80	0.82	V/V
■ OV & UV Voltage Monitors					
OV Monitor Threshold		2.4	2.5	2.6	V
OV Hysteresis Current		-10	-12.5	-15	μA
UV Monitor Threshold		1.38	1.45	1.52	V
UV Monitor Hysteresis		25	75	100	mV
■ SOFT START (SS)					
Charge Current	SS = 2V	-45	-55	-65	μA
Discharge Current	SS = 2V	250	1000		μA
Charge Voltage, V_{SS}		4.4	4.7	5	V
Discharge Voltage, V_{SS}		0.25	0.27	0.30	V

Note 1: Guaranteed by Design, not 100% tested in production.

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
16L PDIP & SO Narrow		
1	GATE	External power switch driver with 1.0A peak capability.
2	I_{SENSE}	Current sense amplifier input.
3	SYNC (CS-51021/23)	Bi-directional synchronization. Locks to the highest frequency.
3	SLEEP (CS-51022/24)	Active high chip disable. In sleep mode, V_{REF} and GATE are turned off.
4	SLOPE	Additional slope to the current sense signal. Internal current source charges the external capacitor.
5	UV	Undervoltage protection monitor.
6	OV	Overvoltage protection monitor.

Package Pin Description: continued

PACKAGE PIN #	PIN SYMBOL	FUNCTION
16L PDIP & SO Narrow		
7	$R_T C_T$	Timing resistor R_T and capacitor C_T determine oscillator frequency and maximum duty cycle, D_{MAX} .
8	I_{SET}	Voltage at this pin sets pulse-by-pulse overcurrent threshold, and second threshold (1.33 times higher) with soft start retrigger (hiccup mode).
9	V_{FB}	Feedback voltage input. Connected to the error amplifier inverting input.
10	COMP	Error amplifier output. Frequency compensation network is usually connected between COMP and V_{FB} pins.
11	SS	Charging external capacitor restricts error amplifier output voltage during the start or fault conditions (hiccup).
12	LGnd	Logic ground.
13	V_{REF}	5.0V reference voltage output.
14	V_{CC}	Logic supply voltage.
15	PGnd	Output power stage ground connection.
16	V_C	Output power stage supply voltage.

Block Diagram

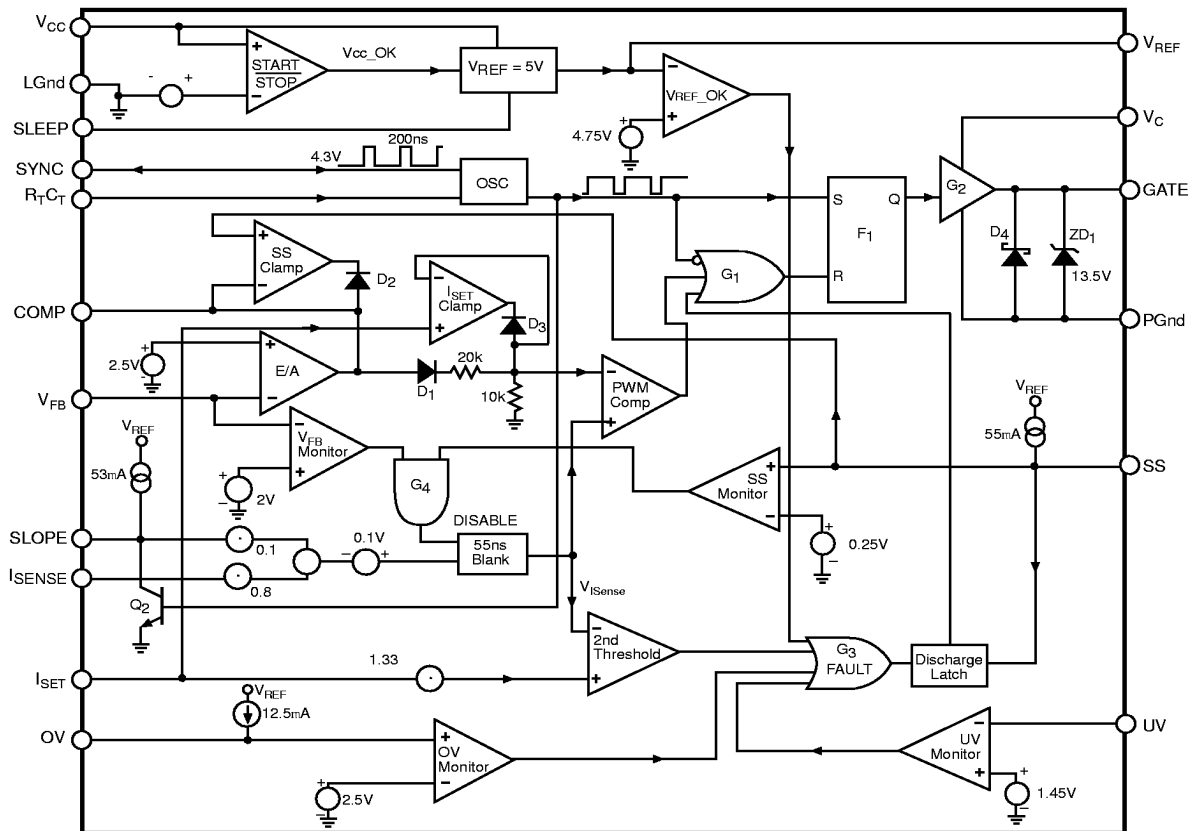


Figure 1: CS-51021/22/23/24 Block Diagram

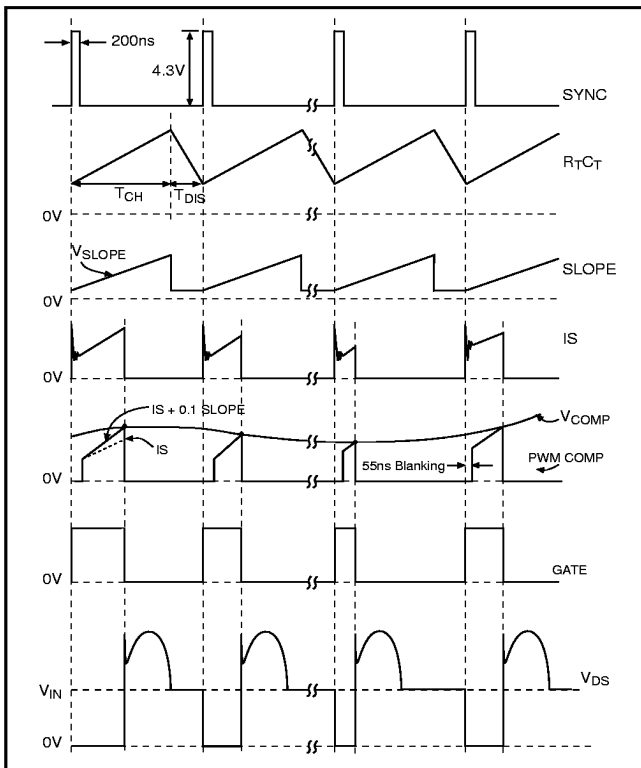


Figure 2: Typical Waveforms

Theory of Operation

Powering the IC

The IC has two supply and two ground pins. V_C and PGnd pins provide high speed power drive for the external power switch. V_{CC} and LGnd pins power the control portion of the IC. The internal logic monitors the supply voltage, V_{CC} . During abnormal operating conditions, the output stage is held at a low impedance state. The CS-51021/22/23/24 requires only 75 μ A of startup current.

Voltage Feedback

The output voltage is monitored via the V_{FB} pin and is compared with the internal 2.5V reference. The error amplifier output minus one diode drop is divided by 3 and connected to the negative input of the PWM comparator. The positive input of the PWM comparator is connected to the modified current sense signal. The oscillator turns the external power switch on at the beginning of each cycle. When current sense ramp voltage exceeds the reference side of PWM comparator, the output stage latches off. It is turned on again at the beginning of the next oscillator cycle.

Current Sense and Protection

The current is monitored at the I_{SENSE} pin. The CS-51021/22/23/24 has leading edge blanking circuitry that ignores the first 55ns of each switching period. Blanking is disabled when V_{FB} is less than 2V so that the minimum on-time of the controller does not have an additional 55ns of delay time during fault conditions. For the remaining portion of the switching period, the current sense signal,

combined with a fraction of the slope compensation voltage, is applied to the positive input of the PWM comparator where it is compared with the divided by three error amplifier output voltage. The pulse-by-pulse overcurrent protection threshold is set by the voltage at the I_{SET} pin. This voltage is passed through the I_{SET} Clamp and appears at the non-inverting input of the PWM comparator, limiting its dynamic range according to the following formula:

$$\text{Overcurrent Threshold} = 0.8 \cdot V_{I(\text{SENSE})} + 0.1V + 0.1 V_{\text{SLOPE}}$$

where

$V_{I(\text{SENSE})}$ is voltage at the I_{SENSE} pin

and

V_{SLOPE} is voltage at the SLOPE pin.

During extreme overcurrent or short circuit conditions, the slope of the current sense signal will become much steeper than during normal operation. Due to loop propagation delay, the sensed signal will overshoot the pulse-by-pulse threshold eventually reaching the second overcurrent protection threshold which is 1.33 times higher than the first threshold and is described by the following equation:

$$\text{2nd Threshold} = 1.33 \cdot V_{I(\text{SET})}$$

Exceeding the second threshold will reset the soft start capacitor C_{SS} and reinitiate the soft start sequence, repeating for as long as the fault condition persists.

Soft Start

During power up, when the output filter capacitor is discharged and the output voltage is low, the voltage across the soft start capacitor (V_{SS}) controls the duty cycle. An internal current source of 55 μ A charges C_{SS} . The maximum error amplifier output voltage is clamped by the SS Clamp. When the soft start capacitor voltage exceeds the error amplifier output voltage, the feedback loop takes over the duty cycle control. The soft start time can be estimated with the following formula:

$$t_{SS} = 9 \cdot 10^4 \cdot C_{SS}$$

The Soft Start voltage, V_{SS} , charges and discharges between 0.25V and 4.3V.

Slope Compensation

DC-DC converters with current mode control require a current sense signal with slope compensation to avoid instability at duty cycles greater than 50%. Slope capacitor C_S is charged by an internal 53 μ A current source and is discharged during the oscillator discharge time. The slope compensation voltage is divided by 10 and is added to the current sense voltage, $V_{I(\text{SENSE})}$. The signal applied to the input of the PWM comparator is a combination of these two voltages. The slope compensation voltage, V_{SLOPE} , is calculated using the following formula:

$$V_{\text{SLOPE}} = 0.1 \cdot \frac{53\mu\text{A} \cdot t_{\text{CHARGE}}}{C_S}$$

where t_{CHARGE} is power switch on-time at the maximum input voltage.

Undervoltage (UV) and Overvoltage (OV) Monitor

Two independent comparators monitor OV and UV conditions. A string of three resistors is connected in series between the monitored voltage and ground (see Figure 3). When voltage at the OV pin exceeds 2.5V, an overvoltage condition is detected and GATE shuts down. An internal 12.5μA current source turns on and feeds current into the external resistor, R₃, creating a hysteresis determined by the value of this resistor (the higher the value, the greater the hysteresis). The hysteresis voltage of the OV monitor is determined by the following formula:

$$V_{OV(HYST)} = 12.5\mu A \cdot R_3$$

where R₃ is a resistor connected from the OV pin to ground.

When the input voltage is low and the UV pin is less than 1.45V, GATE shuts down. The UV pin has fixed 75mV hysteresis.

Both OV and UV conditions are latched until the soft start capacitor is discharged. This way, every time a fault condition is detected the controller goes through the power up sequence.

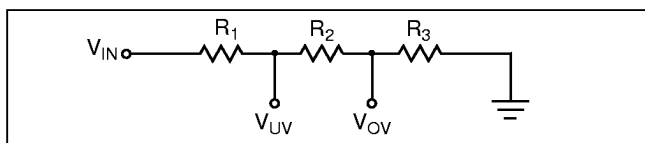


Figure 3: UV/OV Monitor Divider

The following procedure is suggested to calculate the OV/UV resistor divider.

1. Solve for R₃, based on OV hysteresis requirements.

$$R_3 = \frac{V_{OV(HYST)} \cdot 2.5V}{V_{OV} \cdot 12.5\mu A},$$

where V_{OV(HYST)} is the desired amount of overvoltage hysteresis.

2. Find the total impedance of the divider.

$$R_{TOT} = R_1 + R_2 + R_3 = \frac{V_{(OV)} \cdot R_3}{2.5}$$

3. Determine the value of R₂ from the UV threshold conditions.

$$R_2 = \frac{1.45 \cdot R_{TOT}}{V_{(UV)}} - R_3,$$

where V_{UV} is the UV voltage.

4. Now, the value of R₁ can be found.

$$R_1 = R_{TOT} - R_2 - R_3$$

5. Calculate the amount of undervoltage hysteresis seen at V_{IN}.

$$V_{UV(HYST)} = \frac{V_{UV} \cdot 0.075}{1.45}$$

Synchronization

A bi-directional synchronization is provided to synchronize several controllers. When SYNC pins are connected

together, the converters will lock to the highest switching frequency. The fastest controller becomes the master, producing a 4.3V, 200ns pulse train. Only one, the highest frequency SYNC signal, will appear on the SYNC line.

Sleep

The sleep input is an active high input. The CS-51022/51024 is placed in sleep mode when SLEEP is driven high. In sleep mode, the controller and MOSFET are turned off. Connect to Gnd for normal operation. The sleep mode operates at V_{CC} ≤ 15V.

Oscillator and Duty Cycle Limit

The switching frequency is set by R_T and C_T connected to the R_TC_T pin. C_T charges and discharges between 3V and 1.5V.

The maximum duty cycle is set by the ratio of the on time, t_{ON}, and the whole period, T = t_{ON} + t_{OFF}. Because the timing capacitor's discharge current is trimmed, the maximum duty cycle is well defined. It is determined by the ratio between the timing resistor R_T and the timing capacitor C_T. Refer to figures 4 and 5 to select appropriate values for R_T and C_T.

$$f_{SW} = \frac{1}{T_{SW}}; T_{SW} = t_{CH} + t_{DIS}$$

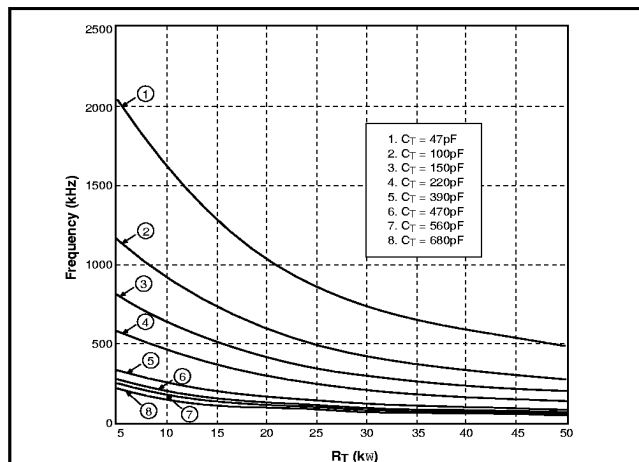


Figure 4: Frequency vs. R_T for Discrete Capacitor Values.

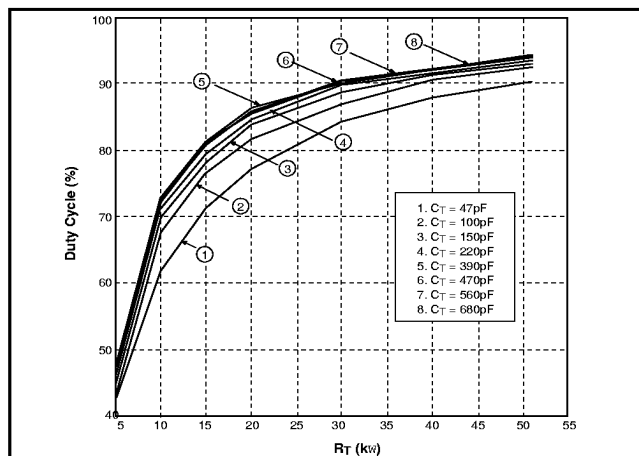


Figure 5: Duty Cycle vs. R_T for Discrete Capacitor Values.

Package Specification

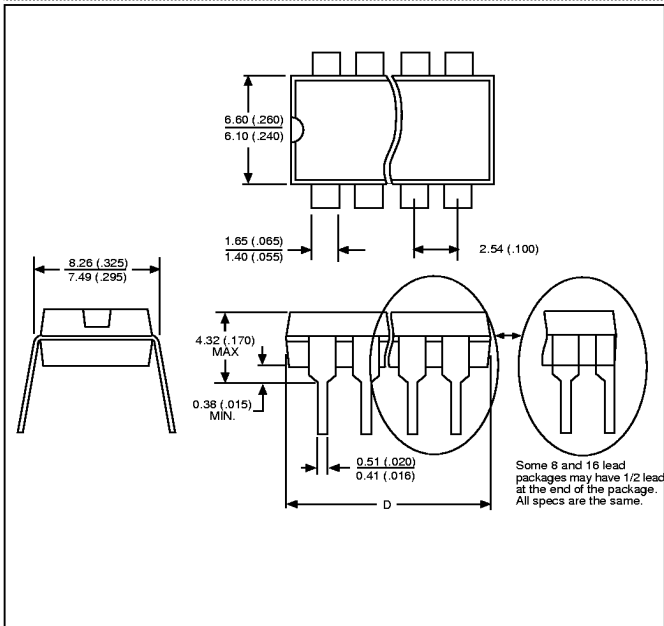
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L SO Narrow	10.00	9.80	.394	.385
16L PDIP	19.18	18.92	.755	.745

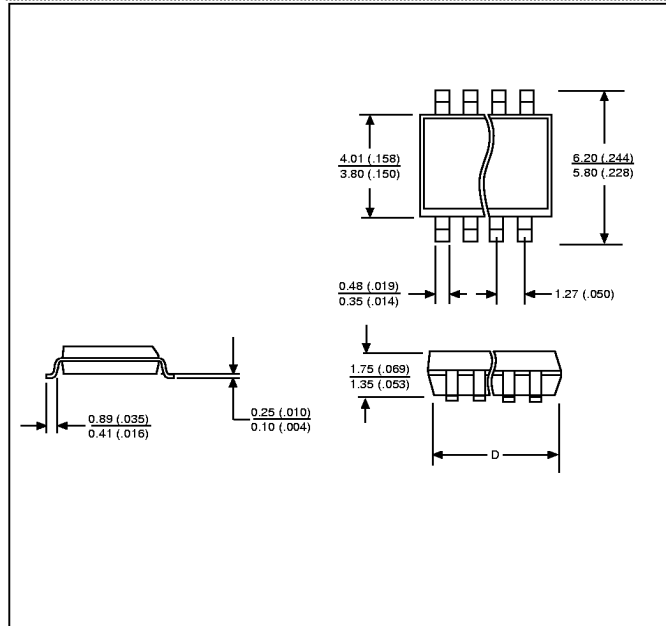
PACKAGE THERMAL DATA

Thermal Data		16L SO Narrow	16L PDIP	
$R_{\theta JC}$	typ	28	42	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	typ	115	80	$^{\circ}\text{C}/\text{W}$

16L SO Narrow, 150 mil wide



16L PDIP, 300 mil wide



Ordering Information

Part Number	Description
CS-51021D16	16L SO Narrow
CS-51021DR16	16L SO Narrow Tape & Reel
CS-51021N16	16L PDIP
CS-51022D16	16L SO Narrow
CS-51022DR16	16L SO Narrow Tape & Reel
CS-51022N16	16L PDIP
CS-51023D16	16L SO Narrow
CS-51023DR16	16L SO Narrow Tape & Reel
CS-51023N16	16L PDIP
CS-51024D16	16L SO Narrow
CS-51024DR16	16L SO Narrow Tape & Reel
CS-51024N16	16L PDIP

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