

## 2M x 16 Static RAM Module

### Features

- High-density 32-megabit SRAM module
- Low active power
  - 5.3W (max.) at 25 ns
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of 0.725 in.
- Available in 80 pin SIMM Package

### Functional Description

The CYM8210 is a high-performance 8-megabit static RAM module organized as 2M words by 16 bits. This module is constructed using eight 512K x 8 SRAMs (CY62148) in SOJ packages mounted on an epoxy laminate board with pins.

Writing to each byte is accomplished by enabling the appropriate Chip Select ( $\overline{E0}$ ,  $\overline{E1}$ ,  $\overline{E2}$ ,  $\overline{E3}$ ) and write enable ( $\overline{WH}$  or  $\overline{WL}$ ).

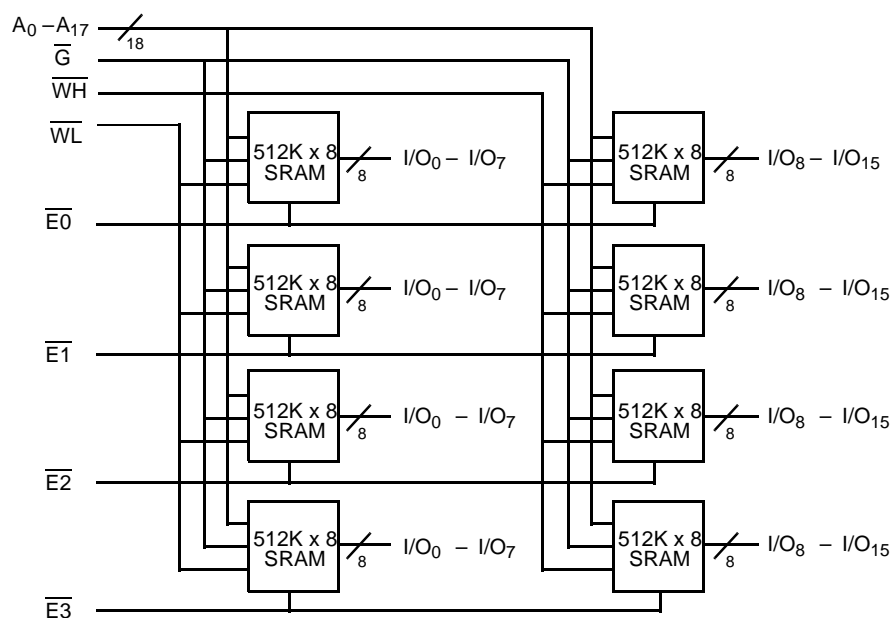
Data on the input/output pins (I/O) is written into the memory location specified on the address pins ( $A_0$  through  $A_{17}$ ).

Reading the device is accomplished by taking the appropriate chip select ( $\overline{E0}$ ,  $\overline{E1}$ ,  $\overline{E2}$ ,  $\overline{E3}$ ) LOW while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

The CYM8210 module is shipped as a 80 pin SIMM.

### Logic Block Diagram



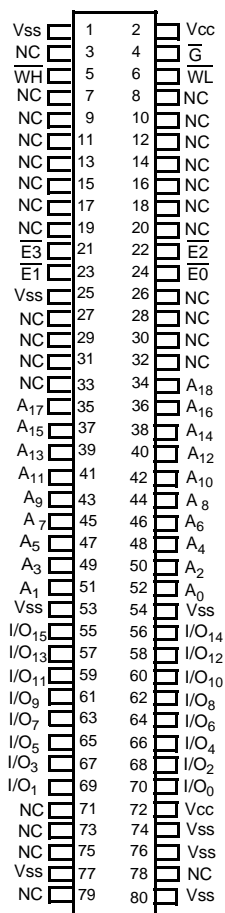
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## Selection Guide

	8210-70
Maximum Access Time (ns)	70
Maximum Operating Current (mA)	158
Maximum Standby Current ( $\mu$ A)	150

## Pin Configurations

**80-Pin  
SIMM  
Top View**



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Ambient Temperature with  
Power Applied  $-10^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Supply Voltage to Ground Potential  $-0.5\text{V}$  to  $+7.0\text{V}$

DC Voltage Applied to Outputs  
in High Z State  $-0.5\text{V}$  to  $+7.0\text{V}$

DC Input Voltage  $-0.5\text{V}$  to  $+7.0\text{V}$

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$

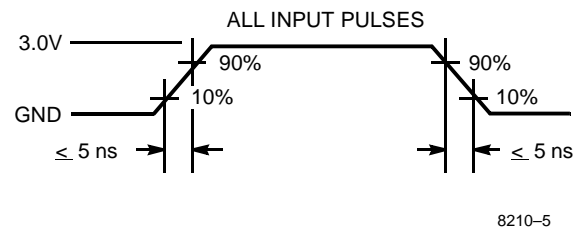
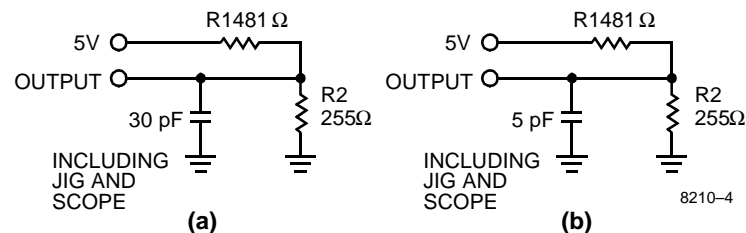
## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM8210-70		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = $-1.0\text{ mA}$	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = $2.1\text{ mA}$		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage		$-0.3$	0.8	V
I <sub>Ix</sub>	Input Leakage Current	$\text{GND} \leq V_I \leq V_{CC}$	$-10$	$+10$	$\mu\text{A}$
I <sub>OZ</sub>	Output Leakage Current	$\text{GND} \leq V_O \leq V_{CC}$ , Output Disabled	$-10$	$+10$	$\mu\text{A}$
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = $0\text{ mA}$ , CS $\leq V_{IL}$		158	mA
I <sub>SB1</sub>	Automatic $\overline{\text{CS}}$ Power-Down Current <sup>[1]</sup>	Max. V <sub>CC</sub> , $\overline{\text{CS}} \geq V_{IH}$ , Min. Duty Cycle = 100%		120	mA
I <sub>SB2</sub>	Automatic CS Power-Down Current <sup>[1]</sup>	Max. V <sub>CC</sub> , $\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$ , V <sub>IN</sub> $\geq V_{CC} - 0.2\text{V}$ , or V <sub>IN</sub> $\leq 0.2\text{V}$		150	$\mu\text{A}$

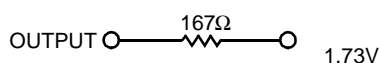
## Capacitance<sup>[2]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = $25^{\circ}\text{C}$ , f = $1\text{ MHz}$ , V <sub>CC</sub> = $5.0\text{V}$	60	pF
C <sub>OUT</sub>	Output Capacitance		50	pF

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



### Notes:

1. A pull-up resistor to V<sub>CC</sub> on the  $\overline{\text{E3/E2/E1/E0}}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
2. Tested on a sample basis.

**Switching Characteristics** Over the Operating Range<sup>[3]</sup>

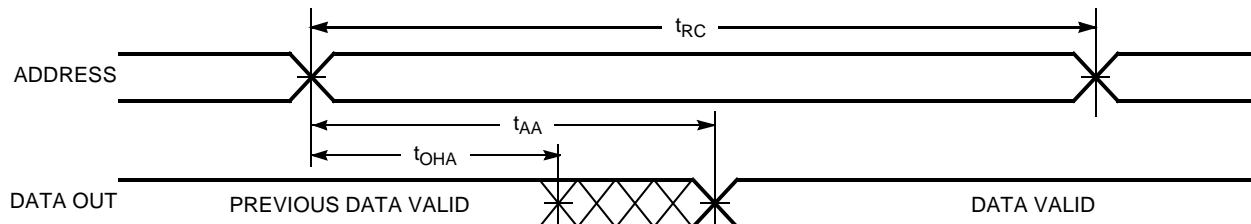
Parameter	Description	70 ns		Unit
		Min.	Max.	
READ CYCLE				
t <sub>RC</sub>	Read Cycle Time	70		ns
t <sub>AA</sub>	Address to Data Valid		70	ns
t <sub>OHA</sub>	Output Hold from Address Change	10		ns
t <sub>ACS</sub>	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ LOW to Data Valid		70	ns
t <sub>DOE</sub>	$\overline{G}$ LOW to Data Valid		35	ns
t <sub>LZOE</sub>	$\overline{G}$ LOW to Low Z	5		ns
t <sub>HZOE</sub>	$\overline{G}$ HIGH to High Z		25	ns
t <sub>LZCS</sub>	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ LOW to Low Z <sup>[4]</sup>	10		ns
t <sub>HZCS</sub>	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ HIGH to High Z <sup>[4, 5]</sup>		25	ns
t <sub>PD</sub>	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ HIGH to Power-Down		70	
WRITE CYCLE <sup>[6]</sup>				
t <sub>WC</sub>	Write Cycle Time	70		ns
t <sub>SCS</sub>	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ LOW to Write End	60		ns
t <sub>AW</sub>	Address Set-Up to Write End	60		ns
t <sub>HA</sub>	Address Hold from Write End	0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		ns
t <sub>PWE</sub>	$\overline{WH}/\overline{WL}$ Pulse Width	55		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		ns
t <sub>HD</sub>	Data Hold from Write End	0		ns
t <sub>LZWE</sub>	$\overline{WH}/\overline{WL}$ HIGH to Low Z	5		ns
t <sub>HZWE</sub>	$\overline{WH}/\overline{WL}$ LOW to High Z <sup>[5]</sup>		25	ns

**Notes:**

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
4. At any given temperature and voltage condition,  $t_{HZCS}$  is less than  $t_{LZCS}$  for any given device. These parameters are guaranteed by design and not 100% tested.
5.  $t_{HZCS}$  and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads and Waveforms. Transition is measured  $\pm 500$  mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of  $\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$  LOW and  $\overline{WH}/\overline{WL}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

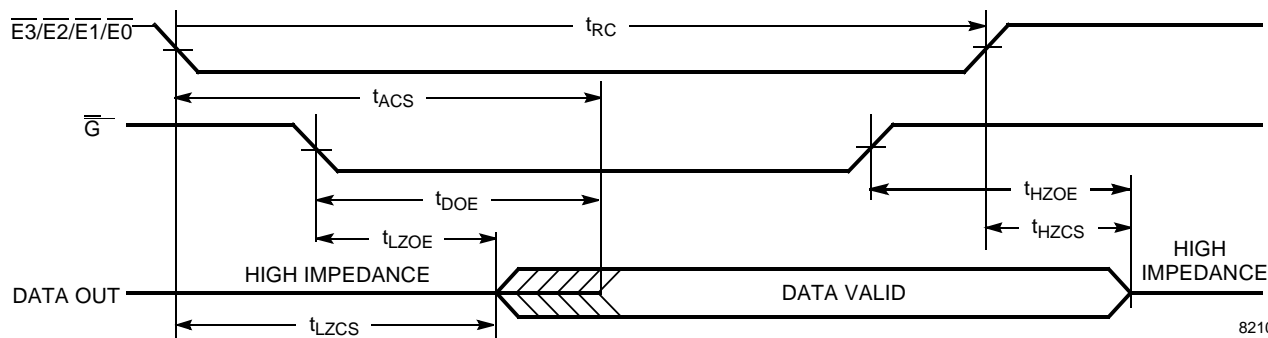
## Switching Waveforms

### Read Cycle No. 1<sup>[7, 8]</sup>



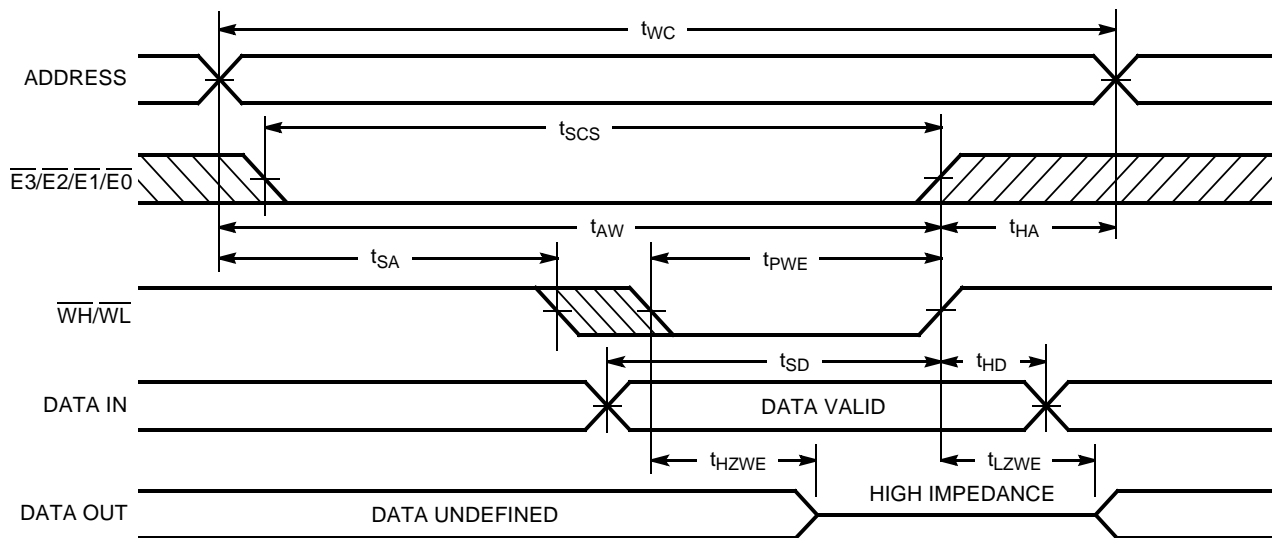
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### Read Cycle No. 2<sup>[7, 9]</sup>



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### Write Cycle No. 1 ( $\overline{WE}$ Controlled)<sup>[6]</sup>

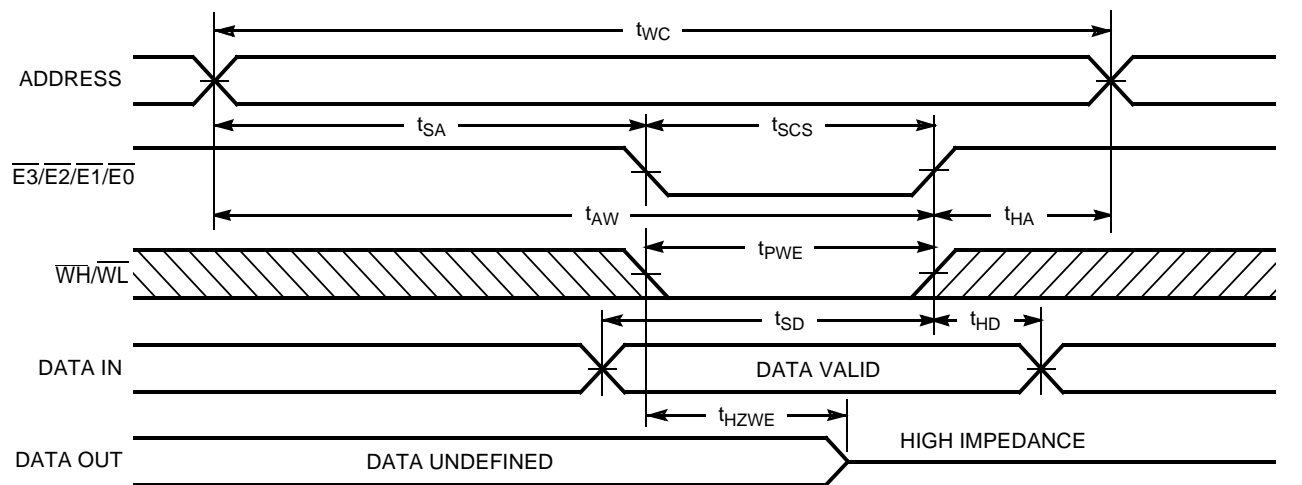


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#### Notes:

7.  $\overline{WH/WL}$  is HIGH for read cycle.
8. Device is continuously selected,  $\overline{E3/E2/E1/E0} = V_{IL}$  and  $\overline{G} = V_{IL}$ .
9. Address valid prior to or coincident with  $\overline{E3/E2/E1/E0}$  transition LOW.

**Switching Waveforms** (continued)

**Write Cycle No. 2 ( $\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$  Controlled)<sup>[6, 10]</sup>**


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**Note:**

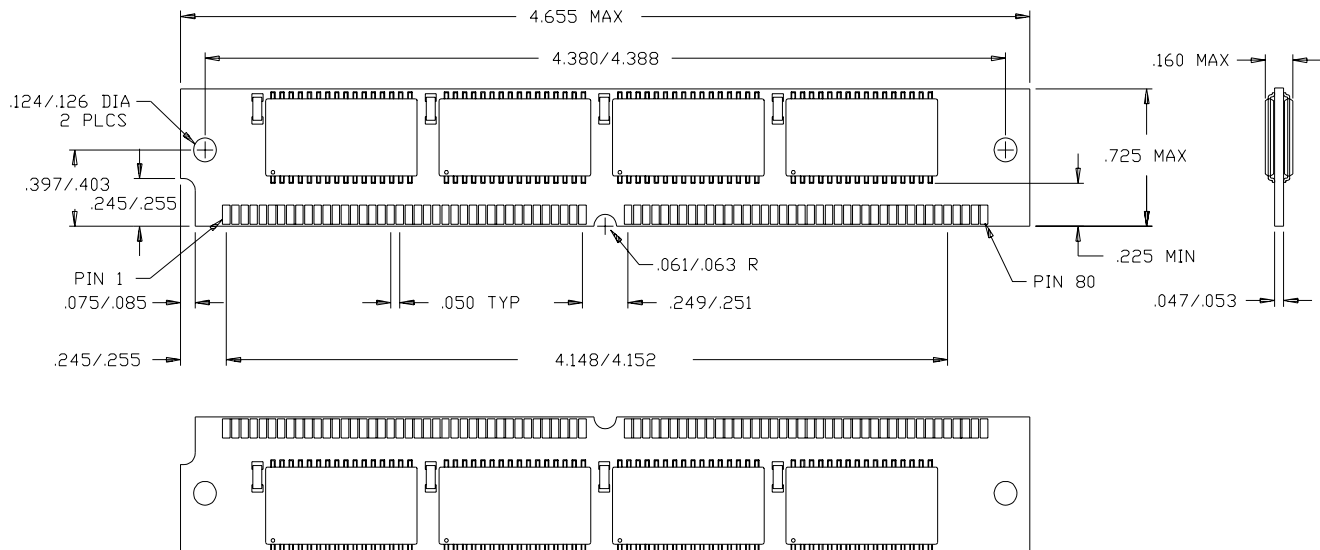
10. If  $\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$  goes HIGH simultaneously with  $\overline{WH}/\overline{WL}$  HIGH, the output remains in a high-impedance state.

## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CYM8210BPM-70C	PM49	80-Pin Plastic SIMM Module	Commercial

## Package Diagrams

**80-Pin Plastic SIMM Module PM49**



Document Title: CYM8210BPM 2M X 16 SRAM Module Datasheet  
Document Number: 38-05008

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106011	05/07/01	MEG	New Data Sheet